PRS-753

Line Protection

Instruction Manual

CYG SUNRI CO., LTD.

Preface

User's Guideline

This instruction manual contains full information of the equipment, including function descriptions, logic diagrams, input signals, output signals, setting parameters and technical parameters. It also lists the operations on safe handling, commissioning and maintaining of this equipment. The instruction manual can be used as a technical reference during the whole product life cycle.

Documentation and manufactured equipment purchased from CYG SUNRI CO., LTD. are dispatched separately due to the necessary manufacturing period. Therefore, they sometimes may not reach the recipients at the same time. Therefore, this manual is provided as a technical reference to commission the equipment.

The installation and commissioning personnel should read all relevant chapters carefully and get a thorough knowledge of the contents of this manual, before conducting any operation to the equipment. In this way, the personnel can get the required knowledge in handling electronic equipment.

This manual contains a security chapter which describes the safety precautions recommended when using the equipment. Before installing and using the equipment, this chapter is recommended to be thoroughly read and understood.

Personnel Security

The content in this chapter specifically describes to prevent and reduce the safety accidents in electric power production and construction procedures, to ensure the personal safety and health of employees in production activities and to ensure the power grids stable operation and reliable power supply.

Any kind of directly touching with the metal parts of the electrical equipment should be avoided when electrical equipment is on operation, because of the potential electric shock risk. Neglecting warning notices should be prevented because the improperly operation may damage the device, even cause personnel injury.

The good operating condition of the equipment depends on proper shipping and handling, proper storage, installation, commissioning and maintenance. Therefore, only qualified personnel should be allowed to operate the equipment. Intended personnel are individuals who:

- Have a thorough knowledge of protection systems, protection equipment, protection functions and the configured functional logic in the IEDs;
- Have a basic knowledge in the installation, commissioning, and operation of the equipment;
- Are familiar with the working field where it is being installed;
- Are able to safely perform operations in accordance with accepted safety engineering steps;
- Are authorized to energize and de-energize equipment, and to isolate, ground, and label it;

- Are trained in the maintenance and use of safety apparatus in accordance with safety engineering regulations;
- Have been trained in first aid if any emergency situations happen.

Warning Indications

The following indicators and standard definitions are used:

⚠ **DANGER!** means that death, severe personal injury and considerable equipment damage will occur if safety precautions are disregarded.

⚠ **WARNING!** means that death, severe personal and considerable equipment damage could occur if safety precautions are disregarded.

⚠ **CAUTION!** means that light personal injury or equipment damage may occur if safety precautions are disregarded.

NOTICE! is particularly applies to damage to device and to resulting damage of the protected equipment.

DANGER!

NEVER allow the current transformer (CT) secondary circuit connected to this equipment to be opened while the primary system is live. Opening the CT circuit will produce a dangerously high voltage.

WARNING!

ONLY qualified personnel should work on or in the vicinity of this device. This personnel **MUST** be familiar with all safety regulations and service procedures described in this manual. During operating of electrical device, certain part of the device is under high voltage. Severe personal injury and significant device damage could result from improper behavior.

WARNING!

Do **NOT** touch the exposed terminals of this device while the power supply is on. The generated high voltage causes death, injury, and device damage.

WARNING!

Thirty seconds is **NECESSARY** for discharging the voltage. Hazardous voltage can be present in the DC circuit just after switching off the DC power supply.

CAUTION!

- **Earthing**

  Securely earthed the earthing terminal of the device.

- **Operating environment**

  ONLY use the device within the range of ambient environment and in an environment free of abnormal vibration.

- **Ratings**

  Check the input ratings **BEFORE** applying AC voltage/current and power supply to the device.

- **Printed circuit board**

  Do **NOT** attach or remove printed circuit board if the device is powered on.

- **External circuit**

  Check the supply voltage used when connecting the device output contacts to external circuits, in order to prevent overheating.

- **Connection cable**

  Carefully handle connection cables without applying excessive force.

NOTICE!

The firmware may be upgraded to add new features or enhance/modify existing features, please **MAKE SURE** that the version of this manual is compatible with the product in your hand.

the products and to make improvements to the documents without notice.

The users are responsible for understanding the information and should not rely on this information as absolute. If the users do act upon the suggestions contained in this document, the users should be responsible for themself and their actions.

CYG SUNRI CO., LTD.

Headquarters: No.13, Keji North 1st Road, North Area of Hi-tech Industral Park, Nanshan District, Shenzhen, China

Tel: +86-400-678-8099

Website: http://www.sznari.com

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Documentation Outline

The manual provides a functional and technical description of this relay and a comprehensive set of instructions for the relay's use and application.

All contents provided by this manual are summarized as below:

1 Briefly Introduction

Briefly introduce the application scope, the selectable functions and product features about this equipment.

2 Technical Specifications

Introduce the technical specifications about this relay, including electrical specifications, mechanical specifications, ambient temperature and humidity range, communication interface parameters, type tests, setting ranges and accuracy limits etc.

3 Protection Functions

Provide a comprehensive and detailed protection function description of all protection modules.

4 Supervision Functions

Introduce the automatic self-supervision function of this equipment.

5 Monitoring & Control

Introduce the measurement, controlling, signaling, recording and other functions of this relay.

6 Hardware

Introduce the main module functions of this relay and describe the definition of all terminals of each module.

7 Human Machine Interface

Include all the menus of device.

8 Configuration Function

Introduce the configurable function (such as protection function configuration, LED configuration, binary input configuration and binary output configuration, analog quantities channels etc.) of this relay.

9 Communication Protocol

Introduce the communication interfaces and protocol that this relay contains. IEC60970-5-103 and IEC61850 protocols are introduced in details.

10 Commissioning

Introduce how to commission this relay, check the calibration and test all the function of this relay.

11 Installation

Recommend on unpacking, handling, inspection and storage of this relay. A guide to the mechanical installation and electrical wiring of this relay is also provided, including earthing recommendations. Some typical wiring connection is demonstrated in this manual as well.

12 Maintenance

A general maintenance steps for this device is outlined.

14 Connection Diagrams

List the connection diagram examples including all types of modules.

15 Manual Version History

List the instruction manual versions and their corresponding modification history records.

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1 Briefly Introduction

1.1 Application Scope

The PRS-753 is a numerical line differential and distance protection intended for protecting and monitoring various line arrangement of various voltage level, ranging from 1000kV to 110kV. PRS-753 can detect and clear all types of internal phase-to-phase and phase-to-earth faults locating within the line protection zone.

This relay can sample the analog values from the traditional instrument transformers, or receive the sampled values from the electronic current and voltage transformers (via a merging unit). The binary inputs and outputs of this relay can be configured according to the demands of a practical engineering through the PRS IED Studio configuration tool auxiliary software, which can meet some special requirements of protection and control functions.

This relay can fully support the IEC61850 communication protocol and GOOSE function, and can completely meet the demands of a modern digitalized substation.

1.2 Product Function

Table 1.2-1 Functions included in the IEDs

Description	IEC 60617	ANSI	CYG Code
Line Differential Protection	3dI>L	87	87L
Mho distance protection	Z<	21	21M
Quadrilateral distance protection,	Z<	21	21Q
Power Swing Blocking Releasing	ZPSBR	68	PSBR
Out-of-Step Protection	ϕ <	78	78O
Scheme communication logic for distance protection	-	CL	85
Scheme communication logic for directional earth fault protection	-	CLN	85N
Three Phase Directional Overcurrent Protection	3I> ->	67P	67P(50/51P)
Directional Earth Fault Overcurrent Protection	Io>->	67N	67N(50/51N)
Directional Negative-sequence Overcurrent Protection	I2>	67I2	67I2
Breaker Failure Protection	3I>/I0>BF	50BF	50BF
Thermal Overload Protection	3Ith>	49	49
Stub Differential Protection	3I>STUB	50STB	87STB
Pole Discordance Protection	PD	52PD	52PD
Reverse Power Protection	P>	32R	32R
Broken Conductor Protection	-	46BC	46BC
Three Phase Overvoltage Protection	3U>	59	59P

Description	IEC 60617	ANSI	CYG Code
Residual Overvoltage protection	2(U0>)	59N	59N
Three Phase Undervoltage Protection	3U<	27	27P
OverFrequency Protection	f>	81O	81O
UnderFrequency Protection	f<	81U	81U
Synchrocheck	SYNC	25SYN	25SYN
Automatic Reclosure	O ->I	79	79AR
Faulty Phase Selection	-	21FL	21FL
Trip Logic	-	94	94T
Fault Detector	-	-	FD
Optical Fibre Communication	-	-	FO
Current circuit supervision	-	87	CTS
Fuse failure supervision	FUSEF	60	VTS
CB Position Supervision	CBCM	CBCM	CBCM

1.3 Product Features

- This device is based on a 32-bit high performance dual-core processor, internal high speed bus and intelligent I/O ports, and the hardware is in modularized design and can be configured flexibly, featuring interchangeability and easy extension and maintenance.
- Modularized hardware design makes this relay be easily upgraded or repaired by a qualified service person. Various function optional modules can satisfy various situations according to the different requirements of the users.
- The adoption of 16-bit A/D converter and the dual-channel sampling technology can ensure the accuracy and reliability of protection sampling and the correctness of protection operation. It also provides dedicated current transformers for metering, and ensures the high accuracy of telemetering with 40-point high speed sampling rate per cycle.
- This device can sample the analog values from the traditional instrument transformers, or receive the sampled values from the electronic transformers. It can support the protocol IEC60044-8, IEC61850-9-2 and GOOSE.
- Various algorithms for protection and measurement have been completed in this device for the feature of electronic transformer sampling, such as the error prevention method of multi-algorithms data anomaly for the digital channels, to realize high accuracy and reliability under various conditions of network faults or communication interruption.
- This device has powerful GOOSE functions, and the connection and cooperation between some devices can be realized without using electrical cables, to facilitate the realization of such functions as simple bus differential protection, overload interlock shedding function and backup automatic transfer function etc.
- This device has fully realized the technology to integrate six functions into one device: protection, measurement, control, remote signaling, merging unit function and remote module

functions, to improve the reliability.

- Various methods of GPS time synchronization are supported in this relay, including SNTP, IEEE 1588, pulse per second (PPS) and IRIG-B synchronization.
- The protection modules are completely separated from other modules, and are independent in both hardware and software. The protection functions do not depend on the communication network, so the failure of communication network will not affect the normal operation of the protection functions.
- Mature protection configuration, fast speed and high security performance can meet the practical requirements. Each protective element is independent, so it is very convenient for whether adopting the selected protective element.
- This device constantly measures and calculates a large amount of analog quantities, such as phase voltage, phase-to-phase voltage, neutral voltage, phase current, neutral current, active power, reactive power, power factor and frequency etc.
- The human machine interface (HMI) with a small control module (a 240×128-dot LCD, a 9-key keypad and 21 LED indicators) on the front panel is very friendly and convenient to the user.
- This device can communicate with a SAS or RTU via different communication intermediates: Ethernet network, RS-485 serial ports. The communication protocol of this device is optional: IEC61850, IEC60870-5-103, DNP3.0.
- This device can detect the tripping circuit of the circuit breaker and monitor the operation (close or trip) time of a circuit breaker by checking the auxiliary contacts of the circuit breaker.
- Complete event recording function is provided: 512 latest fault reports, 512 latest warning records, 128 latest user operation records and 2000 latest records of time tagged sequence of event (SOE) can be recorded.
- Powerful fault and disturbance recording function is supported: 16 latest fault disturbance waves, 16 latest start disturbance waves and 4 manual disturbance waves, the duration of a wave recording is configurable.

2 Technical Specifications

2.1 Electrical Specifications

2.1.1 Current Transformer Ratings

Reference		IEC 60255-1, IEC 60255-27
Rated frequency (fn)		50Hz, 60Hz
Nominal range		fn ± 5Hz
Rated current (In)		1A and 5A adaptive (settable)
Thermal withstand capability	continuously	3×In
	for 10s	20×In
	for 1s	100×In
Burden		< 0.05VA/phase @1A, < 0.2VA/phase @5A

2.1.2 Voltage Transformer Ratings

Reference		IEC 60255-1, IEC 60255-27
Rated frequency (fn)		50Hz, 60Hz
Nominal range		fn ± 5Hz
Rated voltage (Un)		100V ~ 120V (phase-to-phase voltage)
Thermal withstand capability	continuously	240V
	10s	360V
	1s	400V
Burden at rated voltage		< 0.03VA/phase @57.7V

2.1.3 Auxiliary Power Supply

Reference	IEC 60255-1, IEC 60255-26	
Rated voltage	24VDC~250VDC, 48V~250VAC	
Variation	80% ~ 120%	
Frequency	50/60Hz, ± 5Hz	
Maximum interruption time in the auxiliary DC voltage without resetting the IED	0%Un,100ms； 40%Un,200ms； 70%Un,500ms At the Un=DC220V	
Gradual shut down / Start up	Class C (60s shut down ramp, 5 min power off, 60s start up ramp)	
Ripple in the DC auxiliary voltage	Class A (15% of rated @200Hz, 220VDC)	
Maximum load of auxiliary voltage supple	1/2 19” Case:	≤20W (normal state), ≤35W (maximum state)
	1/1 19” Case:	≤30W (normal state) ≤40W (maximum state)

2.1.4 Binary Input

Reference	IEC 60255-1, Clause:6.10.5
Binary input number	1/2 19” Case:Up to 72 1/1 19” Case:Up to 108
Rated voltage	24VDC~250VDC
Pickup voltage	55% ~ 70% rated voltage
“ON” value voltage	70% ~ 120% rated voltage
“OFF” value voltage	< 55% rated voltage
Maximum permitted voltage	120% rated voltage
Resolution of binary input signal	≤ 1ms
Resolution of SOE	≤ 1ms

2.1.5 Binary Output

Reference	IEC 60255-1		
Item	Heavy-capacity output	Tripping output	Signal output
Binary output number	1/2 19” Case:Up to 30 1/1 19” Case:Up to 42	1/2 19” Case:Up to 65 1/1 19” Case:Up to 93	1/2 19” Case:Up to 65 1/1 19” Case:Up to 93
Output model	Potential-free contact	Potential-free contact	Potential-free contact
Max system voltage	380Vac, 250Vdc	380Vac, 250Vdc	380Vac, 250Vdc
Voltage across open contact	1000V RMS for 1min	1000V RMS for 1min	1000V RMS for 1min
Continuous carry	10A @ 380Vac； 10A @ 250Vd	10A @ 380Vac； 10A @ 250Vd	5.0A @ 380Vac； 5.0A @ 250Vdc
Short duration current	30A, 3s 50A, 1s	30A, 3s 50A, 1s	30A, 1s
Breaking capacity	1.00A @ 48Vdc, L/R=40ms 0.35A @ 110Vdc, L/R=40ms 0.30A @ 125Vdc, L/R=40ms 0.20A @ 220Vdc, L/R=40ms 0.15A @ 250Vdc, L/R=40ms	1.00A @ 48Vdc, L/R=40ms 0.35A @ 110Vdc, L/R=40ms 0.30A @ 125Vdc, L/R=40ms 0.20A @ 220Vdc, L/R=40ms 0.15A @ 250Vdc, L/R=40ms	0.60A @ 48Vdc, L/R=40ms 0.10A @ 110Vdc, L/R=40ms 0.05A @ 220Vdc, L/R=40ms
Pickup time	< 1ms	< 8ms	< 10ms
Dropout time	< 5ms	< 5ms	< 8ms

2.2 Mechanical Specifications

Mounting Way	Flush mounted
Weight per device	1/2 19” Case: Approx. 8.6kg (fully equipped) 1/1 19” Case: Approx.12.5kg (fully equipped)
Mechanical size (width×high×deepth)	1/2 19” Case: 260mm*266 mm*217.7 mm 1/1 19” Case: 482.6mm*266 mm*217.7 mm
Hole size (width×high)	1/2 19” Case: 227 mm*267 mm 1/1 19” Case: 450 mm*267 mm
Display language	Optional: Chinese, English

Housing material	Metallic plates, parts and screws: Steel Plastic parts: Polycarbonate	
Housing color	Silver grey	
Location of terminal	Rear panel of the device	
Protection class	IEC60225-1: 2009	Front side:IP40 (IP52 with seal strip) Rear side, connection terminals: IP20 Other Sides: IP40

2.3 Ambient Temperature and Humidity Range

Standard	IEC 60255-1:2009
Operating temperature range	-40°C ~ +70°C
Transport and storage temperature range	-40°C ~ +70°C
Damp heat steady	+40℃ 93%humidity 16h
Damp-heat test, cyclic	6 cycles, +25℃ to +55℃, Humidity 97% to 93%

2.4 Communication Interfaces

2.4.1 Ethernet Port

For Station Level			
Medium		**Parameters**	
Ethernet: Electrical OR Optical	Electrical	Port number	3
		Connector type	RJ-45
		Transmission rate	100Mbits/s
		Transmission standard	100Base-TX
		Transmission distance	≤ 100m
		Protocol	IEC60870-5-103:1997, IEC61850 etc.
		Safety level	Isolation to ELV level
	Optical	Port number	3
		Connector type	LC
		Transmission rate	100Mbits/s
		Transmission standard	100Base-FX
		Optical fiber type	Multi-mode
		Wavelength	1310nm
		Transmission distance	≤ 2000m
		Protocol	IEC60870-5-103:1997, IEC61850 etc.
For Process Level (If required)			
Medium		**Parameters**	
Optical		Port number	4
		Connector type	LC
		Transmission rate	100Mbits/s
		Transmission standard	100Base-FX
		Optical fiber type	Multi-mode

	Wavelength	1310nm
	Transmission distance	≤ 2000m

2.4.2 Serial Port

Medium	Parameters	
RS-485 (EIA)	Port number	2
	Baud rate	4800 ~ 115200bps
	Transmission distance	≤ 500m @ 4800bps
	Maximal capacity	32
	Protocol	IEC60870-5-103:1997, DNP3.0 etc.
	Safety level	Isolation to ELV level

2.4.3 Time Synchronization

Medium	Parameters	
RS-485 (EIA)	Port number	1
	Transmission distance	≤ 500m
	Maximal capacity	32
	Timing standard	IRIG-B
	Safety level	Isolation to ELV level
Optical Ethernet	Port number	1
	Connector type	ST
	Transmission distance	≤ 2000m
	Timing standard	IRIG-B
IEEE 1588	Accuracy	≤ 1ms

2.4.4 Ethernet Port for Debugging

Medium	Parameters	
Electrical Ethernet (in front panel)	Port number	1
	Connector type	RJ-45
	Transmission rate	100Mbits/s
	Transmission standard	100Base-TX
	Transmission distance	≤ 100m
	Safety level	Isolation to ELV level

2.5 Type Tests

2.5.1 Environmental Tests

Dry heat operation test	IEC 60068-2-2, IEC 60255-27	16h, +70℃
Cold operation test	IEC 60068-2-1, IEC 60255-27	16h, -40℃
Dry heat storage test	IEC 60068-2-2, IEC 60255-27	16h , +70℃

Cold storage test	IEC 60068-2-1, IEC 60255-27	16h , -40℃
Damp heat steady state test +Verifcation of function & dielectric (10 days）	IEC60255-27, Clause10.5.1.5 IEC 60255-1, Clause 6.12.3.6 IEC 60068-2-78	+40℃ 93%humidity
Damp-heat test, cyclic	IEC 60068-2-30, IEC 60255-27	6 cycles, +25℃ to +40℃, Humidity 97% to 93%
Change of temperature test	IEC 60068-2-14	5 Cycles , 1℃/min, -40℃ to +70℃

2.5.2 Mechanical Tests

Vibration response test	IEC 60255-21-1, IEC 60255-27	Class 1： Vibration Response: Class 1 (10-59Hz: 0.035mm, 59-150Hz: 0.5gn)
Vibration Endurance:	IEC 60255-21-1, IEC 60255-27	Class 1 (10-150Hz: 1gn)
Shock Response	IEC 60255-21-2, IEC 60255-27	Class 1 (5gn)
Shock Withstands	IEC 60255-21-2, IEC 60255-27	Class 1 (15gn)
Bump	IEC 60255-21-2, IEC 60255-27	Class 1(10gn)
Seismic +Verifcation of function	IEC 60255-21-3 IEC 60255-1, Clause 6.13.3	Class I

2.5.3 Electrical Tests

Impulse Voltage Tests.	IEC 60255-27	Impulse test: 5kV (rated insulation voltage ≤ 63V);Impulse test: 1kV (rated insulation voltage ＞ 63V);
AC or DC Dielectric Test	IEC 60255-27	dielectric 50,60Hz 5/60s DC 2.8KV AC 2KV
Insulation Resistance	IEC 60255-27	>100Mohm @500Vdc
Protective Bonding Resistance	IEC 60255-27	Test current DC20A, >12 Vac /Vdc, >60s,< 0.1 ohm

2.5.4 Electromagnetic Compatibility

Burst Disturbance Test / Damped Oscillatory Wave Immunity Test	IEC 60255-26, IEC 61000-4-18	For Power Supply, Binary Input / Output:Common Mode: 2.5kV, Differential Mode: 1kV;For Communication Port:Common Mode: 1kV
Electrostatic Discharge test	IEC 60255-26, IEC 61000-4-2	Contact Discharge: 8kV, Air Discharge: 15kV
Fast Transient test	IEC 60255-26, IEC 61000-4-4	(Power / Earth Port: 4kV, Signal / Control Port: 2kV)
Surge Immunity Test	IEC 60255-26, IEC 61000-4-5	For Power Supply, Binary Input / Output: L-E: 4kV, L-L: 2kV, voltage waveform: 1.2/50μs, current waveform: 8/20μs；Communication Port: L-E: 1kV, L-L: -, voltage waveform: 1.2/50μs, current waveform: 8/20μs)
Conducted radio interference test	IEC 60255-26, IEC 61000-4-6	150kHz~80MHz(Uo: 140dB μV or Uo: 10V)
Electromagnetic fields immunity	IEC 60255-26, IEC 61000-4-3	Test Field Strength: 10V/m , Sweep frequency: 80MHz – 1000MHz, Spot frequency: 80MHz, 160MHz, 450MHz, 900MHz @ 80% Modulation & Pulse
immunity to conduct, common mode disturbance in frequency range 0 Hz to 150KHz	61000-4-16	Level 4：continuous 30V,short duration 300V at 50/3,50,60Hz; 15Hz~150Hz:30-3 decreases at 20dB/decade; 150Hz~1.5kHz:3 constant; 1.5kHz~15kHz:3-30 increases at 20dB/decade; 15kHz~150kHz:30 constant
Power frequency magnetic fields	IEC 61000-4-8, IEC 60255-26	Continuous: 100A/m, Short Duration 1s to 3s: 1000A/m)
Pulse magnetic field immunity test	IEC 61000-4-9	Class 5: Current 6.4/16μs, 1000A/m
Damped oscillatory magnetic field immunity test	IEC 61000-4-10	Class 5: 0.1MHz&1MHz, 100A/m
Power frequency immunity tests	IEC 60255-26	Input: Class A,Common Mode: 300V, Differential Mode: 150V

Ring wave immunity test	IEC 61000-4-12	Ring Wave Class 4,4kV
Conducted RF interference on power supply terminals	IEC 60255-26, CISPR 22	Conducted Emission Limit for Auxiliary Power Supply Port： Frequency range: 0.15MHz – 0.5MHz (Quasi Peak: 79μV, Avg: 66μV), Frequency range: 0.5MHz – 30MHz (Quasi Peak: 73μV, Avg: 60μV)；
Radiated interference	IEC 60255-26, CISPR 22	Radiated Emission Limit on Enclosure Port： Frequency range: 30MHz - 230MHz (Quasi Peak: 40μV), Frequency range: 230MHz - 1000MHz (Quasi Peak: 47μV)

2.6 Terminals

Connection Type	Wire Size
CT and VT circuit connectors	Screw terminals,4mm^2 lead
Binary I/O connection system	Screw terminals, 2.5mm^2 lead

2.7 Measurement Range and Accuracy

Metering Item	Range	Accuracy
Phase range	0° ~ 360°	≤ 0.5% or ±1°
Frequency	35.00Hz ~ 70.00Hz	≤ 0.01Hz
Current (three phase 3Ip)	0.05In<I<4.00In	±0.5%In, 0.05In~1.00In ±0.5%I, 1.00In~4.00In
Voltage (Phase 3Up, Phase-to-Phase 3Upp)	0.05Un<U<1.50Un	±0.5%Un, 0.05Un~1.00Un; ±0.5%U, 1.00Un~1.50Un

2.8 Protective Functions

2.8.1 Fault Detector

2.8.1.1 Superimposed Current Element

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater

2.8.1.2 Residual Current Element

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater

2.8.2 Line Differential Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater

Time delay accuracy	≤ 25ms (at 4 times current setting)

2.8.3 Distance Protection

Accuracy	≤ 2.5% Setting or 0.1Ω/In, whichever is greater
Time delay accuracy	≤ 1% Setting+25ms

2.8.4 Three Phase Directional Overcurrent Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 2 times current setting)
Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (start value multiples in range of 1.2…20 when I> In) ≤ 5.0% of operating time or 40ms, whichever is greater (start value multiples in range of 2…20 when I≤ In)

2.8.5 Directional Earth Fault Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 2 times current setting)
Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (start value multiples in range of 1.2…20 when I> In) ≤ 5.0% of operating time or 40ms, whichever is greater (start value multiples in range of 2…20 when I≤ In)

2.8.6 Directional Negative-sequence Overcurrent Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 2 times current setting)
Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (start value multiples in range of 1.2…20 when I> In) ≤ 5.0% of operating time or 40ms, whichever is greater (start value multiples in range of 2…20 when I≤ In)

2.8.7 Breaker Failure Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Time delay accuracy	≤ 1% Setting+20ms (at 2 times current setting)
Drop-off time	≤ 12.5ms

2.8.8 Thermal Overload Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy	≤ 2.5% of operating time or 30ms, whichever is greater (start value multiples in range of 1.2…20 when I> In) ≤ 5.0% of operating time or 40ms, whichever is greater (start value multiples in range of 2…20 when I≤ In)

2.8.9 Stub Differential Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy	≤ 1% Setting+30ms (at 2 times current setting)

2.8.10 Pole Discordance Protection

Accuracy	≤ 2.5% Setting or 0.02In, whichever is greater
Resetting ratio	97%
Time delay accuracy	≤ 1% Setting+30ms (at 2 times current setting)

2.8.11 Reverse Power Protection

Accuracy	≤ 2.5% Setting or 0.5W, whichever is greater
Resetting ratio	97%
Time delay accuracy	≤ 1% Setting+30ms

2.8.12 Broken Conductor Protection

Accuracy	≤ 2.5% Setting
Resetting ratio	97%
Time delay accuracy	≤ 1% Setting+30ms

2.8.13 Three Phase Overvoltage Protection

Accuracy	≤ 2.5% Setting or 0.01Un, whichever is greater
Resetting ratio	98%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 1.2 times voltage setting)
Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (for voltage between 1.2 and 2 multiples of pickup)

2.8.14 Residual Overvoltage Protection

Accuracy	≤ 2.5% Setting or 0.01Un, whichever is greater
Resetting ratio	98%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 1.2 times voltage setting)

Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (for voltage between 1.2 and 2 multiples of pickup)

2.8.15 Three Phase Undervoltage Protection

Accuracy	≤ 2.5% Setting or 0.01Un, whichever is greater
Resetting ratio	102%
Time delay accuracy (definite-time characteristic)	≤ 1% Setting+30ms (at 0.8 times voltage setting)
Time delay accuracy (inverse-time characteristic)	≤ 2.5% of operating time or 30ms, whichever is greater (for voltage between 0.5 and 0.8 multiples of pickup)

2.8.16 Overfrequency Protection

Accuracy	≤ 0.02Hz
Time delay accuracy	≤1% Setting+30ms (at 1.2 times frequency setting)

2.8.17 Underfrequency Protection

Accuracy	≤ 0.02Hz
Time delay accuracy	≤1% Setting+30ms (at 0.8 times frequency setting)

2.8.18 Auto-reclosing

Phase accuracy	3.0Deg
Voltage accuracy	≤ 2.5% Setting or 0.01Un, whichever is greater
Frequency accuracy	0.01Hz
Time delay accuracy	≤ 1% Setting+20ms

2.8.19 Transient Overreach

Tolerance for all high-speed protection	≤ 2%

2.8.20 Fault Locator

Accuracy for multi-phase faults with single end feed	3%
Tolerance will be higher in case of single-phase fault with high ground resistance.	

3 Protection Functions

3.1 Overview

The PRS-753 relay is a microprocessor based relay which can provide mature protection for various primary equipment (such as overhead line, underground cable etc). The following sections detail the individual protection functions of this relay.

The glossary will be listed in the below form.

Category	Profession Vocabulary	Abbreviation
Electricity	Time	T
	Phase	Ph
	Direction	Dir
	Overcurrent	OC
	Curve	Curve
	Temperature	Temp
	Characteristic	Char
	Polarity	Pol
	Quantity	Qua
	Factor	Factor
	Current	Cur
	Residual Current	ResCur
	Negative Current	NegCur
	Positive Current	PosCur
	Voltage	Vol
	Residual Voltage	ResVol
	Negative Voltage	NegVol
	Positive Voltage	PosVol
	High Voltage	HigVol
	Low Voltage	LowVol
	thermal	Therm
	Overload	OL
	Negative	Neg
	Sequence	Seq
	Residual	Res
	Beta	Beta
	harmonic	Harm
	Power	Pow
	Earth-fault	EF
	Failure	Fail
	Impedence	Imp
	Reactance	React

Category	Profession Vocabulary	Abbreviation
	Induction	Induct
	Positive	Posi
Operation	Block	Blk
	Enable	Ena
	Operation	Op
	Trip	Tr
	Protection	Prot
	Mode	Mod
	Forward	Fwd
	Reverse	Rev
	Constant	Const
	External	Ex
	Internal	In
	Number	Num
	Selector	Sel
	Measurement	Meas
	Parameter	Para
	Multiplier	Mult
	Minimum	Min
	Alarm	Alm
	Reclose	Recls
	Counter	Counter
	Correction	Correction
	Available	Avai
	Initial	Init
	Reference	Ref
	Normal	Norm
	Restraint	Restr
	Slope	Slope
	deblock	Deblk
	Winding	Wnd
	Elimination	Elim
	Nominal	Nom
	Connection	Connection
	Hysteresis	Hyst
	Compensation	Comp
	Check	Chk
	Synchronize	Syn
	Synchronization	Syn
	Energize	Energ
	Weigh	Weig
	Activation / Activate	Activ

Category	Profession Vocabulary	Abbreviation
	Error	Err
	Configuration	Cfg
	Parameter	Para
	Management	Mana
	Interrupt	Intr
	SelfCheck	SelfChk
	Start	Str
Apparatus	Generator	Gen
	Motor	Motor
	Rotor	Rotor
	Stator	Stator
	Busbar	Bus
	Transformer	TF
	Transmission Line	TL
	Line	Line
	Capacitor	Cap
	Reactor	Reac
	Resistor	Resis
	Switch	Sw
	Component	Comp

3.2 System Parameters

3.2.1 Overview

To correct configuration of analog input channels, other protected system information, such as the parameters of voltage transformer and current transformer are also required.

3.2.2 Settings

Table 3.2-1 System parameters

NO	Name	Range	Unit	Step	Default	Description
1	Prot_TA_Primary	1~9999	A	1	1000	Primary rated current of CT
2	Prot_TA_Secondary	1 or 5	A	4	1	Secondary rated current of CT
3	Prot_TV_Primary	1~2000	KV	0.01	220	Primary rated voltage of VT
4	Prot_TV_Secondary	1~1000	V	0.01	100	Secondary rated voltage of VT
5	CT_Group	1 or 2	-	1	1	CT group input number

3.3 Line Parameters

3.3.1 Overview

When the device equips with line protection functions, line parameters of protected line are required, especially for fault location, precise line parameters are the basic criterion for accurate fault location.

3.3.2 Settings

Table 3.3-1 Line parameters

NO	Name	Range	Unit	Step	Default	Description
1	Z1L	(0.05~655)/In	ohm	0.01	10	Positive-sequence impedance of the whole line (secondary value)
2	LinAng	10~89	deg	0.01	85	Line positive-sequence impedance angle
3	Z0L	(0.05~655)/In	ohm	0.01	30	Zero-sequence impedance of the whole line (secondary value)
4	LinAng0	30~89	deg	0.01	80	Line zero-sequence impedance angle
5	Line_Kz	0~10.000	-	0.001	0.67	Zero-sequence compensation coefficient magnitude
6	Line_KzAng	0~360.00	deg	0.01	0	Zero-sequence compensation coefficient angle
7	LineLength	0.00~655.00	km	0.01	100	Total length of the whole line

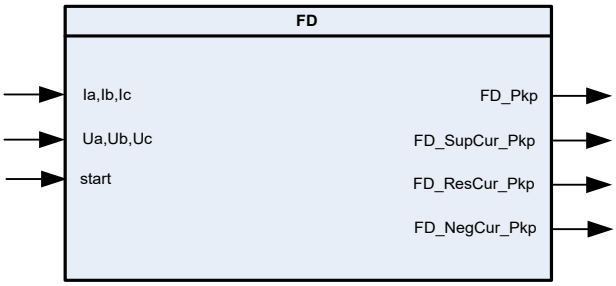
3.4 Fault Detector FD

3.4.1 Overview

The device has DSP module with BCPU (main protection board) and PCPU (backup protection board) both for fault detector and protection calculation. Data acquisition circuits of BCPU and PCPU modules are totally independent.

Fault detector in BCPU and PCPU picks up to provide positive supply to output relays. The output relays can only operate when both the fault detector in BCPU and PCPU operate. Otherwise, the output relays would not operate.

3.4.1.1 Function Block



3.4.1.2 Signals

Table 3.4-1 FD Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	start	Other protection start signal

Table 3.4-2 FD Output Signals

NO.	Signal	Description
1	FD_Pkp	The device picks up
2	FD_SupCur_Pkp	Superimposed current fault detector element operates
3	FD_ResCur_Pkp	Residual current fault detector element operates
4	FD_NegCur_Pkp	Negative-sequence current fault detector element operates

3.4.2 Protection Principle

Main part of FD is superimposed current detector element that detects the change of phase-to-phase power frequency current, and residual current fault detector element that calculates the vector sum of 3 phase currents as supplementary. They are continuously calculating the analog input signals.

All fault detectors in this device include:

1. Fault detector based on superimposed current: superimposed current is greater than the setting value.
2. Fault detector based on residual current: Residual current is greater than the setting value.
3. Fault detector based on negative-sequence current: Negative-sequence current is greater than the setting value.
4. Fault detector based on phase current: Phase current is greater than the setting value.
5. Fault detector based on voltage: Phase voltage is greater than the setting value.

6. Fault detector based on weak infeed logic: Weak infeed logic of current differential protection pickup.
7. Fault detector based on thermal overload logic: thermal overload pickup.
8. Fault detector based on circuit breaker position: Circuit breaker position discordance.
9. Fault detector based on reverse power logic: reverse power pickup.
10. Fault detector based on broken conductor logic: broken conductor pickup.

If any of the above conditions is complied, FD will operate to activate the output circuit providing DC power supply to the output relays. The fault detector based on superimposed current and the fault detector based on residual current are always enabled, and all protection functions are permitted to operate when they operate.

3.4.2.1 Fault Detector Based on Superimposed Current

Superimposed phase current is obtained by subtracting the phase current from that of a cycle before.

$\Delta I = I(k) - I(k - N)$

$I(k)$ is the sampling value at a point.

$I(k - N)$ is the value of a sampling point before a cycle.

Operation criteria:

$\Delta I_{\phi} = 1.25\Delta I_{Th} + \Delta I_{Set}$

Where:

ΔI_{ϕ}: Superimposed phase current (Φ=A, B, C)

ΔI_{Set}: The fixed threshold value (i.e. the setting FD_SupCur_Str)

ΔI_{Th}: The floating threshold value

This element adopts adaptive floating threshold varied with the change of load current continuously. The change of load current is small and steadily under normal or power swing condition, the adaptive floating threshold with the ΔI_{Set} is higher than the change of current under these conditions and hence maintains the element stability.

The coefficient, 1.25, is an empirical value which ensures the threshold always higher than the unbalance output value of the system.

If operation condition is met, the fault detector based on superimposed current will operate to provide DC power supply for output relays, the pickup signal will maintain 7s after the fault detector based on superimposed current drops off.

3.4.2.2 Fault Detector Based on Residual Current

In case of long distance fault or big resistance fault, superimposed current is relative small, so, residual current is used to judge pickup condition.

The operation condition will be met when 3I0 is greater than the setting FD_ResCur_Str. The fault detector based on residual current is always in service.

Where:

3I0: residual current calculates from the vector sum of Ia, Ib and Ic

If operation condition is met, the fault detector based on residual current will operate to provide DC power supply for output relay, and the pickup signal will maintain 7s after the fault detector based on residual current drops off.

3.4.2.3 Fault Detector Based on Negative-sequence Current

The operation condition will be met when I2 is greater than the setting FD_NegCur_Str. It can be enabled or disabled by the logic setting FD_Neg_Ena.

Where:

I2: negative-sequence current calculates from the vector of Ia, Ib and Ic

If operation condition is met, the fault detector based on negative-sequence current will operate to provide DC power supply for output relay, and the pickup signal will maintain 7s after the fault detector based on negative-sequence current drops off.

3.4.2.4 Fault Detector Based on Phase Current

The fault detector based on phase current will operate to provide DC power supply for output relay when phase overcurrent protection is enabled and meets the operation condition, and the pickup signal will maintain 7s after the fault detector based on phase current drops off.

3.4.2.5 Fault Detector Based on Voltage

This fault detector based on voltage includes the fault detectors of overvoltage protection, undervoltage protection and frequency protection. The fault detector based on voltage will operate to provide DC power supply for output relay when corresponding voltage element is enabled and meets the operation condition, and the pickup signal will maintain 7s after the fault detector based on voltage drops off.

3.4.2.6 Fault Detector Based on Weak Infeed Logic

To ensure to reliably start differential protection at the weak infeed side of weak feeders and at the remote fault side of high-impedance-grounded faults, fault detector based on weak infeed is equipped. It has two parts. The first one is that, if there is low voltage at the side and the differential current of the low voltage phase reaches the differential current threshold, the fault detector based on weak infeed will operate; the second one is that, if there is zero-sequence and negative-sequence voltage at the other side and only the differential current of one phase reaches the differential current threshold, the fault detector based on weak infeed will operate. The pickup signal

will maintain 7s after the fault detector based on weak infeed logic drops off.

3.4.2.7 Fault Detector Based on Thermal Overload Logic

The fault detector based on thermal overload logic will operate to provide DC power supply for output relay when tripping logic of thermal overload protection meets the operation condition, and the pickup signal will maintain 7s after the fault detector based on thermal overload logic drops off.

3.4.2.8 Fault Detector Based on Circuit Breaker Position

When pole discordance protection is enabled, i.e. the logic setting [52PD_Ena] is set as “1”, and if three phases of circuit breaker are not in the same status,the fault detector based on circuit breaker position will operate to provide DC power supply for output relay, and the pickup signal will maintain 7s after the fault detector based on circuit breaker position drops off.

3.4.2.9 Fault Detector Based on Reverse Power Logic

The fault detector based on reverse power logic will operate to provide DC power supply for output relay when tripping logic of reverse power protection meets the operation condition, and the pickup signal will maintain 7s after the fault detector based on reverse power logic drops off.

3.4.2.10 Fault Detector Based on Broken Conductor Logic

The fault detector based on broken conductor logic will operate to provide DC power supply for output relay when tripping logic of broken conductor protection meets the operation condition, and the pickup signal will maintain 7s after the fault detector based on broken conductor logic drops off.

3.4.3 Logic

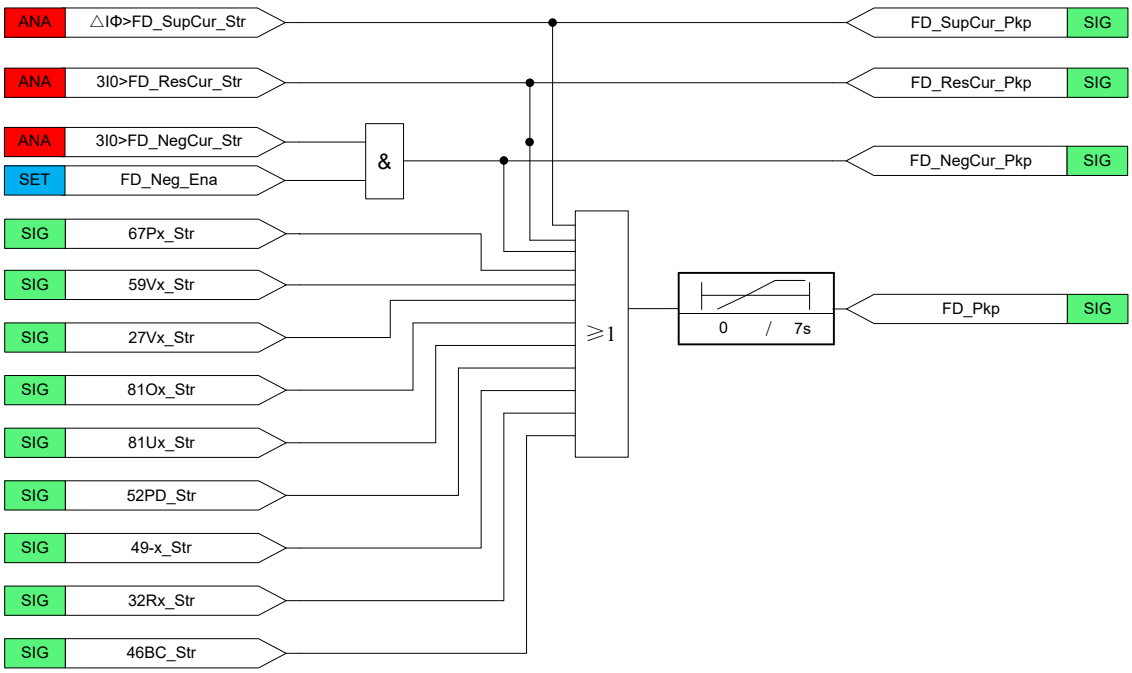


Figure 3.4.1 Logic Diagram for Fault Detector

3.4.4 Settings

Table 3.4-3 Settings of fault detector

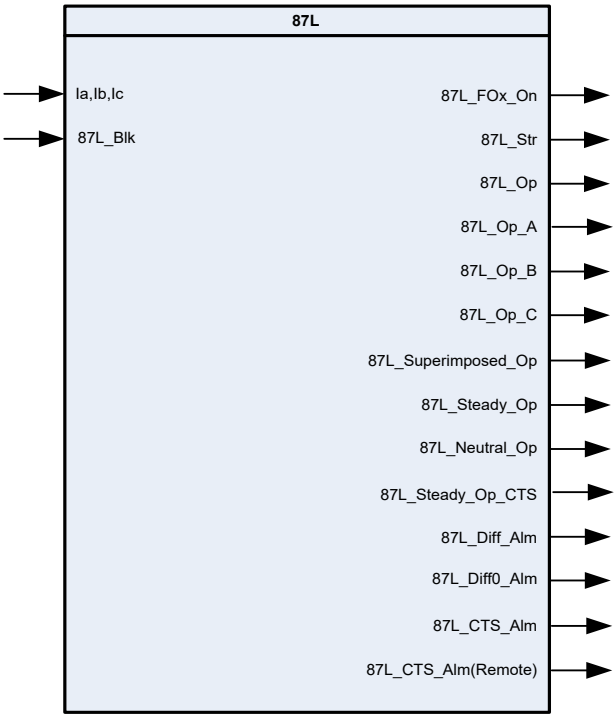
No.	Name	Range	Unit	Step	Default	Description
1	FD_Neg_Ena	0 or 1	-	1	0	Enabling/disabling negative-sequence current fault detector element 0: disable 1: enable
2	FD_SupCur_Str	(0.05~30.00) ×In	A	0.01	0.5	Current setting of superimposed current fault detector element
3	FD_ResCur_Str	(0.05~30.00) ×In	A	0.01	0.5	Current setting of residual current fault detector element
4	FD_NegCur_Str	(0.05~30.00) ×In	A	0.01	0.5	Current setting of negative-sequence current fault detector element

3.5 Line Differential Protection 87L

3.5.1 Overview

Line differential protection can be used as main protection of the protected multi-terminal circuit, consisting of overhead power lines and cables. It offers phase-segregated current differential protection with high sensitivity and provides phase selection information for single-phase tripping.

3.5.1.1 Function Block



3.5.1.2 Signals

Table 3.5-1 87L Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	87L_Blk	Block signal of 87L

Table 3.5-2 87L Output Signals

NO.	Signal	Description
1	87L_FOx_On	Current differential protection is enabled. (corresponding to channel x)
2	87L_Str	Start signal from weak infeed
3	87L_Op	Operation signal from any phase
4	87L_Op_A	Operation signal from phase A
5	87L_Op_B	Operation signal from phase B
6	87L_Op_C	Operation signal from phase C
7	87L_Superimposed_Op	Operation signal from superimposed current differential element

NO.	Signal	Description
8	87L_Steady_Op	Operation signal from steady-state current differential element
9	87L_Neutral_Op	Operation signal from neutral current differential element
10	87L_Steady_Op_CTS	Operation signal from steady-state current differential element when CT circuit fails
11	87L_Diff_Alm	Alm signal from differential current overreach
12	87L_Diff0_Alm	Alm signal from zero sequence differential current overreach
13	87L_CTS_Alm	Alm signal from CT circuit failure
14	87L_CTS_Alm(Remote)	Alm signal from CT circuit failure of remote end

3.5.2 Protection Principle

Line differential protection applies the basis of current comparison (Kirchhoff's current law). For this a device has to be installed at each end of the area to be protected. The devices exchange their measurands via communication channels. Each device performs the current comparison with these measurands and trips the assigned circuit breaker, if there is a short circuit in the protection range.

The communication channel between two devices is monitored and its propagation delay is measured continuously. Once channel failure is detected, the current differential protection will be blocked automatically.

Line differential protection comprises three elements:

- Superimposed current differential element (1 stage)
- Steady-state current differential element(1 stage)
- Neutral current differential element (2 stage)

3.5.2.1 Superimposed Current Differential Element

Operation criteria:

$$\begin{cases} \Delta I_{Diff\,\phi} \geq 0.8 \times \Delta I_{Bias\,\phi} \\ \Delta I_{Diff\,\phi} \geq I_H \end{cases}$$

Where:

$\Delta I_{Diff\,\phi}$: The superimposed differential current($\Delta I_{Diff\,\phi} = \left|\Delta \dot{I}_{M\,\phi} + \Delta \dot{I}_{N\,\phi}\right|$)

$\Delta I_{Bias\,\phi}$: The superimposed restraint current($\Delta I_{Bias\,\phi} = \left|\Delta \dot{I}_{M\,\phi} - \Delta \dot{I}_{N\,\phi}\right|$)

I_H : $\mathrm{Max}(87L\_Cur\_Op,\ I_c,\ \frac{U_N}{X_{C1}} - \frac{U_N}{X_{ML}} - \frac{U_N}{X_{NL}})$

$\Delta\dot{I}_{M\phi}$, $\Delta\dot{I}_{N\phi}$ are the superimposed current at both sides of the protected lines after capacitive current compensation.

87L_Cur_Op is the current setting of current differential protection.

U_N is rated phase voltage.

X_{C1} is the positive-sequence capacitive impedance of the line, set by the setting 87L_X_{C1}.

X_{ML1} is the impedance setting of reactor of local line, set by the setting 87L_X_{ML1}.

X_{NL1} is the impedance setting of reactor of remote line, receive from the remote end via communication channel.

If the charging current compensation function is disabled (the setting 87L_CapCurrComp is set as "0"), I_c, $\frac{U_N}{X_{C1}} - \frac{U_N}{X_{ML}} - \frac{U_N}{X_{NL}}$ is not considered to calculate setting. The regulation is adaptive to other stages of current differential protection.

Superimposed current differential element are put into service only within 2 cycles after fault occurrence.

Operation characteristic curve is shown as following figure.

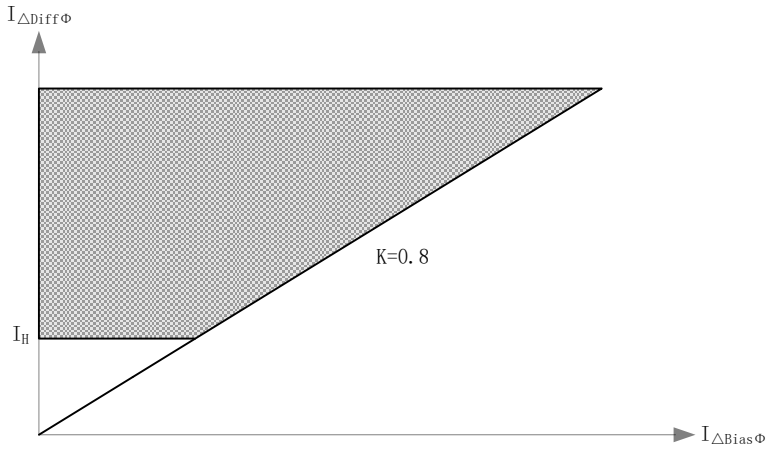


Figure 3.5.1 Operation characteristic of superimposed current differential element

3.5.2.2 Steady-state Current Differential Element

Operation criteria:

$$\begin{cases} I_{Diff\phi} > I_H & \left(I_{Bias\phi} < Knee1\right) \\ I_{Diff\phi} > I_H + K1 * \left(I_{Bias\phi} - Knee1\right) & \left(Knee1 \le I_{Bias\phi} < Knee2\right) \\ I_{Diff\phi} > I_H + K1 * (Knee2 - Knee1) + K2 * \left(I_{Bias\phi} - Knee2\right) & \left(I_{Bias\phi} > Knee2\right) \end{cases}$$

Where:

$I_{Diff\phi}$: The phase differential current($I_{Diff\phi} = \left|\dot{I}_{M\phi} + \dot{I}_{N\phi}\right|$)

$I_{Bias\phi}$: The phase restraint current($I_{Bias\phi} = \left|\dot{I}_{M\phi} - \dot{I}_{N\phi}\right|$)

I_H : $Max(87L\_Cur\_Op,\ I_c,\ \frac{U_N}{X_{C1}} - \frac{U_N}{X_{ML}} - \frac{U_N}{X_{NL}})$

$\dot{I}_{M\phi}$, $\dot{I}_{N\phi}$ are the current at both sides of the protected lines after capacitive current compensation.

"Knee1" and "Knee2" are respectively current settings of knee point 1 and knee point 2, the corresponding set value: 87L_Cur_K1 and 87L_Cur_K2)

"K1" and "K2" are two slopes of current differential protection, the corresponding set value: 87L_Slope1, 87L_Slope2.

Operation characteristic curve is shown as following figure.

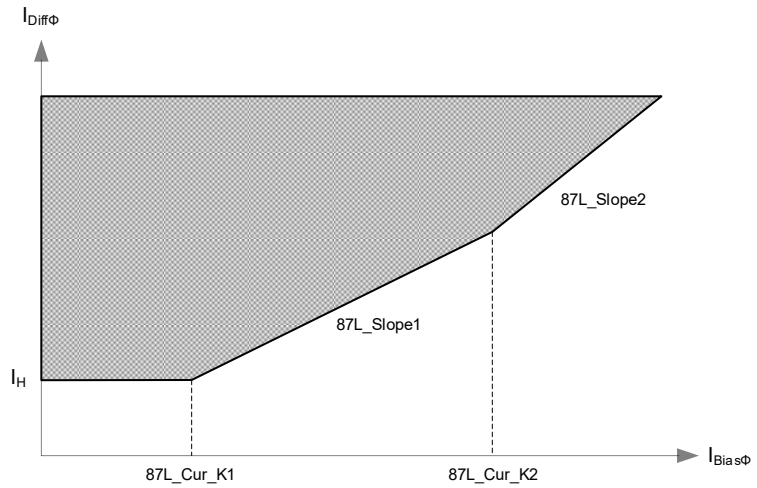


Figure 3.5.2 Operation characteristic of steady-state current differential element

3.5.2.3 Neutral Current Differential Element

Operation criteria:

$$\begin{cases} I_{Diff0} > 0.6 \times I_{Bias0} \\ I_{Diff0} > I_L \\ I_{Diff\phi} > 0.12 \times I_{Bias\phi} \\ I_{Diff\phi} > I_L \end{cases}$$

Where:

I_{Diff0}: The neutral differential current($I_{Diff0} = \left|\dot{I}_{M0} + \dot{I}_{N0}\right|$)

I_{Bias0}: The neutral restraint current($I_{Bias0} = \left|\dot{I}_{M0} - \dot{I}_{N0}\right|$)

$I_{Diff\phi}$ is the same to those mentioned above

$I_{Bias\phi}$ is the same to those mentioned above

I_L : 87L_Cur_Op_Neutral

$\dot{I}_{M0}$, $\dot{I}_{N0}$ are the neutral current at both sides of the protected lines.

Operation characteristic curve is shown as following figure.

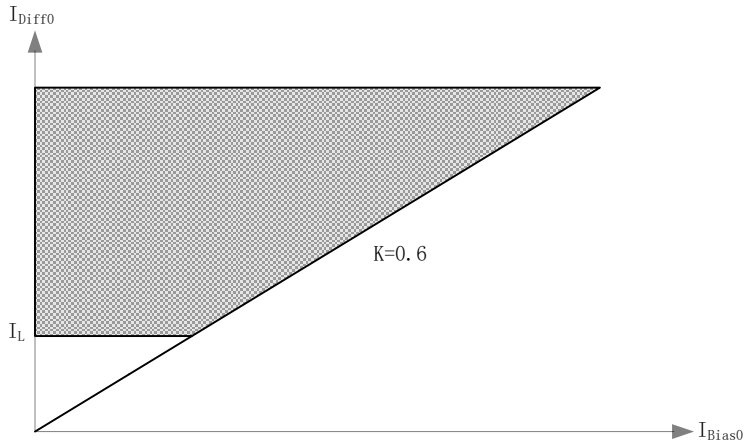


Figure 3.5.3 Operation characteristic of Neutral current differential element

Adopting neutral current differential element is mainly to reflect high-impedance-grounded faults under heavy load. As fault component, neutral current boasts high sensitivity.

The criterion is defined by 87L_T_Neutral delay phase selection action (neutral differential phase selection is based on selecting the phase with maximum differential current as the fault phase after neutral differential action) to avoid impacts from asynchronous three-phase switching-on and CT transient state process. Delay three phases trip after 87L_T_Neutral+150ms.

The device's neutral differential acts only when the superimposed and steady-state current differential fails to act.

When the percentage of second and third harmonic component to fundamental component of neutral differential current is greater than 15, the neutral current differential element will be blocked by harmonic, which can avoid the neutral differential current caused by the inconsistent CT characteristics of the empty charging transformer.

If second and third harmonic component of neutral differential current is lower than the minimum operating current (0.05In) then harmonic calculation is not carried out and harmonic blocking element does not operate.

Operation criteria:

$$\begin{cases} I_{Diff0\_2nd} + I_{Diff0\_3rd} > 0.15 * I_{Diff0} \\ I_{Diff0\_2nd} + I_{Diff0\_3rd} > 0.05In \end{cases}$$

Where:

I_{Diff0} is the same to those mentioned above

I_{Diff0_2nd} : The second harmonic component of neutral differential current($I_{Diff0\_2nd} = |\dot{I}_{M0\_2nd} + \dot{I}_{N0\_2nd}|$)

I_{Diff0_3rd} : The third harmonic component of neutral differential current($I_{Diff0\_3rd} = |\dot{I}_{M0\_3rd} + \dot{I}_{N0\_3rd}|$)

3.5.2.4 Capacitive Current Compensation

For the long transmission line whose capacitive current is very large, in order to increase the sensitivity of current differential element especially for an earth fault associated with high fault resistance, capacitive current must be compensated to eliminate the effect that capacitive current has on differential current.

1. For long transmission line without shunt reactor

The mode for capacitive current compensation adopted by the device is only to make compensation for the current input into the differential comparator at the side and make no compensation for the current transmitted through the channel to the other side, or say, to only deduct the current $\dot{I}_c$ produced by distributed capacitance in differential calculation. For the protection equipment of both sides, the calculation formulas of differential current are as follows:

$$\begin{cases} \text{Mside} & I_{Diff\phi} = \left|\dot{I}_{M\phi} + \dot{I}_{N\phi} - \dot{I}_{M\phi,c}\right| \\ \text{Nside} & I_{Diff\phi} = \left|\dot{I}_{M\phi} + \dot{I}_{N\phi} - \dot{I}_{N\phi,c}\right| \end{cases}$$

Where, $\dot{I}_{M\phi}$ and $\dot{I}_{N\phi}$ are the calculated current compensation of both sides. Taking an example of $\dot{I}_{M\phi}$, the calculation formula is shown in the following euqation:

$$\dot{I}_{M\phi,c} = \left(\frac{\dot{U}_{M\phi} - \dot{U}_{M0}}{2X_{C1}} + \frac{\dot{U}_{M0}}{2X_{C0}}\right) + \left(\frac{\dot{U}_{N\phi} - \dot{U}_{N0}}{2X_{C1}} + \frac{\dot{U}_{N0}}{2X_{C0}}\right)$$

Where:

$\dot{U}_{M\phi}$ and $\dot{U}_{N\phi}$ are the phase voltage at both sides of the protected lines.

$\dot{U}_{M0}$ and $\dot{U}_{N0}$ are the zero sequence voltage at both sides of the protected lines.

X_{C1} is the positive-sequence capacitive impedance of the line, set by the setting 87L_X_{C1}.

X_{C0} is the zero-sequence capacitive impedance of the line, set by the setting 87L_X_{C0}.

In case of single-end supply and unloaded switching to the line, this compensation mode is more suitable than separate full-compensation or half-compensation. Compensation eliminates the impact of steady capacitive current.

2. For long transmission line with shunt reactor

Because a part of capacitive current has been compensated by shunt reactor, reactive current $\dot{I}_L$ must be subtracted from capacitive current calculated by above equation, i.e. Equation 3.2-5.

The calculation formula of reactive current is shown in the following equation:

$$\dot{I}_{M\phi,L} = \frac{\dot{U}_{M\phi} - \dot{U}_{M0}}{X_{ML1}} + \frac{\dot{U}_{M0}}{X_{ML1}+3X_{ML0}}$$

Where:

X_{ML1} is the impedance setting of reactor of local line, set by the setting 87L_X_{ML1}.

X_{ML0} is the impedance setting of ground reactor of local line, set by the setting 87L_X_{ML0}.

Then,

$$\dot{I}_{M\phi,c} = \left(\frac{\dot{U}_{M\phi} - \dot{U}_{M0}}{2X_{C1}} + \frac{\dot{U}_{M0}}{2X_{C0}}\right) + \left(\frac{\dot{U}_{N\phi} - \dot{U}_{N0}}{2X_{C1}} + \frac{\dot{U}_{N0}}{2X_{C0}}\right) - \dot{I}_{M\phi,L}$$

3. For short transmission line

Capacitive current is very small, the sensitivity of current differential protection can still meet the requirement without capacitive current compensation. The capacitive current compensation is disabled when the logic setting 87L.CapCurrComp is set as “0”.

3.5.2.5 CT Circuit Failure

The criterion of CT circuit failure is as follows (take phase A for example):

$$\begin{cases} 3I_{M0} > (0.1I_N, \text{FD\_ResCur\_Str})_{min} \\ 3I_{N0} < (0.1I_N, \text{FD\_ResCur\_Str})_{min} \\ FD.Op_N = 0 \\ I_{DiffA} > (0.1I_N, \text{FD\_ResCur\_Str})_{min} \end{cases}$$

Where:

FD_ResCur_Str is the current setting of residual current fault detector element.

$FD.Op_N$ is the non-started sign of the remote side.

I_{DiffA} is the differential current.

$3I_{M0}$,$3I_{N0}$ are the neutral current at both sides of the protected lines.

If Equation is met, in case of a 12s delay, the device will determine it as CT circuit failure, and send 87L_CTS_Alm alarm signals. After CT circuit failure alarm signals, the device will block superimposed current differential protection and neutral current differential protection.

The steady-state current differential protection will show two kinds of behavior during CT circuit failure:

If logic setting 87L_CTS_Blk (differential protection being blocked during CT circuit failure) is set as “1”, the steady-state current differential protection of CT circuit failure phase will be blocked.

If logic setting 87L_CTS_Blk is set as “0” and the current differential current of the faulty phase is

more than the differential current setting 87L_Cur_CTS during CT circuit failure, the current differential protection will operate with alarm signal being issued at the same time.

CT circuit failure signals of the opposite side will be sent to this side by digital channels, and the device at this side will, after 1s delay confirmation, send 87L_CTS_Alm(Remote) alarm signals and carry out the same logic processing as this side's CT circuit failure.

If CT circuit fails, current differential protection adjusts its time delay to 25ms, trip three-phase circuit breaker and block auto-reclosing.

3.5.2.6 CT Saturation Detection and Blocking

The characteristics of instantaneous action make differential protection suffer more impacts of short circuit transient process. Larger restraint coefficients will reduce protection sensitivity. Considering the randomness of CT saturation, the detection algorithm for CT saturation due to external faults is added in the criterion, so as not to reduce protection sensitivity in case of internal fault and overcome adverse impact of CT saturation.

Due to the existence of CT linear transmission area, CT is unsaturated in the very short period of time when short circuit happens. Thus, for serious faults outside the area, there exists clear timer difference between the moment when differential current occurs and the moment when faults appear; for faults inside the area, they are basically the same. Therefore, detecting time difference can judge CT saturation.

Upon detecting CT saturation, the device will block differential protection. Meanwhile, considering that faults may spread into the area after saturation, application of waveform recognition technology can activate protect fast so as to make correct action for the faults shifting from the outside to the inside of the area.

3.5.2.7 Opposite-side CT Transformation Ratio Regulation Coefficient

The device can itself adapt to different CT transformation ratios at both sides. The primary value of CT transformation ration at the opposite side is obtained from communication. The software will automatically convert the current of the opposite side into the value when the CT transformation ratio at this side occurs. The value seen in the device's interface is that converted from the current of the opposite side when the transformation ratio at this side occurs.

3.5.2.8 Differential Current Overreach Alarm

To prevent faults in the device's AC input and data acquisition system, when the time that the differential current of one phase in the three takes to exceed 0.75-times 87L_Cur_Op is above the time setting 87L_T_DiffAlm, the device will send 87L_DIFF_Alm alarm signals. Similarly, the neutral differential protection is equipped with zero sequence differential current overreach alarm element. When the time that the zero-sequence differential current takes to exceed 0.75- times 87L_Cur_Op_Neutral is above the time setting 87L_T_DiffAlm, the device will send 87L_DIFF0_Alm alarm signals. Differential current overreach alarm elements have no impact on differential protection.

3.5.3 Logic

3.5.3.1 Common Element

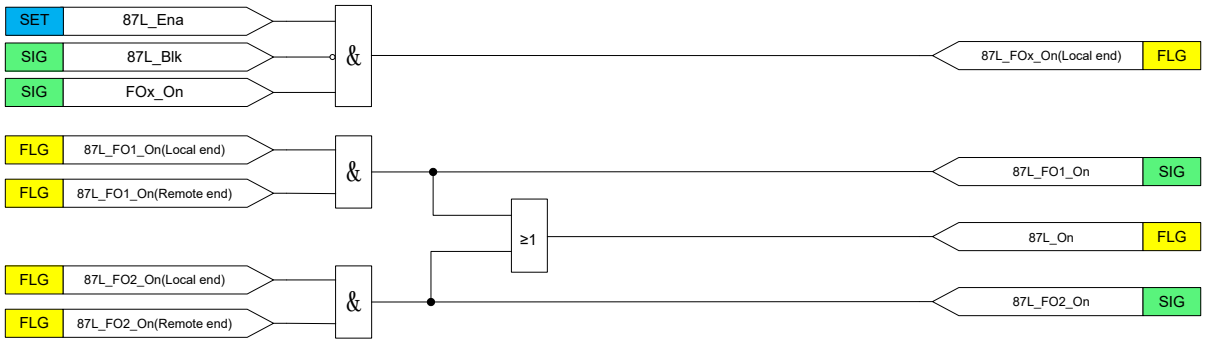


Figure 3.5.4 Enabling/disabling logic of 87L

Where:

87L_FOx_On(Remote end): remote current differential protection is enabled corresponding to channel x

3.5.3.2 Superimposed Current Differential Element

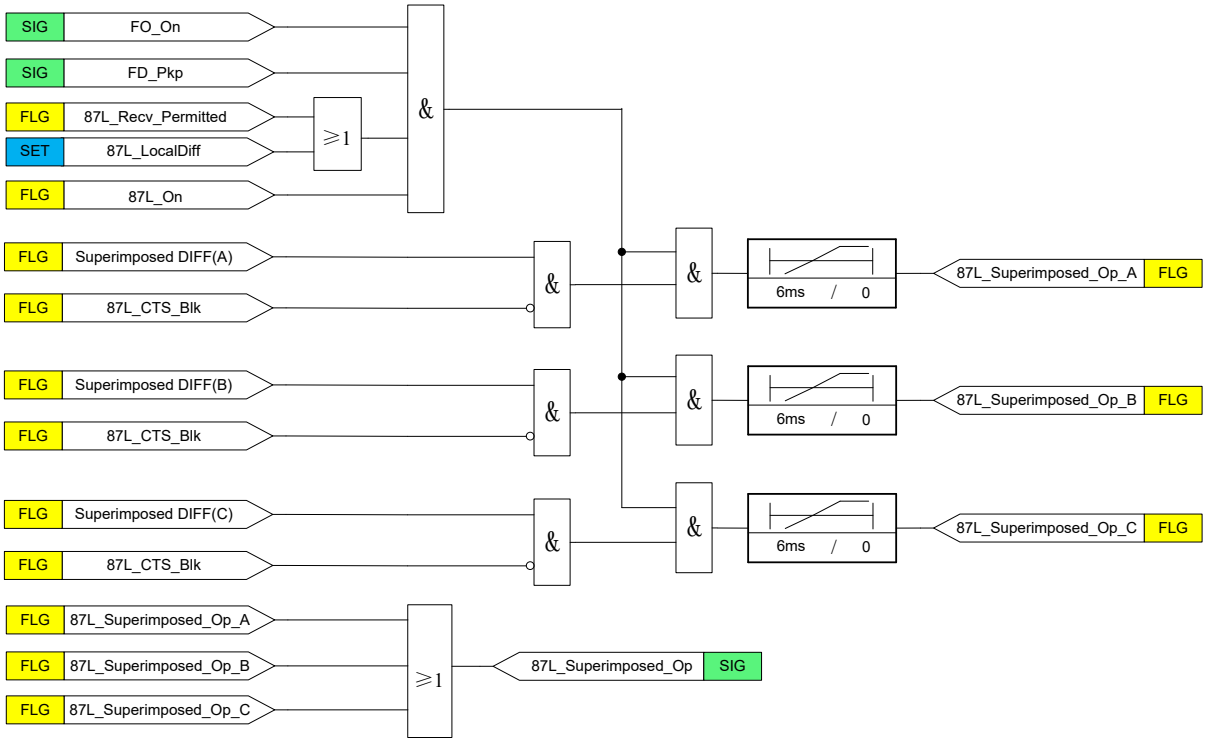


Figure 3.5.5 Superimposed current differential element of 87L

Where:

Superimposed DIFF(A): superimposed current differential element for phase A

Superimposed DIFF(B): superimposed current differential element for phase B

Superimposed DIFF(C): superimposed current differential element for phase C

87L_Recv_Permitted: current differential protection permissive signal that received from the remote end via communication channel. Please refer to section about the conditions to send permissive signal.

3.5.3.3 Steady-state Current Differential Element

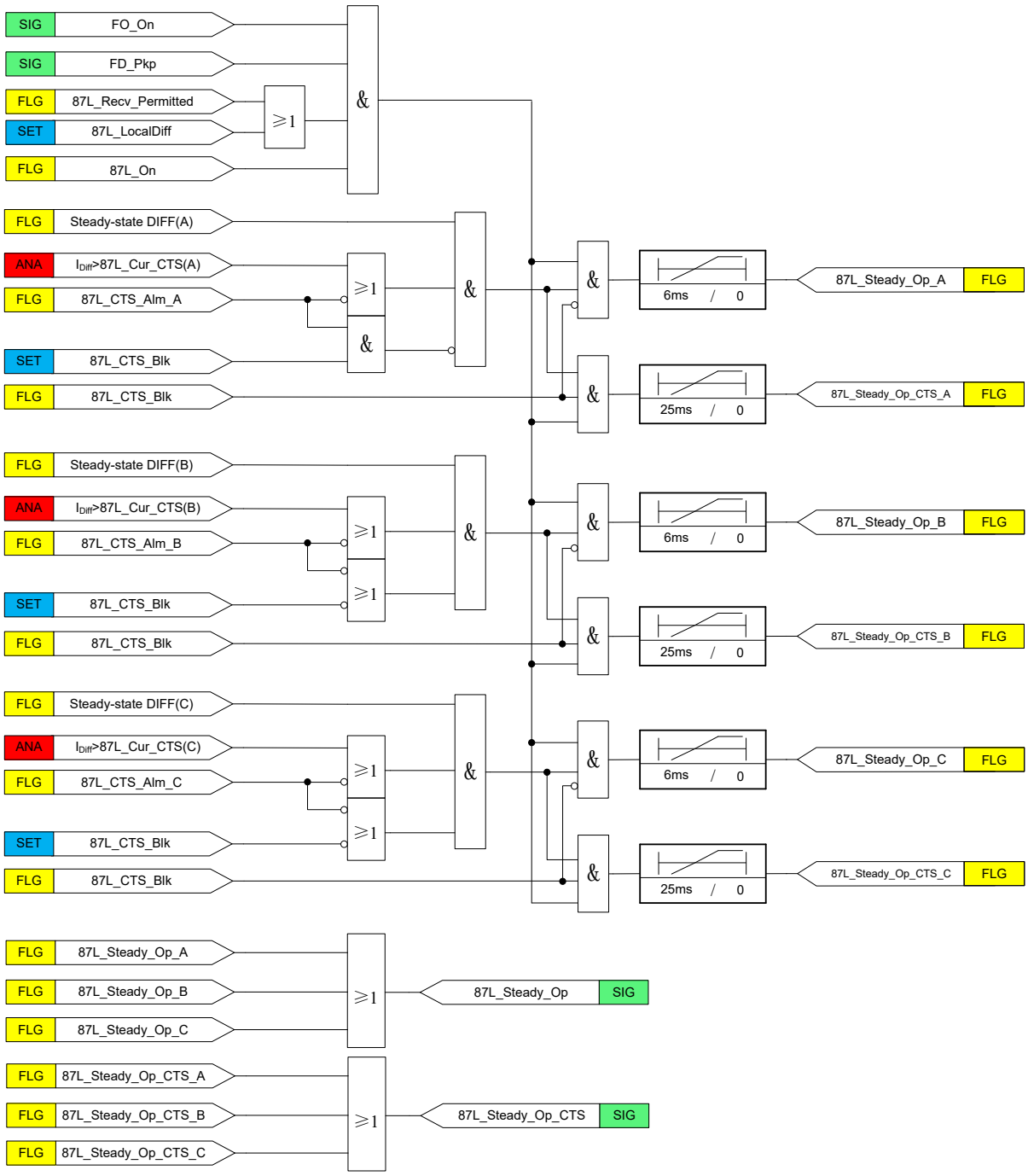


Figure 3.5.6 Steady-state current differential element of 87L

Where:

Steady-state DIFF(A): steady-state current differential element for phase A

Steady-state DIFF(B): steady-state current differential element for phase B

Steady-state DIFF(C): steady-state current differential element for phase C

I_{Diff} : differential current

A: phase A

B: phase B

C: phase C

3.5.3.4 Neutral Current Differential Element

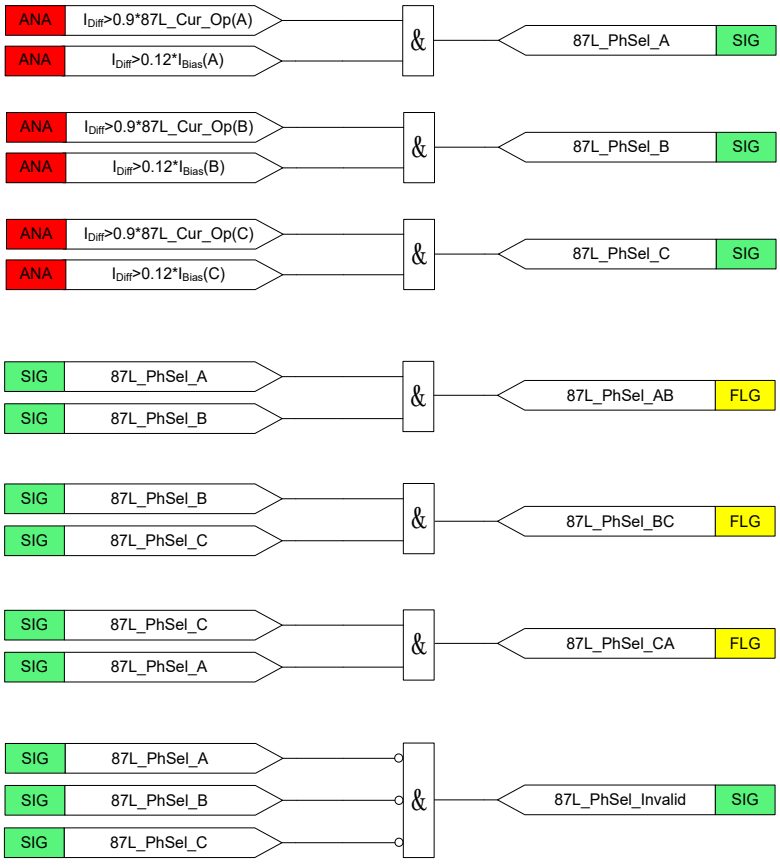


Figure 3.5.7 Phase selection element of 87L

Where:

I_{Diff} : differential current

I_{Bias} : restraint current

A: phase A

B: phase B

C: phase C

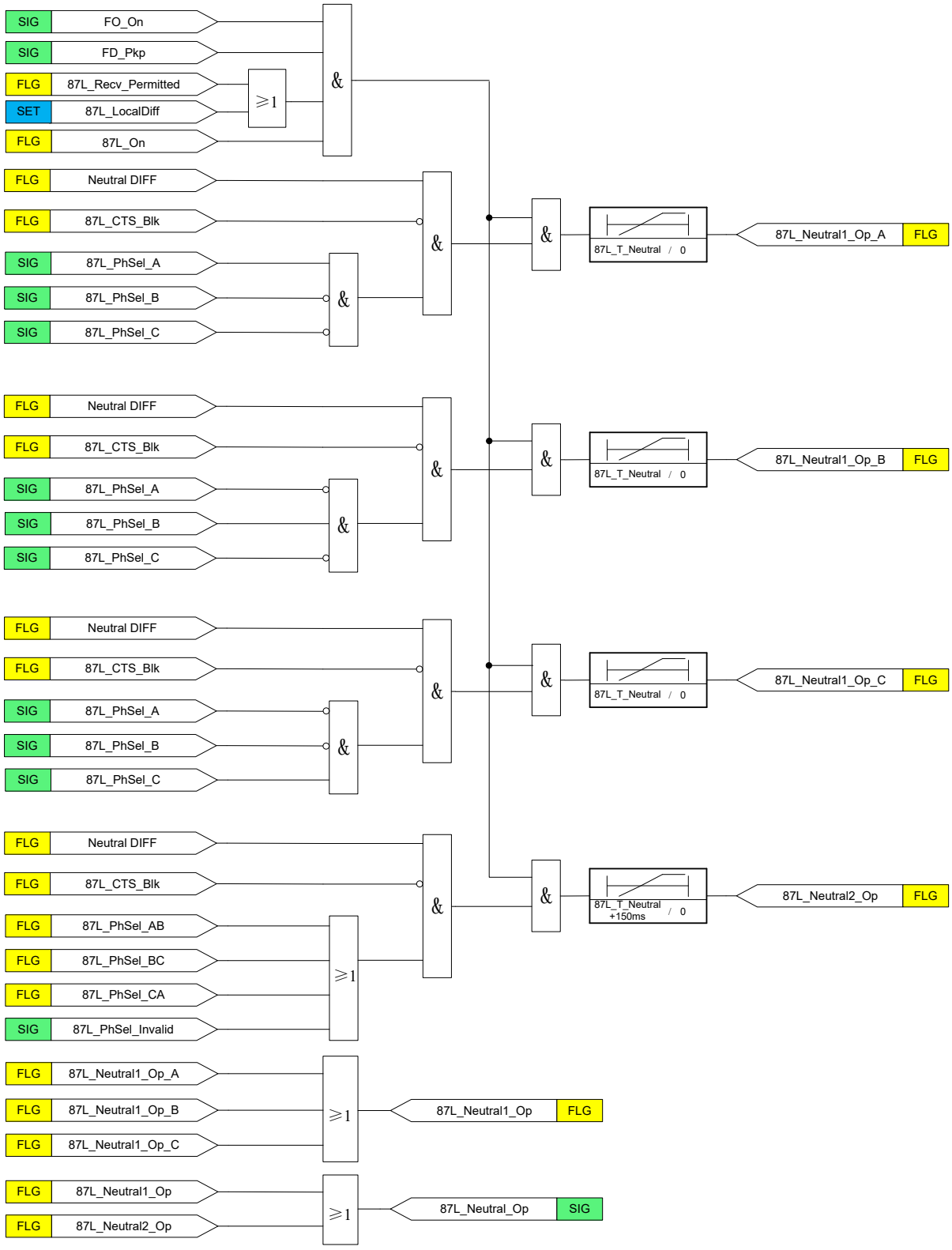


Figure 3.5.8 Neutral current differential element of 87L

Where:

Neutral DIFF: neutral current differential element

3.5.3.5 Operation signals

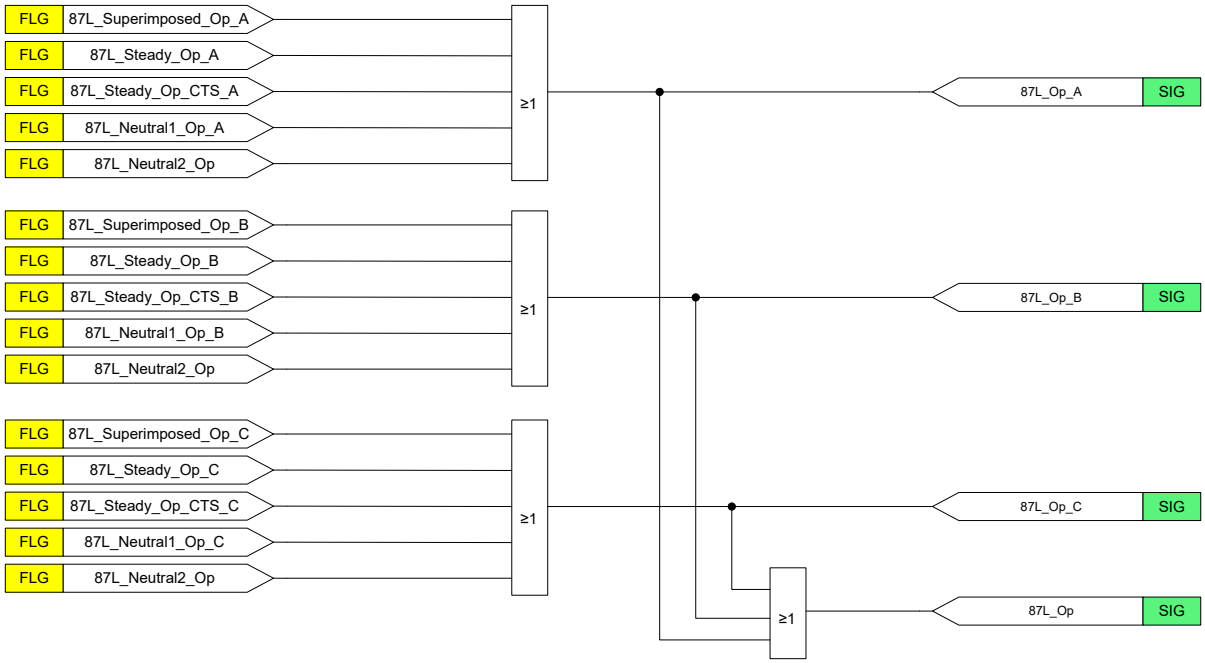


Figure 3.5.9 Operation signals of 87L

3.5.3.6 CT Circuit Failure

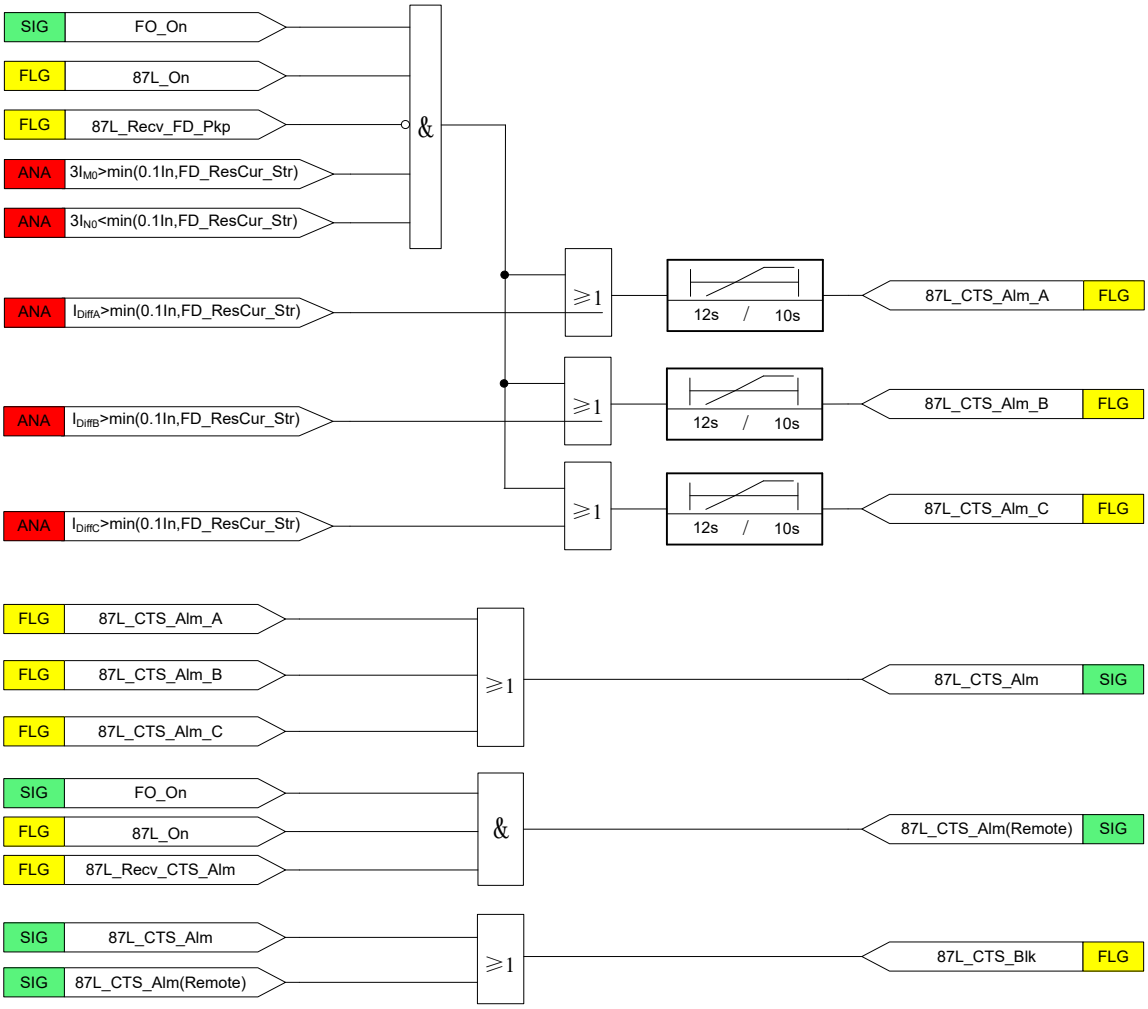


Figure 3.5.10 CT Circuit Failure element of 87L

Where:

$3I_{M0}$: the neutral current at local side.

$3I_{N0}$: the neutral current at remote side.

I_{DiffA} : the differential current of phase A.

I_{DiffB} : the differential current of phase B.

I_{DiffC} : the differential current of phase C.

87L_Recv_FD_Pkp: the device picks up signal that received from the remote end via communication channel. Please refer to section about the conditions of the device picks up.

87L_Recv_CTS_Alm: CT circuit failure signal that received from the remote end via communication channel.

3.5.3.7 Send Permissive Signal

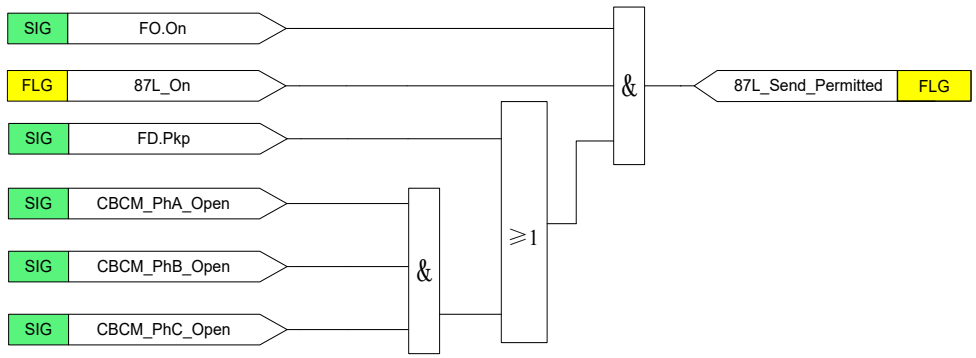


Figure 3.5.11 Sending permissive signal of 87L

3.5.3.8 Differential Current Overreach Alarm

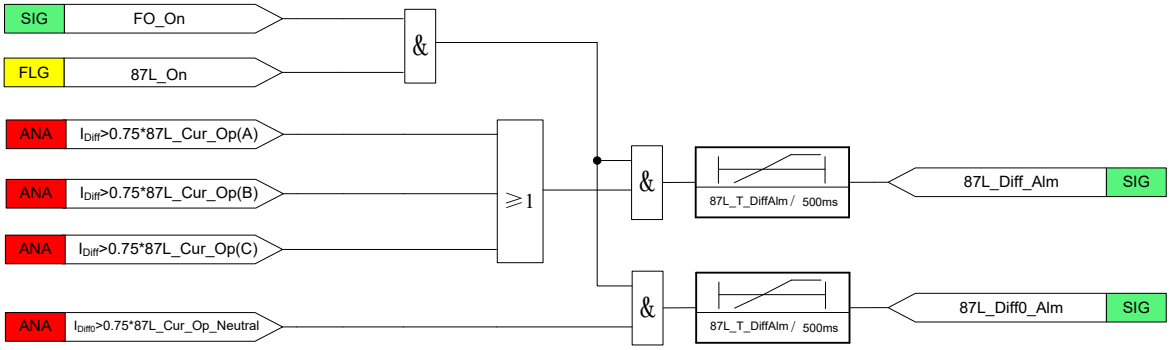


Figure 3.5.12 Differential current overreach alarm signal of 87L

Where:

IDiff : differential current

IDiff0 : the neutral differential current

A: phase A

B: phase B

C: phase C

3.5.4 Settings

Table 3.5-3 Settings of 87L

No.	Name	Range	Unit	Step	Default	Description
1	87L_Ena	0 or 1	-	1	0	Enabling/disabling current differential protection 0: disable 1: enable

No.	Name	Range	Unit	Step	Default	Description
2	87L_CTS_Blk	0 or 1	-	1	0	Enabling/Disabling current differential protection blocked during CT circuit failure 0: disable 1: enable
3	87L_CapCurrComp	0 or 1	-	1	0	Enabling/Disabling capacitive current compensation 0: disable 1: enable
4	87L_LocalDiff	0 or 1	-	1	0	Enabling/disabling local independent current differential protection (independent current differential protection means local current differential protection can operate without permissive signal from remote end) 0: disable 1: enable
5	87L_Cur_Op	(0.05~30.00)×In	A	0.01	2	Current setting of superimposed and steady-state current differential protection
6	87L_Cur_CTS	(0.05~30.00)×In	A	0.01	2	Current setting of current differential protection when CT circuit failure
7	87L_Cur_Op_Neutral	(0.05~30.00)×In	A	0.01	2	Current setting of neutral current differential protection
8	87L_Cur_K1	(0.05~30.00)×In	A	0.01	1	Current setting of knee point 1 for steady-state current differential protection
9	87L_Cur_K2	(0.05~30.00)×In	A	0.01	3	Current setting of knee point 2 for steady-state current differential protection
10	87L_Slope1	0.30~1.00	-	0.01	0.6	Slope 1 of steady-state current differential protection

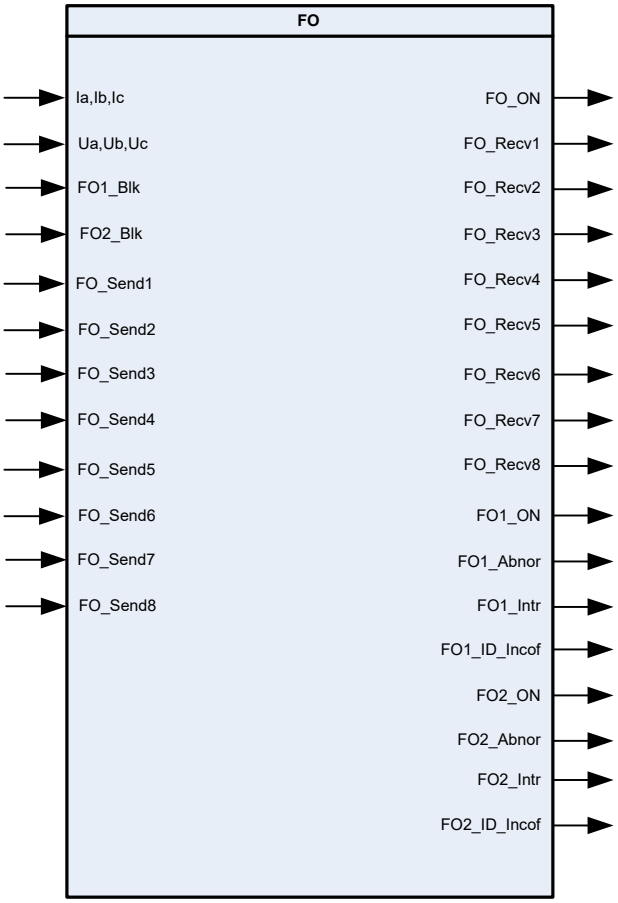
No.	Name	Range	Unit	Step	Default	Description
11	87L_Slope2	0.30~1.00	-	0.01	0.75	Slope 2 of steady-state current differential protection
12	87L_T_Neutral	0.040~10.000	s	0.001	0.1	Time delay of neutral current differential protection
13	87L_T_DiffAlm	1.000~60.000	s	0.001	5	Time delay of differential current overreach alarm
14	87L_X_{C1}	(40~60000)/In	ohm	1	1000	positive-sequence capacitive impedance of the line
15	87L_X_{C0}	(40~60000)/In	ohm	1	1000	Zero-sequence capacitive impedance of the line
16	87L_X_{ML1}	(40~60000)/In	ohm	1	1000	Impedance setting of reactor of local line
17	87L_X_{ML0}	(40~60000)/In	ohm	1	1000	Impedance setting of ground reactor of local line

3.6 Optical Fiber Communication FO

3.6.1 Overview

The devices can transmit permissive signal, blocking signal, transfer signal and transfer trip used by current differential protection via optical fiber channel. The communication rate can be 2048kbits/s via optional dedicated optical fiber channel or multiplex channel. By the setting FO_Protocol, the device can support G.703 or C37.94.

3.6.1.1 Function Block



3.6.1.2 Signals

Table 3.6-1 FO Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	FO1_Blk	Block signal of Channel 1
4	FO2_Blk	Block signal of Channel 2
5	FO_Send1	Sending signal 1
6	FO_Send2	Sending signal 2
7	FO_Send3	Sending signal 3
8	FO_Send4	Sending signal 4
9	FO_Send5	Sending signal 5
10	FO_Send6	Sending signal 6

NO.	Signal	Description
11	FO_Send7	Sending signal 7
12	FO_Send8	Sending signal 8

Table 3.6-2 FO Output Signals

NO.	Signal	Description
1	FO_ON	Channel is normal
2	FO_Recv1	Receiving signal 1
3	FO_Recv2	Receiving signal 2
4	FO_Recv3	Receiving signal 3
5	FO_Recv4	Receiving signal 4
6	FO_Recv5	Receiving signal 5
7	FO_Recv6	Receiving signal 6
8	FO_Recv7	Receiving signal 7
9	FO_Recv8	Receiving signal 8
10	FO1_ON	Channel 1 is normal
11	FO1_Abnor	Channel 1 is abnormal
12	FO1_Intr	Channel 1 is interrup
13	FO1_ID_Incof	Channel 1 ID is inconformity
14	FO2_ON	Channel 2 is normal
15	FO2_Abnor	Channel 2 is abnormal
16	FO2_Intr	Channel 2 is interrup
17	FO2_ID_Incof	Channel 2 ID is inconformity

3.6.2 Protection Principle

Besides current and voltage, 8 digital bits are integrated in each frame of transmission message for various applications. Each received message frame via fiber optical channel will pass through security check to ensure the integrity of the message consistently.

The communication channel can be configured as single channel mode or as dual channels mode.

3.6.2.1 2-terminal Channel Interface

The modules can communicate in two modes via multiplexer or dedicated optical fiber. Communication through dedicated optical fiber is usually recommended unless the received power

does not meet with the requirement.

Channel of 2048kbits/s via dedicated fiber is shown in Figure 3.6.1.

Channel of 2048kbits/s via multiplexer is shown in Figure 3.6.2.

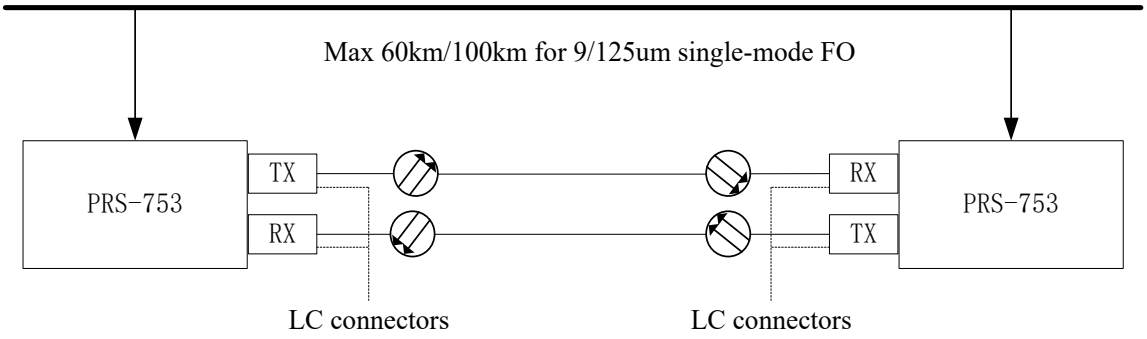


Figure 3.6.1 Direct optical link up to 40km with 1310nm or up to 135km with 1550nm

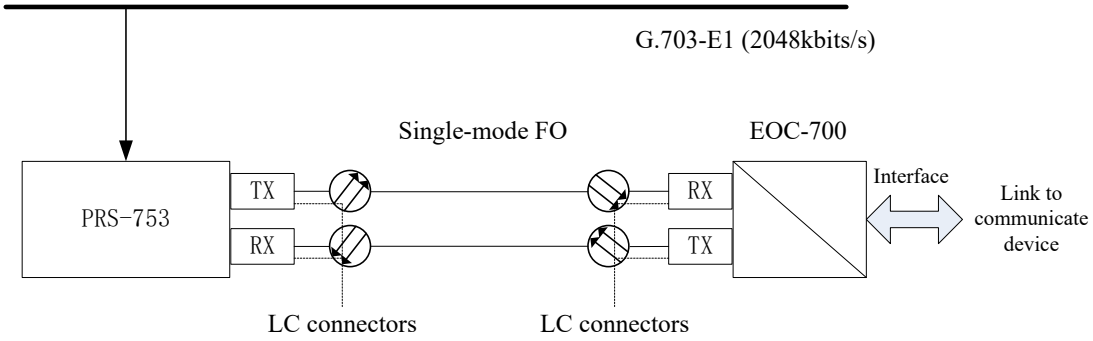


Figure 3.6.2 Connect to a communication network via EOC-700

Two fiber cores of optical cable are dedicated to current differential protection.

Two fiber cores of optical cable are normally in service, and all data are exchanged via the other healthy core if one core is failed.

3.6.2.2 3-terminal Channel Interface

The modules can communicate in two modes via multiplexer or dedicated optical fiber. Communication through dedicated optical fiber is usually recommended unless the received power does not meet with the requirement.

Channel of 2048kbits/s via dedicated fiber is shown in Figure 3.6.3.

Channel of 2048kbits/s via multiplexer is shown in Figure 3.6.4.

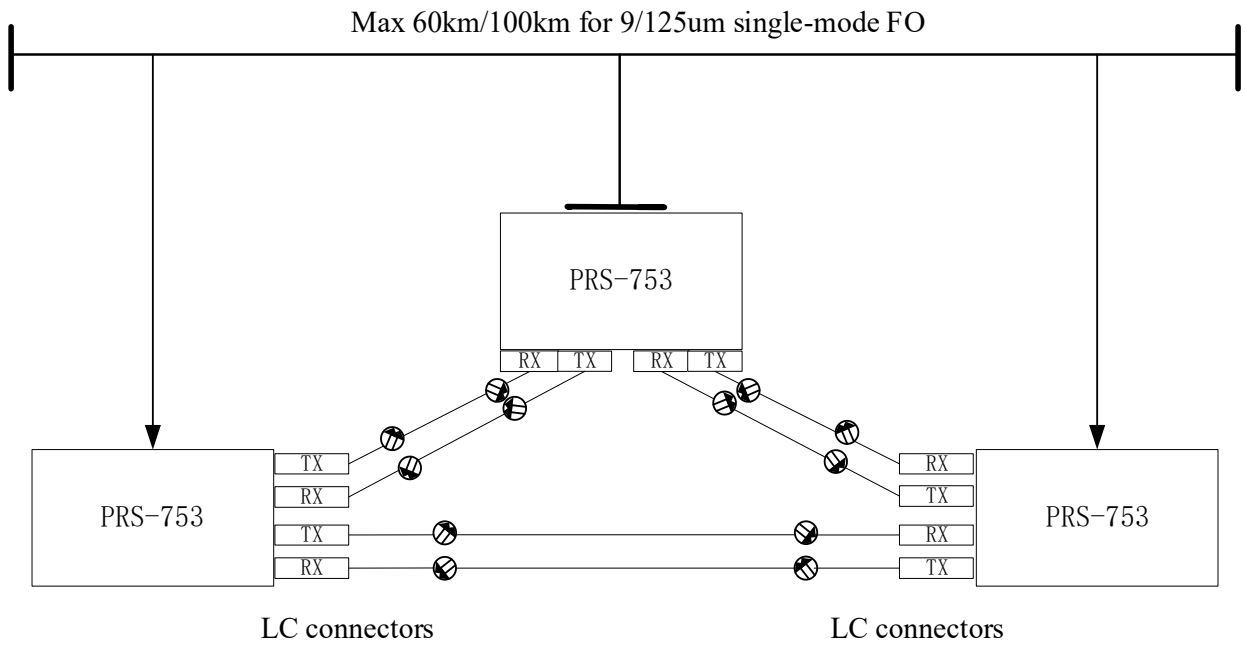


Figure 3.6.3 Direct optical link up to 40km with 1310nm or up to 135km with 1550nm

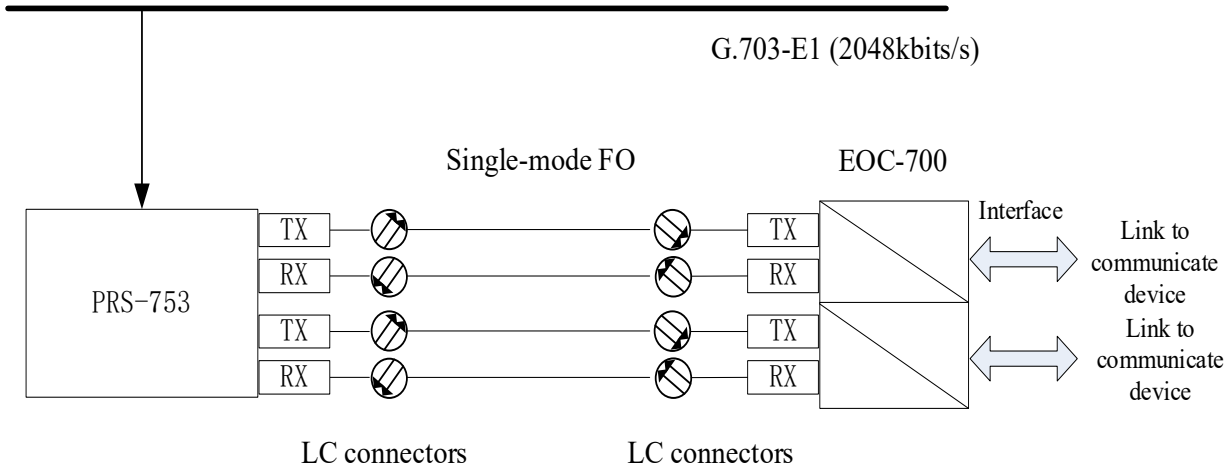


Figure 3.6.4 Connect to communication network via EOC-700

Two fiber cores of optical cable are dedicated to current differential protection.

3.6.2.3 Communication Reliability

To ensure communication reliability, the monitoring and processing of communication state include the following aspects:

Every frame of data goes through CRC test (by hardware) and code test. The one which has errors is rejected;

1) Statistics of error frame will be made every second. If the number of error frames exceed the given value, it is considered as abnormal communication. In case of abnormal communication, the differential protection will be blocked and will automatically continue once the communication is recovered. When the bit error rate of the transmission of the device's

automatically statistics reaches a given value, it will send FOx_Abnor alarm signals.

2) The communication is at a constant speed, so that the number of frames received per second is constant. If number of missing frames goes beyond a given value, it is considered as channel interruption; when the channel is interrupted, the differential protection will be blocked and will automatically continue once the communication is recovered; the device will send FOx_Intr alarm signals when the channel interruption continues 100ms;

3) For the binary inputs in the device that is also transmitted via digital communication channel, special complementary test will be given to further improve the transmission reliability.

3.6.2.4 Communication Clock

The device transmits and receives messages based on respective clocks, which are called transmit clock (i.e. clock TX) and receive clock (i.e. clock RX) respectively. Clock RX is fixed to be extracted from received message frame, which can ensure no slip frame and no error message received.

Clock TX has two options:

1. Use internal crystal clock, which is called internal clock. (master clock)
2. Use external clock, which is extracted from received message frame. (slave clock)

Depend on the clock used by the device at both ends, there are three modes.

1. Master-master mode

Both ends use internal clock.

2. Slave-slave mode

Both ends use external clock.

3. Master-slave mode

One of them uses internal clock, the other uses external clock.

The logic setting FOx_IntClock is used in current differential protection to select the communication clock. The internal clock is enabled automatically when the logic setting FOx_IntClock is set as “1”. Contrarily, the external clock is enabled automatically when the logic setting FOx_IntClock is set to “0”.

If the device uses dedicated optical fibre channel, the devices at both sides shall be set as internal clock. Then the clock inside of the device is used in transmitting data, and the transmitter clock is extracted from received message frame.

If the device uses the 2048kbits/s (E1) interface of the SDH digital communication system by EOC-700 equipment, the devices at both sides shall be set as external clock. The transmitter clock and receive clock of data are the same clock source, both extracted from the received code stream.

3.6.2.5 Identity Code

In order to ensure reliability of the device when digital communication channel is applied, settings FO_LocID and FO_RmtID are provided as identity code to distinguish uniquely the device at remote

end using same channel.

Under normal conditions, the identity code of the device at local end should be different with that at remote end. In addition, it is recommended that the identity code of all devices, i.e., the setting FO_LocID, should be unique in the power grid. The setting range is from 0 to 65535. Only for loop test, they are set as the same.

The setting FO_LocID of the device at an end should be the same as the setting FO_RmtID of the device at opposite end and the greater FO_LocID between the two ends is chosen as a master end for sampling synchronism, the smaller FO_LocID is slave end. If the setting FO_LocID is set the same as FO_RmtID, that implies the device in loopback testing state.

The setting FO_LocID is packaged in the message frame and transmitted to the remote end. When the FO_LocID of the device at remote end received by local device is same to the setting FO_RmtID of local device, the message received from the remote end is valid, and protection information involved in message is read. When these settings are not matched, the message is considered as invalid and protection information involved in message is ignored, FOx_ID_Incof alarm will be issued.

3.6.3 Logic

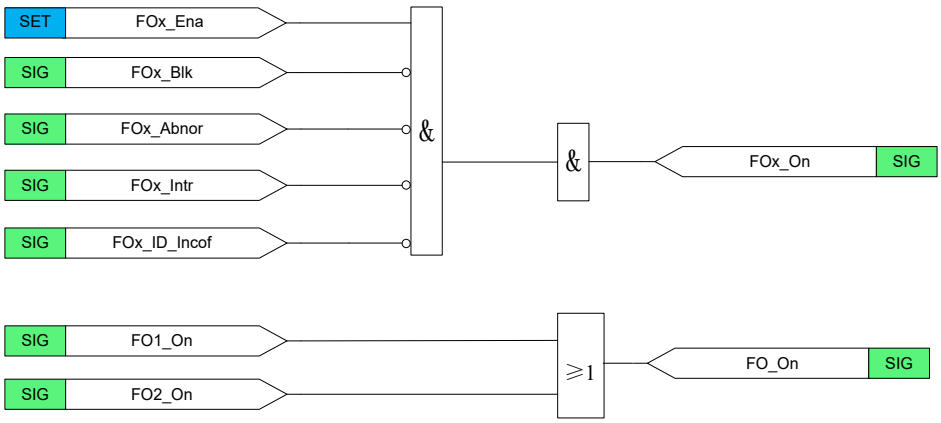


Figure 3.6.3 Logic diagram of optical fibre channel enabling

3.6.4 Settings

Table 3.6-3 Settings of optical fibre communication

No.	Name	Range	Unit	Step	Default	Description
1	FO_Protocol	0 or 1	-	1	0	It is used to select protocol type, G.703 or C37.94 0: G.703 1: C37.94
2	FO_LocID	0~65535	-	1	1	Identity code of the device at local end

No.	Name	Range	Unit	Step	Default	Description
3	FO_RmtID	0~65535	-	1	0	Identity code of the device at remote end
4	FOx_Ena	0 or 1	-	1	0	Enabling/disabling channel x (x can be 1 or 2) 0: disable 1: enable
5	FOx_IntClock	0 or 1	-	1	1	Option of internal clock or external clock(x can be 1 or 2) 0: external clock 1: internal clock

3.7 Distance Protection 21

3.7.1 Overview

The main and important function of distance protection (21) is to monitored the transmission line (T/L) operating parameters and to provide very sensitive and accurate operation of protection where overcurrent protection and earth fault protection cannot meet the required high standard of protection. Such kind of protection operates based on the ratio of voltage and current is known as distance protection. The ratio of current and voltage directly measured by current transformer (CT) and voltage or potential transformer (PT or VT) respectively.

Distance protection (21) relay device provide forward or reverse five settable zone.

Every zone of distance protection is providing dependable settings and full design scheme of measurement phase to phase (line value) and phase to earth (phase value). The characteristics of distance protection zone are:

- Mho characteristics
    - Phase to phase (line value) distance element
    - Phase to earth (phase value) distance element
    - Distance SOTF element
- Quadrilateral characteristics
    - Phase to phase (line value) distance protection
    - Phase to earth (phase value) distance protection
    - Reactance line element
    - Direction line element
    - Resistance line element
    - Distance SOTF element
- Power swing blocking releasing (PSBR)

- Each zone can be easily configuring PSBR setting

- Load Encroachment (LoadEnch)
  - Configure with long and heavy loaded transmission lines

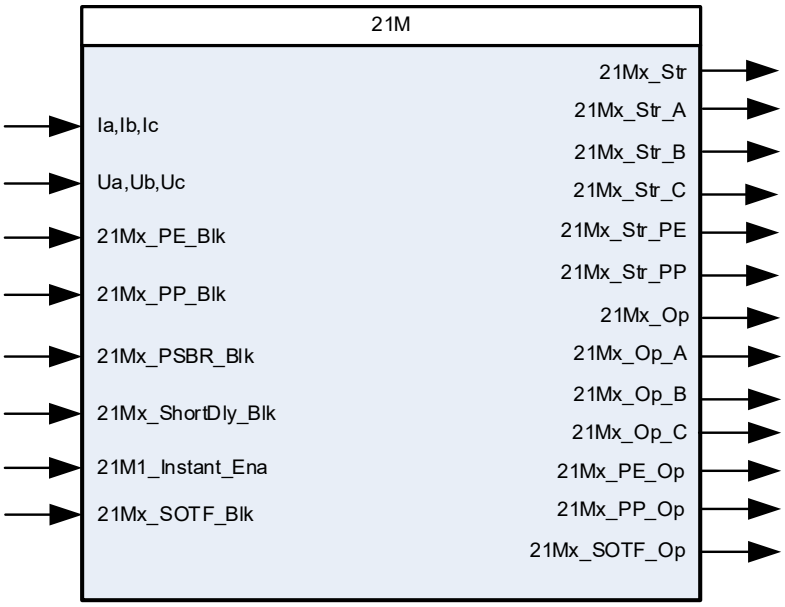
- Pilot distance protection
  - The pilot zone is for PUTT, POTT and blocking scheme.
  - The forward direction element is for sending signal for POTT and tripping upon receiving permissive signal for both PUTT and POTT scheme.
  - The forward direction element for blocking scheme is used to stop sending blocking signal.
  - The reverse direction element is only for POTT scheme with weak infeed condition.

When VT circuit fails, VT circuit supervision logic will output a blocking signal to block all distance protection.

Distance protection can select line VT or bus VT for protection algorithm by a setting VTS_LineVT.

3.7.2 Mho Distance Protection 21M

3.7.2.1 Function Block



3.7.2.2 Signals

Table 3.7-1 21M Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	21Mx_PE_Blk	Block signal of phase-to-earth 21M zone x (x=1,2,3,4,5)
4	21Mx_PP_Blk	Block signal of phase-to-phase 21M zone x (x=1,2,3,4,5)

NO.	Signal	Description
5	21Mx_PSBR_Blk	Blocking power swing blocking releasing of 21M zone x (x=1,2,3,4,5)
6	21Mx_ShortDly_Blk	Block signal of accelerating 21M zone x (x=2,3,4,5)
7	21M1_Instant_Ena	Enable zone 1 of distance protection operates without time delay
8	21Mx_SOTF_Blk	Block signal of distance switch onto fault function zone x (x=1,2,3,4,5)

Table 3.7-2 21M Output Signals

NO.	Signal	Description
1	21Mx_Str	Common start signal from zone x (x=1,2,3,4,5)
2	21Mx_Str_A	Start signal from phase A zone x (x=1,2,3,4,5)
3	21Mx_Str_B	Start signal from phase B zone x (x=1,2,3,4,5)
4	21Mx_Str_C	Start signal from phase C zone x (x=1,2,3,4,5)
5	21Mx_Str_PE	Start signal from phase-to-earth zone x (x=1,2,3,4,5)
6	21Mx_Str_PP	Start signal from phase-to-phase zone x (x=1,2,3,4,5)
7	21Mx_Op	Operation signal from zone x (x=1,2,3,4,5)
8	21Mx_Op_A	Operation signal from phase A zone x (x=1,2,3,4,5)
9	21Mx_Op_B	Operation signal from phase B zone x (x=1,2,3,4,5)
10	21Mx_Op_C	Operation signal from phase C zone x (x=1,2,3,4,5)
11	21Mx_PE_Op	Operation signal from phase-to-earth zone x (x=1,2,3,4,5)
12	21Mx_PP_Op	Operation signal from phase-to-phase zone x (x=1,2,3,4,5)
13	21Mx_SOTF_Op	Operation signal from switch onto fault function (x=1,2,3,4,5)

3.7.2.3 Protection Principle

1. Phase-to-phase distance element

Phase-to-phase positive sequence voltage is used as polarized signal for phase-to-phase distance protection.

Operation voltage: $\dot{U}_{op\,\phi\,\phi} = \dot{U}_{\phi\,\phi} - \dot{I}_{\phi\,\phi} \times Z_{ZD}$ $\phi\ \phi = AB, BC, CA$

Polarized voltage: $\dot{U}_{p\,\phi\,\phi} = \dot{U}_{1\,\phi\,\phi}\angle\theta$

Where:

Z_{ZD} : the impedance setting zone x of phase-to-phase distance protection, set by the setting 21Mx_PP_Imp_Op (x=1, 2, 3, 4, 5)

$U_{\phi\phi}$ is the phase-to-phase voltage

$U_{1\phi\phi}$ is the positive sequence voltage

$I_{\phi\phi}$ is the phase-to-phase current

Phase comparison equation is:

$$270° > \arg\frac{\dot{U}_{p\phi\phi}}{\dot{U}_{op\phi\phi}} > 90°$$

In short line, phase shift θ could be applied to the polarized voltage to improve the performance against high resistance fault. The device provides an angle-shift setting, 21Mx_PP_Phi_Shift, to set value of θ among 0°, 15° and 30°. Their impedance shift characteristics towards quadrant 1 are respectively shown as the impedance circle A, B and C in Figure 3.7.2.

For the three-phase close up short-circuit fault, the positive sequence voltage is lower, and the memorized positive sequence voltage is used. When the memory fades out, the operation characteristic will be reverse offset a little to enclose the origin to ensure keeping operating of distance protection until the fault being cleared. The phase comparison equation is:

$$270° > \arg\frac{\dot{U}_{\phi\phi} + 0.1 \times \dot{I}_{\phi\phi} \times Z_{ZD}}{\dot{U}_{\phi\phi} - \dot{I}_{\phi\phi} \times Z_{ZD}} > 90°$$

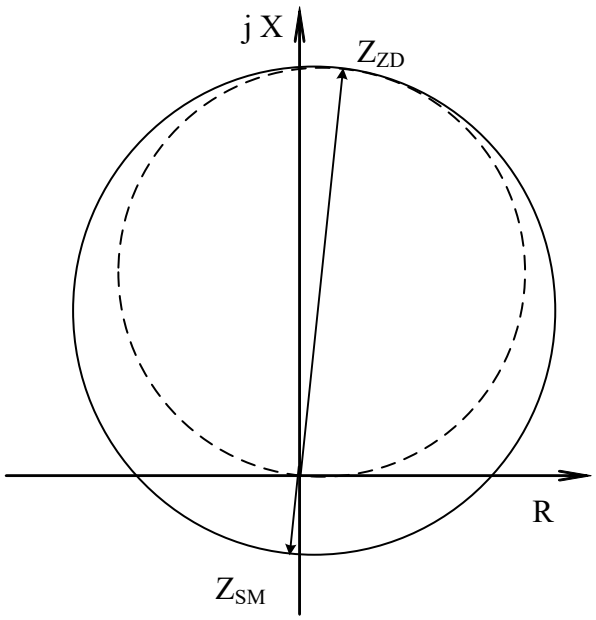


Figure 3.7.1 Phase-to-phase operation characteristic of mho distance protection

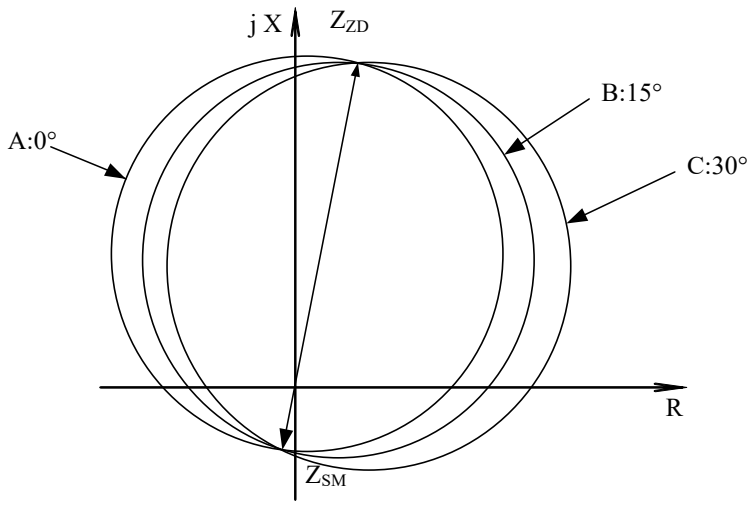


Figure 3.7.2 Impedance shift characteristic of mho distance protection

2. Phase-to- earth distance element

Operation criteria:

$$270° > \arg\frac{\dot{U}_{1\phi}\angle\theta}{\dot{U}_{\phi} - \left(\dot{I}_{\phi} + k \times 3\dot{I}0\right) \times Z_{ZD}} > 90° \qquad \phi = A, B, C$$

Where:

Z_{ZD} : the impedance setting zone x of phase-to-ground distance protection, set by the setting 21Mx_PE_Imp_Op (x=1, 2, 3, 4, 5)

U_{ϕ} is the phase voltage

I_{ϕ} is the phase current

$U_{1\phi}$ is the positive sequence voltage

$3I0$ is the zero-sequence current

k is zero-sequence compensation coefficient

In short line, phase shift θ could be applied to the polarized voltage to improve the performance against high resistance fault. The device provides an angle-shift setting, 21Mx_PE_Phi_Shift, to set value of θ among 0°, 15° and 30°. Their impedance shift characteristics towards quadrant 1 are respectively shown as the impedance circle A, B and C in Figure 3.7.2.

To improve the operation characteristics of phase-to-ground distance element so as to allow them to cover ground fault with high resistance. Without overreach, the device adopts zero sequence reactance relays to further solve the problem of overreach operation of phase-to-ground distance element. The operation criterion of zero sequence reactance relays is:

$$360° > \arg\frac{\dot{U}_{\phi} - \left(\dot{I}_{\phi} + k \times 3\dot{I}0\right) \times Z_{ZD}}{\left(\dot{I}_{\phi} + k \times 3\dot{I}0\right) \angle -\beta} > 180°$$

Where:

β: the angle of zero sequence compensation reactance, set by 21Mx_X0Comp_Ang.

The operation characteristics of above equation on impedance planes are a straight line at the set impedance vector end, shown as figure 3.7.3. In the operation criterion of zero sequence reactance relays, $\dot{I}0$ phase moves backward for β degree to appropriately limit its operation area to improve safety.

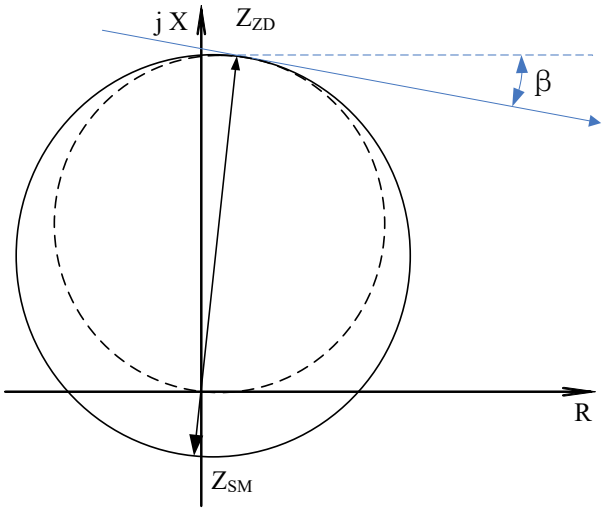


Figure 3.7.3 Phase-to-ground operation characteristic of mho distance protection

3. Distance SOTF element

When the logic setting 21Mx_SOTF_Ena is set to “1”, the distance SOTF element is enabled. For manual closing or automatic closing on to a fault, zone1, 2, 3 ,4 or 5 of distance protection will accelerate to trip, and block AR.

3.7.2.4 Logic

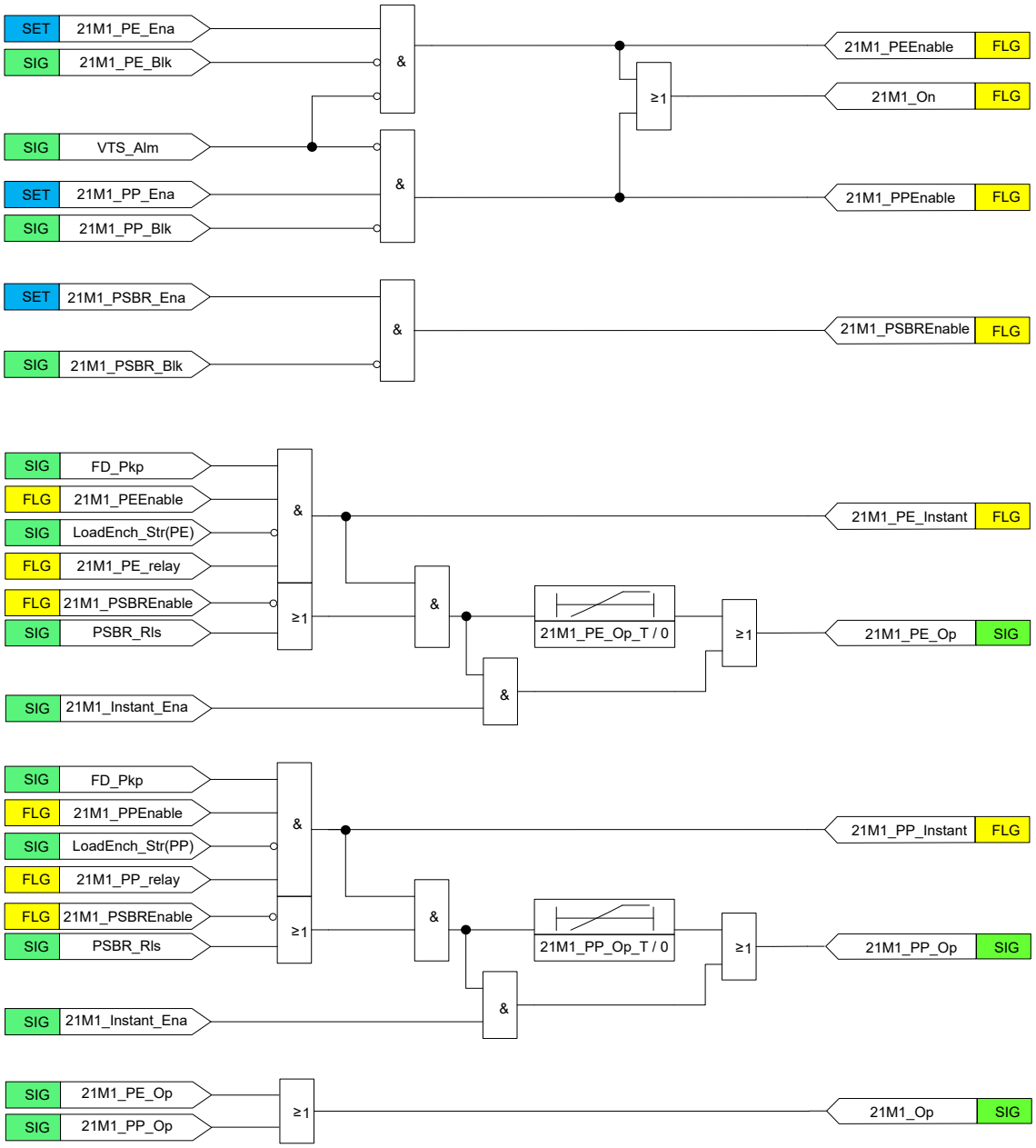


Figure 3.7.4 Logic diagram of distance protection (Mho zone 1)

Where:

PSBR_Rls: is the signal of power swing blocking releasing signal

21M1_PE_relay means that measured impedance by zone 1 of phase-to-earth distance protection is within the range determined by the setting 21M1_PE_Imp_Op.

21M1_PP_relay means that measured impedance by zone 1 of phase-to-phase distance protection is within the range determined by the setting 21M1_PP_Imp_Op.

LoadEnch_Str (PE) means that load trapezoid characteristic for distance element is enabled and measured phase-to-earth impedance into the load area.

LoadEnch_Str (PP) means that load trapezoid characteristic for distance element is enabled and measured phase-to-phase impedance into the load area.

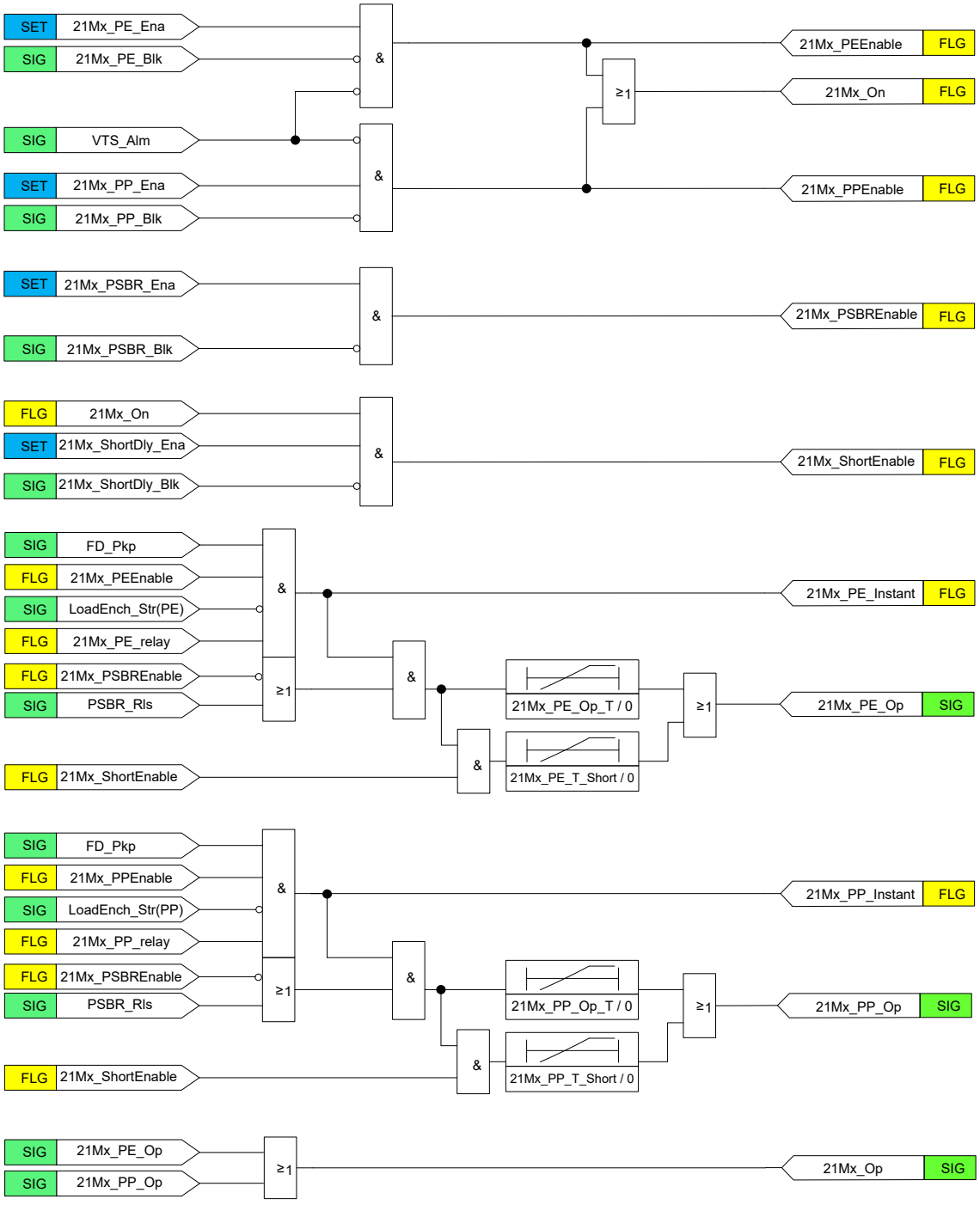


Figure 3.7.5 Logic diagram of distance protection (Mho zone x)

Where:

x=2,3,4,5

21Mx_PE_relay means that measured impedance by zone x of phase-to-earth distance protection is within the range determined by the setting 21Mx_PE_Imp_Op.

21Mx_PP_relay means that measured impedance by zone x of phase-to-phase distance protection is within the range determined by the setting 21Mx_PP_Imp_Op.

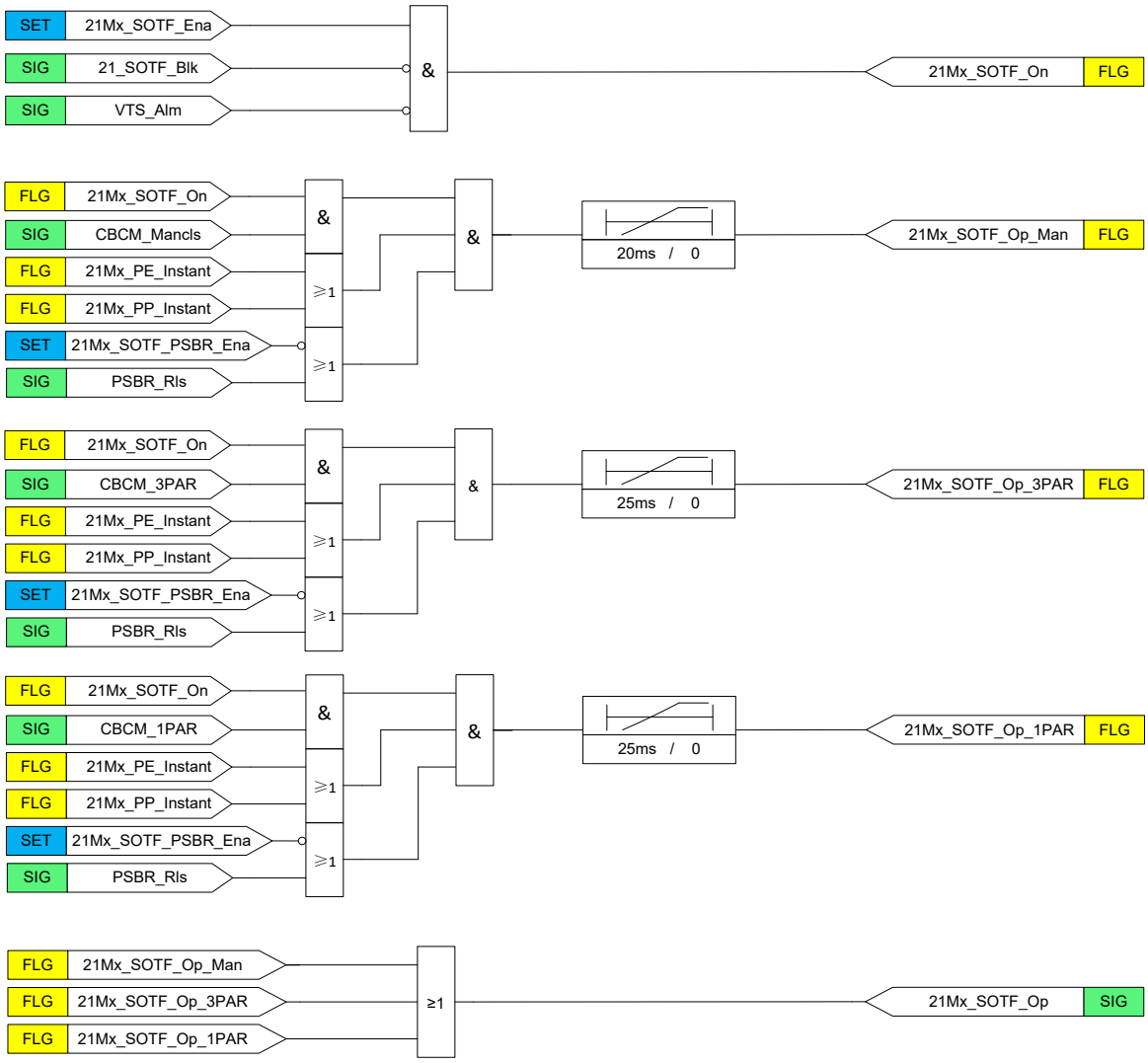


Figure 3.7.6 Logic diagram of Mho distance protection (SOTF)

Where:

x=1,2,3,4,5

CBCM_Mancls: is the signal of Manual closing signal for SOTF logic

CBCM_1PAR: is the signal of 1-pole reclosing signal for SOTF logic

CBCM_3PAR: is the signal of 3-pole reclosing signal for SOTF logic

3.7.2.5 Settings

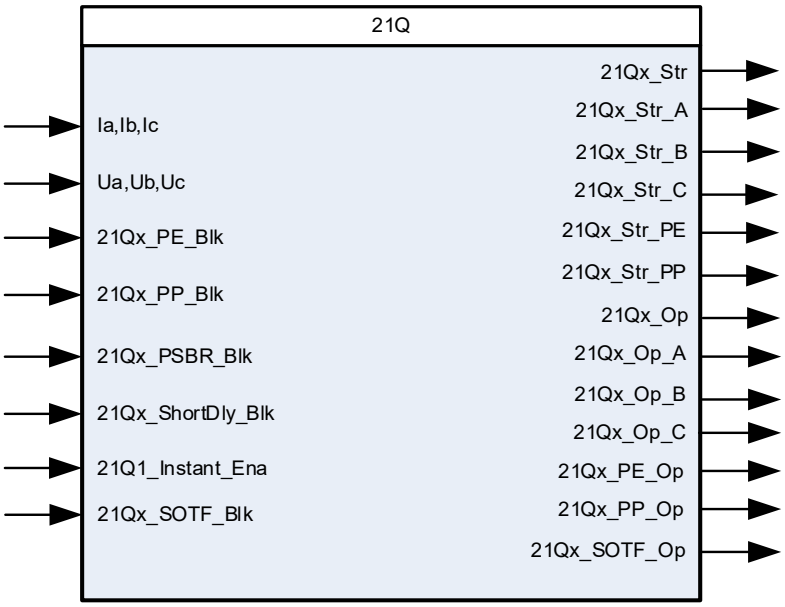
Table 3.7-3 21M Settings

NO	Name	Range	Unit	Step	Default	Description
1	21Mx_Dir_Mod	0 or 1	-	1	0	Direction option for zone x of distance protection (x=1,2, 3, 4, 5) 0: Forward 1: Reverse
2	21Mx_PE_Ena	0 or 1	-	1	0	Enabling/disabling zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
3	21Mx_PP_Ena	0 or 1	-	1	0	Enabling/disabling zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
4	21Mx_PSBR_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance protection controlled by PSBR (x=1, 2, 3, 4, 5) 0: disable 1: enable
5	21Mx_ShortDly_Ena	0 or 1	-	1	0	Enabling/disabling fixed accelerate zone x of distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
6	21Mx_SOTF_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance SOTF protection (x=1, 2, 3, 4, 5) 1: enable 0: disable
7	21Mx_SOTF_PSBR_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance SOTF protection controlled by PSBR (x=1, 2, 3, 4, 5) 1: enable 0: disable
8	21Mx_ZAng	10~89	deg	0.01	85	Phase angle of positive-sequence impedance for zone x of distance protection (x=1, 2, 3, 4, 5)

NO	Name	Range	Unit	Step	Default	Description
9	21Mx_Kz	0~10.000	-	0.001	0.67	Zero-sequence compensation coefficient magnitude for zone x of distance protection (x=1, 2, 3, 4, 5)
10	21Mx_KzAng	0~360.00	deg	0.01	0	Zero-sequence compensation coefficient angle for zone x of distance protection (x=1, 2, 3, 4, 5)
11	21Mx_PE_Phi_Shift	0, 15 or 30	deg	15	0	Phase shift of phase-to-earth distance protection for zone x (x=1, 2, 3, 4, 5)
12	21Mx_X0Comp_Ang	0~30	deg	0.01	12	Zero sequence reactance compensation angle (x=1, 2, 3, 4, 5)
13	21Mx_PE_Imp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
14	21Mx_PE_Op_T	0.000~10.000	s	0.001	10	Time delay of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
15	21Mx_PE_T_ShortDly	0.000~10.000	s	0.001	10	Short time delay of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
16	21Mx_PP_Phi_Shift	0, 15 or 30	deg	15	0	Phase shift of phase-to-phase distance protection for zone x (x=1, 2, 3, 4, 5)
17	21Mx_PP_Imp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)
18	21Mx_PP_Op_T	0.000~10.000	s	0.001	10	Time delay of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)
19	21Mx_PP_T_ShortDly	0.000~10.000	s	0.001	10	Short time delay of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)

3.7.3 Quadrilateral Distance Protection 21Q

3.7.3.1 Function Block



3.7.3.2 Signals

Table 3.7-4 21Q Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	21Qx_PE_Blk	Block signal of phase-to-earth 21Q zone x (x=1,2,3,4,5)
4	21Qx_PP_Blk	Block signal of phase-to-phase 21Q zone x (x=1,2,3,4,5)
5	21Qx_PSBR_Blk	Blocking power swing blocking releasing of 21Q zone x (x=1,2,3,4,5)
6	21Qx_ShortDly_Blk	Block signal of accelerating 21Q zone x (x=2,3,4,5)
7	21Q1_Instant_Ena	Enable zone 1 of distance protection operates without time delay
8	21Qx_SOTF_Blk	Block signal of distance switch onto fault function zone x (x=1,2,3,4,5)

Table 3.7-5 1Q Output Signals

NO.	Signal	Description
1	21Qx_Str	Common start signal from zone x (x=1,2,3,4,5)
2	21Qx_Str_A	Start signal from phase A zone x (x=1,2,3,4,5)
3	21Qx_Str_B	Start signal from phase B zone x (x=1,2,3,4,5)
4	21Qx_Str_C	Start signal from phase C zone x (x=1,2,3,4,5)

NO.	Signal	Description
5	21Qx_Str_PE	Start signal from phase-to-earth zone x (x=1,2,3,4,5)
6	21Qx_Str_PP	Start signal from phase-to-phase zone x (x=1,2,3,4,5)
7	21Qx_Op	Operation signal from zone x (x=1,2,3,4,5)
8	21Qx_Op_A	Operation signal from phase A zone x (x=1,2,3,4,5)
9	21Qx_Op_B	Operation signal from phase B zone x (x=1,2,3,4,5)
10	21Qx_Op_C	Operation signal from phase C zone x (x=1,2,3,4,5)
11	21Qx_PE_Op	Operation signal from phase-to-earth zone x (x=1,2,3,4,5)
12	21Qx_PP_Op	Operation signal from phase-to-phase zone x (x=1,2,3,4,5)
13	21Qx_SOTF_Op	Operation signal from switch onto fault function (x=1,2,3,4,5)

3.7.3.3 Protection Principle

Features available with quadrilateral distance protection include 5 settable forward or reverse zones phase-to-ground or phase-to-phase distance element. Each zone can respectively enable or disable power swing blocking releasing.

1) The reactance line element

Operation criteria:

phase-to-ground:

$$180° < \arg\frac{\dot{U}_{\phi} - \left(\dot{I}_{\phi} + k \times 3\dot{I}0\right) \times Z_{ZD}}{\left(\dot{I}_{\phi} + k \times 3\dot{I}0\right)\angle -\delta} < 360° \qquad \phi = A, B, C$$

phase-to-phase:

$$180° < \arg\frac{\dot{U}_{\phi\,\phi} - \dot{I}_{\phi\,\phi} \times Z_{ZD}}{\dot{I}_{\phi\,\phi}\angle -\delta} < 360° \qquad \phi\ \phi = AB, BC, CA$$

Where:

Z_{ZD} : the impedance setting zone x of quadrilateral distance protection, set by the setting 21Qx_PE_Imp_Op OR 21Qx_PP_Imp_Op (x=1, 2, 3, 4, 5)

$U_{\phi\,\phi}$ is the phase-to-phase voltage

$I_{\phi\,\phi}$ is the phase-to-phase current

U_{ϕ} is the phase voltage

I_{ϕ} is the phase current

$3I0$ is the zero-sequence current

k is zero-sequence compensation coefficient

δ: the angle of zero sequence compensation reactance, set by 21Qx_X0Comp_Ang.

2) The directional line element

Operation criteria:

phase-to-ground:

$$-\alpha < \arg\frac{\dot{U}_{p\phi}}{\dot{I}_{\phi}} < 90° + \beta$$

phase-to-phase:

$$-\alpha < \arg\frac{\dot{U}_{p\phi\phi}}{\dot{I}_{\phi\phi}} < 90° + \beta$$

Where:

$\dot{U}_{p\phi\phi}$ is the phase-to-phase polarized voltage

$\dot{U}_{p\phi}$ is the phase polarized voltage

α: the angle of directional line, set by the setting 21Qx_Ang_Alpha (x=1, 2, 3, 4, 5)

β: the angle of directional line, set by the setting 21Qx_Ang_Beta (x=1, 2, 3, 4, 5)

3) The resistance line element

Operation criteria:

phase-to-ground:

$$\varphi < \arg\frac{\dot{U}_{\phi} - \left(\dot{I}_{\phi} + k \times 3\dot{I}0\right) \times R_{ZD}}{\left(\dot{I}_{\phi} + k \times 3\dot{I}0\right)} < 180° + \varphi$$

phase-to- phase:

$$\varphi < \arg\frac{\dot{U}_{\phi\phi} - \dot{I}_{\phi\phi} \times R_{ZD}}{\dot{I}_{\phi\phi}} < 180° + \varphi$$

Where:

R_{ZD} : the resistance setting zone x of quadrilateral distance protection, set by the setting 21Qx_PE_R_Op OR 21Qx_PP_R_Op (x=1, 2, 3, 4, 5)

φ: phase angle of positive-sequence impedance for zone x of distance protection, set by the setting 21Qx_ZAng (x=1, 2, 3, 4, 5)

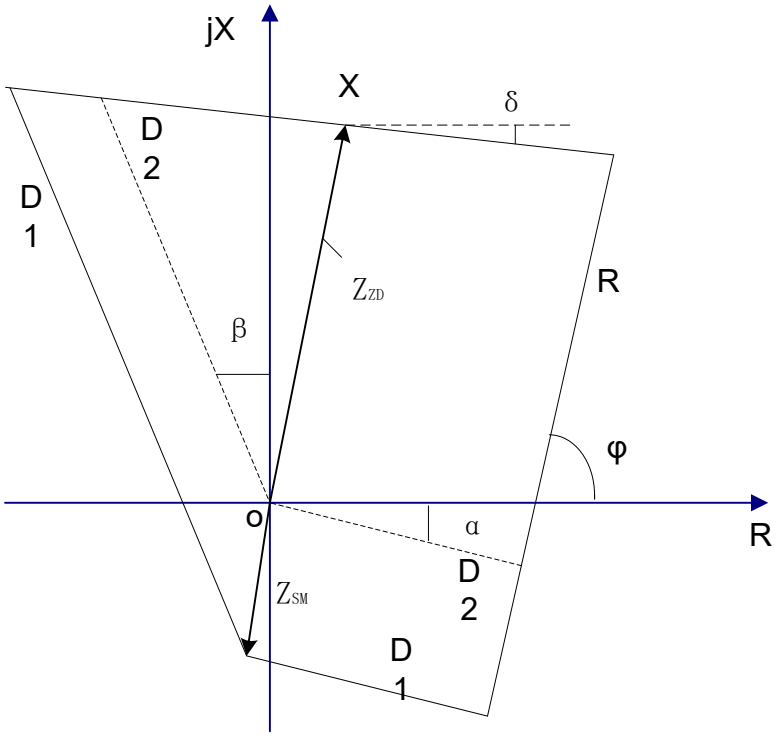


Figure 3.7.7 Impedance characteristic of quadrilateral distance protection

In the figure 3.7.6,the X element completes the fault location, adopt the reactance line element, characteristic is like X line, downward offset angle of the R axis; the D element completes the direction judgment, adopt the directional line element, characteristic is like D broken line; the R element reflect high-impedance-grounded faults, adopt the resistance line element, characteristic is like R line.

When the logic setting 21Qx_SOTF_Ena is set to “1”, the distance SOTF element is enabled. For manual closing or automatic closing on to a fault, zone 1,2,3,4 or 5 of distance protection will accelerate to trip.

3.7.3.4 Logic

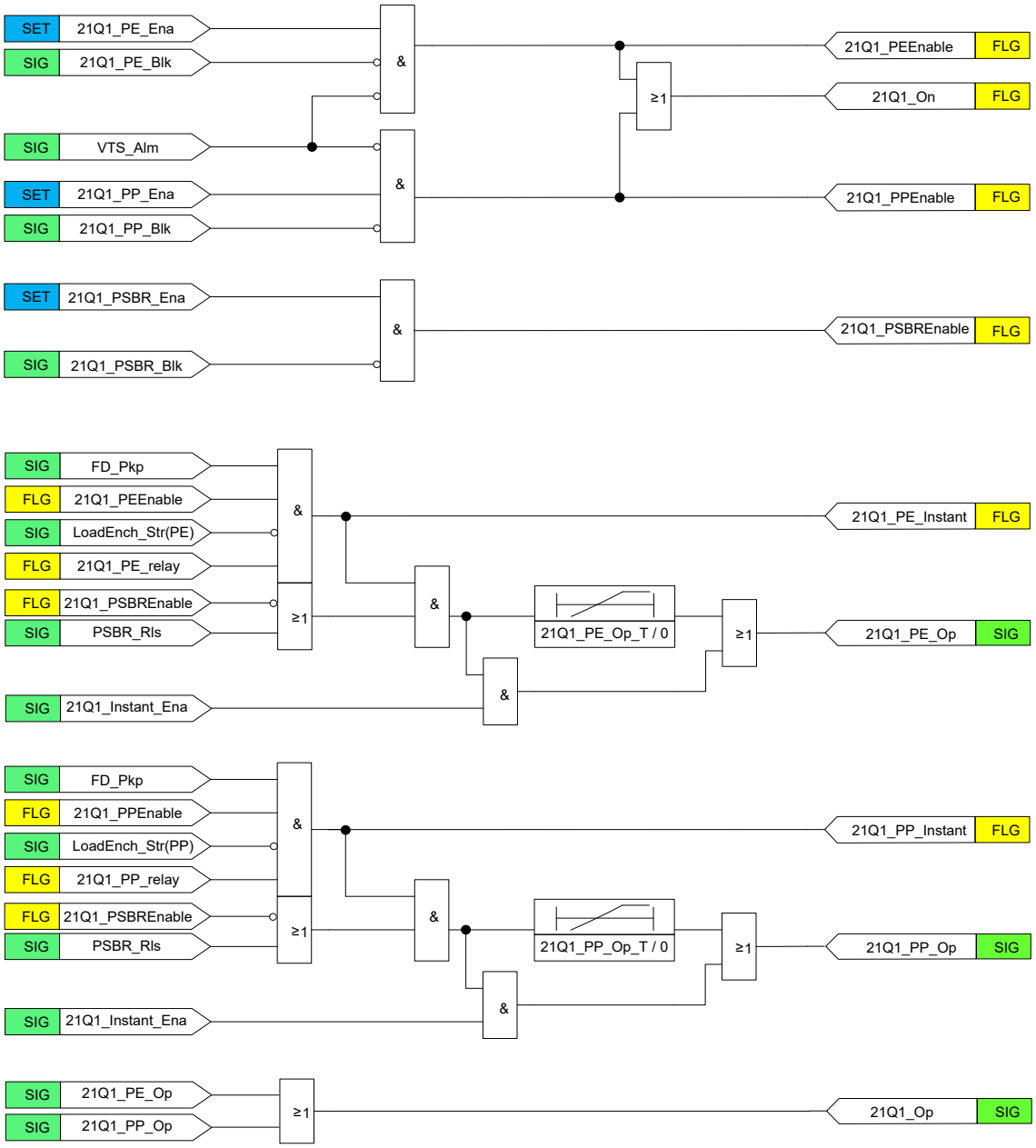


Figure 3.7.8 Logic diagram of distance protection (Quad zone 1)

Where:

PSBR_Rls: is the signal of power swing blocking releasing signal

21Q1_PE_relay means that measured impedance by zone 1 of phase-to-earth distance protection is within the range determined by the setting 21Q1_PE_Imp_Op and 21Q1_PE_R_Op.

21Q1_PP_relay means that measured impedance by zone 1 of phase-to-phase distance protection is within the range determined by the setting 21Q1_PP_Imp_Op and 21Q1_PP_R_Op.

LoadEnch_Str (PE) means that load trapezoid characteristic for distance element is enabled and measured phase-to-earth impedance into the load area.

LoadEnch_Str (PP) means that load trapezoid characteristic for distance element is enabled and measured phase-to-phase impedance into the load area.

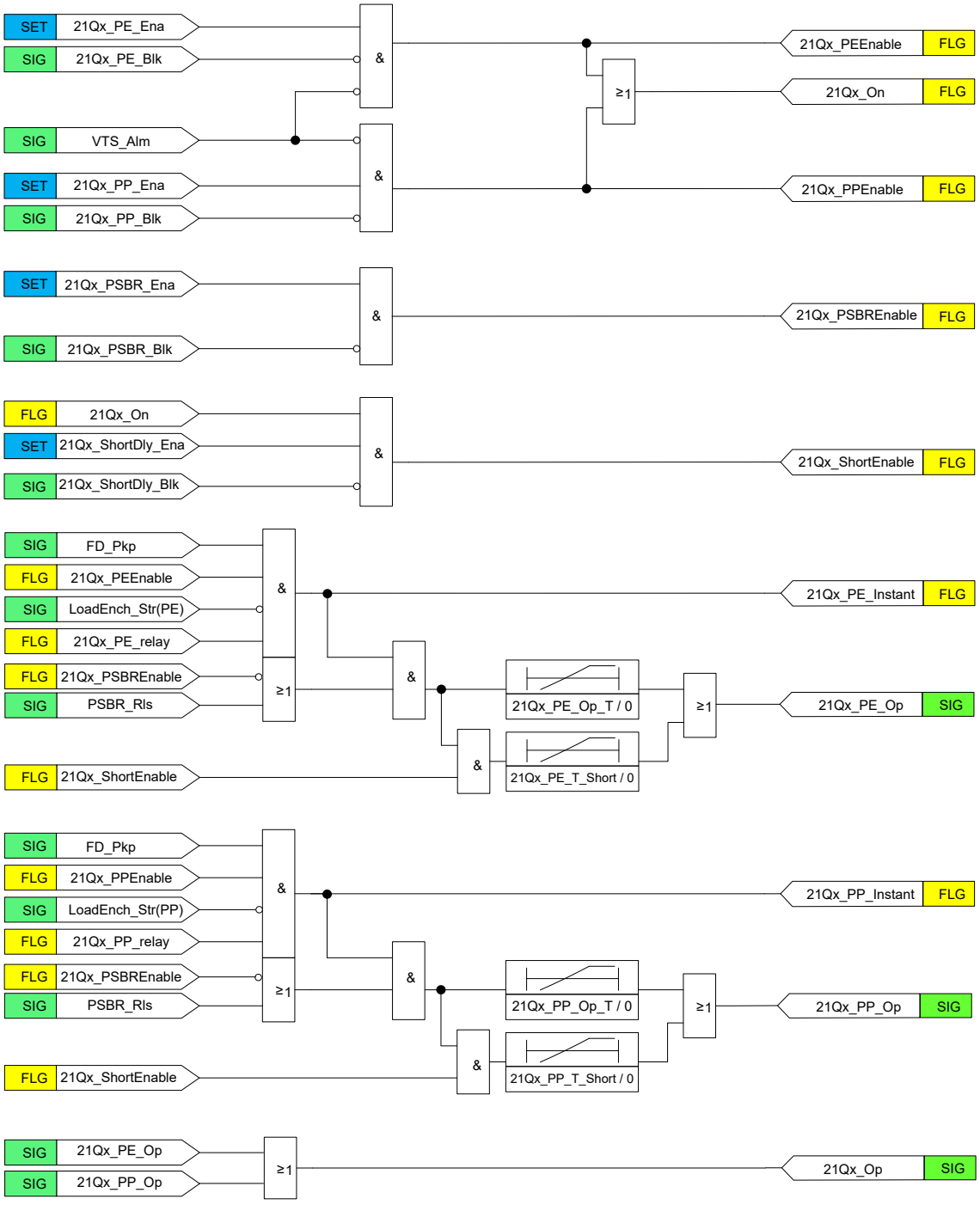


Figure 3.7.9 Logic diagram of distance protection (Quad zone x)

Where:

x=2,3,4,5

21Qx_PE_relay means that measured impedance by zone x of phase-to-earth distance protection is within the range determined by the setting 21Qx_PE_Imp_Op and 21Qx_PE_R_Op.

21Qx_PP_relay means that measured impedance by zone x of phase-to-phase distance protection

is within the range determined by the setting 21Qx_PP_Imp_Op and 21Qx_PP_R_Op.

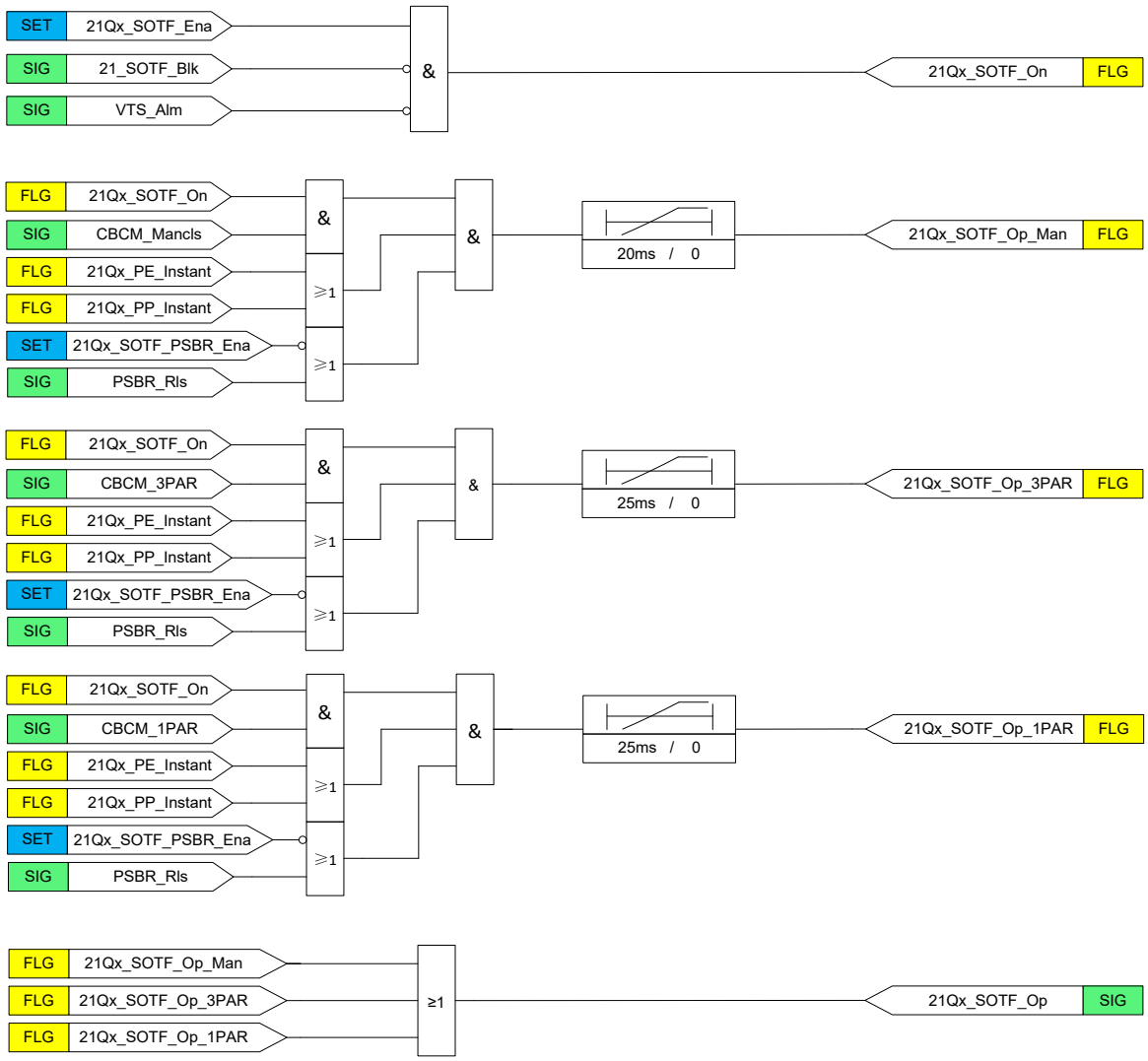


Figure 3.7.10 Logic diagram of Quad distance protection (SOTF)

Where:

x=1,2,3,4,5

CBCM_Mancls: is the signal of Manual closing signal for SOTF logic

CBCM_1PAR: is the signal of 1-pole reclosing signal for SOTF logic

CBCM_3PAR: is the signal of 3-pole reclosing signal for SOTF logic

3.7.3.5 Settings

Table 3.7-6 21Q Settings

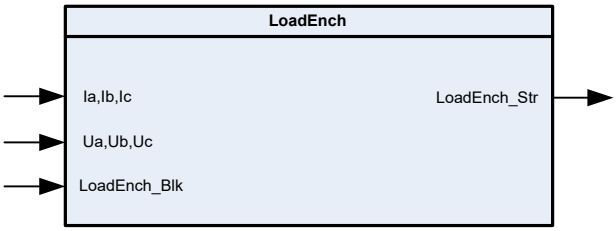
NO	Name	Range	Unit	Step	Default	Description
1	21Qx_Dir_Mod	0 or 1	-	1	0	Direction option for zone x of distance protection (x=1,2, 3, 4, 5) 0: Forward 1: Reverse
2	21Qx_PE_Ena	0 or 1	-	1	0	Enabling/disabling zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
3	21Qx_PP_Ena	0 or 1	-	1	0	Enabling/disabling zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
4	21Qx_PSBR_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance protection controlled by PSBR (x=1, 2, 3, 4, 5) 0: disable 1: enable
5	21Qx_ShortDly_Ena	0 or 1	-	1	0	Enabling/disabling fixed accelerate zone x of distance protection (x=1, 2, 3, 4, 5) 0: disable 1: enable
6	21Qx_SOTF_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance SOTF protection (x=1, 2, 3, 4, 5) 1: enable 0: disable
7	21Qx_SOTF_PSBR_Ena	0 or 1	-	1	0	Enabling/disabling zone x of distance SOTF protection controlled by PSBR (x=1, 2, 3, 4, 5) 1: enable 0: disable

NO	Name	Range	Unit	Step	Default	Description
8	21Qx_ZAng	10~89	deg	0.01	85	Phase angle of positive-sequence impedance for zone x of distance protection (x=1, 2, 3, 4, 5)
9	21Qx_Kz	0~10.000	-	0.001	0.67	Zero-sequence compensation coefficient magnitude for zone x of distance protection (x=1, 2, 3, 4, 5)
10	21Qx_KzAng	0~360.00	deg	0.01	0	Zero-sequence compensation coefficient angle for zone x of distance protection (x=1, 2, 3, 4, 5)
11	21Qx_Ang_Alpha	5~45	deg	0.01	25	Angle of blinder in fourth quadrant for forward direction (x=1, 2, 3, 4, 5)
12	21Qx_Ang_Beta	0~85	deg	0.01	30	Angle of blinder in second quadrant for forward direction (x=1, 2, 3, 4, 5)
13	21Qx_X0Comp_Ang	0~30	deg	0.01	12	Zero sequence reactance compensation angle (x=1, 2, 3, 4, 5)
14	21Qx_PE_Imp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
15	21Qx_PE_R_Op	(0.05~500)/In	ohm	0.01	20	Resistance setting of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
16	21Qx_PE_Op_T	0.000~10.000	s	0.001	10	Time delay of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
17	21Qx_PE_T_ShortDly	0.000~10.000	s	0.001	10	Short time delay of zone x of phase-to-earth distance protection (x=1, 2, 3, 4, 5)
18	21Qx_PP_Imp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)
19	21Qx_PP_R_Op	(0.05~500)/In	ohm	0.01	20	Resistance setting of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)

NO	Name	Range	Unit	Step	Default	Description
20	21Qx_PP_Op_T	0.000~10.000	s	0.001	10	Time delay of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)
21	21Qx_PP_T_ShortDly	0.000~10.000	s	0.001	10	Short time delay of zone x of phase-to-phase distance protection (x=1, 2, 3, 4, 5)

3.7.4 Load Encroachment LoadEnch

3.7.4.1 Function Block



3.7.4.2 Signals

Table 3.7-7 LoadEnch Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	LoadEnch_Blk	Load trapezoid characteristic blocking input, it is triggered from binary input or programmable logic etc.

Table 3.7-8 LoadEnch Output Signals

NO.	Signal	Description
1	LoadEnch_Str	Measured impedance is inside the load area. If load trapezoid characteristic is enabled and measured impedance is inside the load area, LoadEnch_Str=1 If load trapezoid characteristic is disabled or measured impedance is outside the load area, LoadEnch_Str=0

3.7.4.3 Protection Principle

When distance protection is used to protect long, heavily loaded lines, the risk of encroachment of the load impedance into the tripping characteristic of the distance protection may exist. A load trapezoid characteristic for all zones is used to exclude the risk of unwanted fault detection by the distance protection during heavy load flow.

Operation criteria of phase to ground:

$$\begin{cases} -\varphi_{load} < Arg\dfrac{\dot{U}_{\Phi}}{\dot{I}_{\Phi}+\dot{K}\cdot 3\dot{I}_{0}} < \varphi_{load} \\ 180°-\varphi_{load} < Arg\dfrac{\dot{U}_{\Phi}}{\dot{I}_{\Phi}+\dot{K}\cdot 3\dot{I}_{0}} < 180°+\varphi_{load} \\ -90° < Arg(\dfrac{\dot{U}_{\Phi}}{I_{\Phi}+K\cdot 3I_{0}} - \left|\dfrac{U_{\Phi set}}{\dot{I}_{\Phi}+\dot{K}\cdot 3\dot{I}_{0}}\right|) < 90° \\ 90° < Arg(\dfrac{\dot{U}_{\Phi}}{I_{\Phi}+K\cdot 3I_{0}} + \left|\dfrac{U_{\Phi set}}{\dot{I}_{\Phi}+\dot{K}\cdot 3\dot{I}_{0}}\right|) < 270° \end{cases}$$

Operation criteria of phase to phase:

$$\begin{cases} -\varphi_{load} < Arg\dfrac{\dot{U}_{\Phi\Phi}}{\dot{I}_{\Phi\Phi}} < \varphi_{load} \\ 180°-\varphi_{load} < Arg\dfrac{\dot{U}_{\Phi\Phi}}{\dot{I}_{\Phi\Phi}} < 180°+\varphi_{load} \\ -90° < Arg(\dfrac{\dot{U}_{\Phi\Phi}}{\dot{I}_{\Phi\Phi}} - \left|\dfrac{U_{\Phi\Phi set}}{\dot{I}_{\Phi\Phi}}\right|) < 90° \\ 90° < Arg(\dfrac{\dot{U}_{\Phi\Phi}}{\dot{I}_{\Phi\Phi}} + \left|\dfrac{U_{\Phi\Phi set}}{\dot{I}_{\Phi\Phi}}\right|) < 270° \end{cases}$$

As shown below, if the measured impedance into the load area, distance elements need to be blocked.

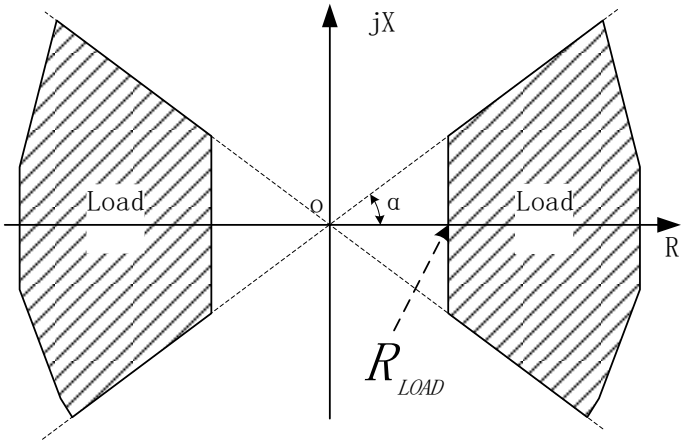


Figure 3.7.11 Distance element with load trapezoid

α : the load area angle, set by the setting LoadEnch_phi

R_{LOAD} : the minimum load resistance, set by the setting LoadEnch_R

These values are common for all zones.

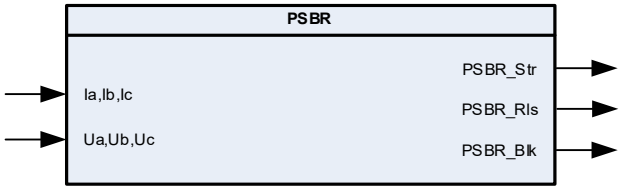
3.7.4.4 Settings

Table 3.7-9 Settings of LoadEnch

No.	Name	Range	Unit	Step	Default	Description
1	LoadEnch_Ena	0 or 1	-	1	0	Enabling/disabling load trapezoid characteristic 0: disable 1: enable
2	LoadEnch_phi	0~70	deg	0.01	30	Angle setting of load trapezoid characteristic, it should be set according to the maximum load area angle (φLoad_Max), φLoad_Max+5° is recommended.
3	LoadEnch_R	(0.05~500)/In	ohm	0.01	20	Resistance setting of load trapezoid characteristic, it should be set according to the minimum load resistance, 70%~90% minimum load resistance is recommended.

3.7.5 Power Swing Blocking Releasing PSBR

3.7.5.1 Function Block



3.7.5.2 Signals

Table 3.7-10 PSBR Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input

Table 3.7-11 PSBR Output Signals

NO.	Signal	Description
1	PSBR_Str	Start signal from PSBR
2	PSBR_Rls	PSBR operates to release distance protection
3	PSBR_Blk	Block signal from PSBR

3.7.5.3 Protection Principle

When power swing occurs on the power system, the impedance measured by the distance measuring element may vary from the load impedance area into the operating zone of the distance element. The distance measuring element may operate due to the power swing occurs in many points of interconnected power systems. To keep the stability of whole power system, tripping due to operation of the distance measuring element during a power swing is generally not allowed. Our distance protection adopts power swing blocking releasing to avoid maloperation resulting from power swing. In another word, distance protection is blocked all along under the normal condition and power swing when the respective logic settings are enabled. Only when fault (internal fault or power swing with internal fault) is detected, power swing blocking for distance protection is released by PSBR element.

Power swing blocking for distance element will be released if any of the following PSBR elements operates. Each distance zone elements has respective setting for selection this function.

1) Swing detector element (SD)

2) Unsymmetrical fault PSBR element (UF PSBR)

3) Symmetrical fault PSBR element (SF PSBR)

1. Swing detector element

If the device picked up before swing condition is met, PSBR will operate for 160ms.

This detection is based on measuring the voltage at power swing center, during power swing, swing condition is shown as below:

$$\begin{cases} -0.7U_N < U_{OS} < 0.7U_N \\ \Delta U_{OS} > 1V \\ U_1 > 18V \ \& \ U_2 < 3V \ \& \ 3U_0 < 8V \\ 3I_0 < I\_Line \ \& \ I_1 > \text{PSBR.I} \end{cases}$$

If operation condition is met, the swing detector will operate.

2. Unsymmetrical fault PSBR element

The operation criterion:

I0+I2>m×I1

The “m”, an empirical value, is internal fixed coefficient which can ensure operation during power swing with internal unsymmetrical fault, while no operation during power swing.

3. Symmetrical fault PSBR element

This detection is based on measuring the voltage at power swing center, during power swing, U1cosΦ will constantly change periodically.

$$U_{OS}=U1\times COS\Phi$$

Where:

Φ: the angle between positive sequence voltage and current

U1: the positive sequence voltage

1) Releasing element 1

During power swing, power swing center voltage U1cosΦ has the following characteristics: When electric potential phase angle difference between power supplies at two sides is 180o, U1cosΦ＝0 and change rate dU1cosΦ/dt is the maximum. When this phase angle difference is near 0, power swing center voltage change rate dU1cosΦ/dt is the minimum. During short circuit, U1cosΦ remains unchanged and dU1cosΦ/dt＝0.

2) Releasing element 2

For these reasons, the method to release distance protection on condition that power swing center voltage U1cosΦ is less than a setting and after a short delay can be used as symmetric fault discriminating element. This element can accurately differentiate power swing and 3-phase short circuit fault, and constitute a complete power swing blocking scheme with other elements. The element to open distance protection if U1cosΦ is less than a certain setting and after a delay is easy to realize and has short delay, and can trip fault more quickly and accurately trip 3-phase short circuit fault during power swing.

- when -0.03UN<UOS<0.08UN, the SF PSBR element will operate after 150ms.
- when -0.1UN<UOS<0.25UN, the SF PSBR element will operate after 500ms.

3) Releasing element 3

To reduce the time delay for SF PSBR element during power swing, the change rate of voltage at power swing center is also used which can release SF PSBR element quickly for the fault occurred during power swing. The typical release time is less than 60ms.

3.7.5.4 Logic

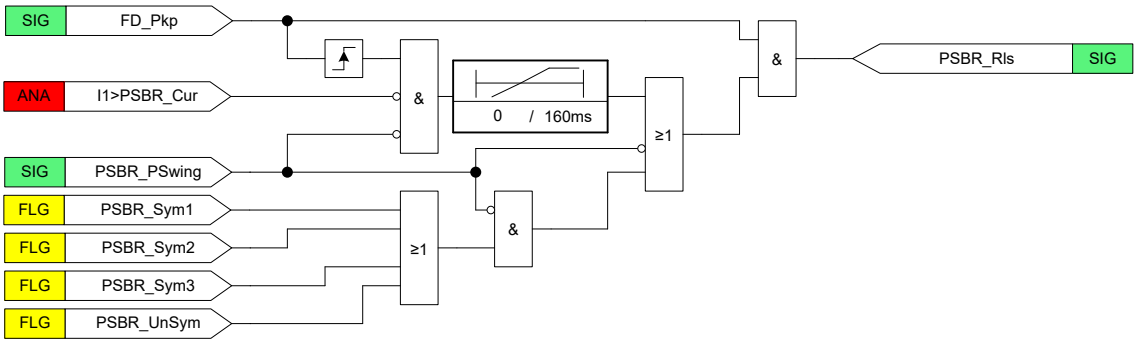


Figure 3.7.12 Logic diagram of PSBR

3.7.5.5 Settings

Table 3.7-12 Settings of PSBR

No.	Name	Range	Unit	Step	Default	Description
1	PSBR_Cur	(0.05~30.00) ×In	A	0.01	20	Current setting for power swing blocking

3.8 Out-of-Step Protection 78O

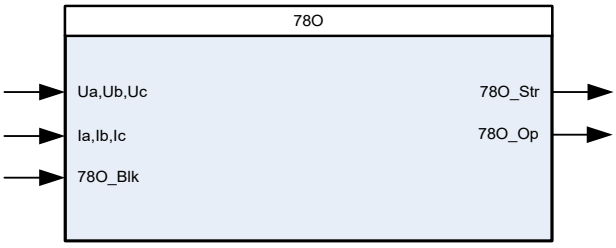
3.8.1 Overview

When the power system loses synchronism, out-of-step protection 78O can automatically disconnect the power plant and the associated load from the power system to prevent damage.

78O use voltage angle criteria and it can adapt to a variety range of power grid structures and operation mode. 78O has the following characteristics:

- Using the criterion of voltage angle, 78O can accurately identifies the system oscillation. The function can operate reliably and correctly if the oscillation period is less than 160ms.
- 78O is not affected by the fault, for example, three-phase symmetrical fault and its recovery, converted fault and power swing which does not lead to system out-of-step.
- When the system is in open-phase operation mode, 78O will not operate even if the system is out-of-step. When the system returns to full-phase operation mode and is still in out-of-step condition, 78O will operate.
- The 78O function can identify the system power angle and avoid disconnecting the circuit breaker when the angle difference is around 180 °.

3.8.1.1 Function Block



3.8.1.2 Signals

Table 3.8-1 78O Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	Ia,Ib,Ic	Three-phase current input
3	78O_Blk	Blocking signal of 78O

Table 3.8-2 78O Output Signals

NO.	Signal	Description
1	78O_Str	Start signal from 78O
2	78O_Op	Operation signal from 78O

3.8.2 Protection Principle

3.8.2.1 Start of the Function

By calculating the voltage at oscillation center of the transmission line, the function can detect whether the system is in power swing or symmetry fault condition.

$$\begin{cases} -0.7Un < U_1\cos(\varphi) < 0.7Un \\ 3U_1 > 18V \wedge 3U_2 < 8V \wedge 3U_0 < 8V \\ 3I_0 < 300A \wedge I_1 > 500A \end{cases}$$

Where:

Un is the rated voltage.

U_1 is positive-sequence voltage.

U_2 is negative-sequence voltage.

U_0 is zero-sequence voltage.

I_1 is positive-sequence current.

φ is the angle difference between positive-sequence voltage and current.

The function will operate when the criterion is met and last for at least 25ms.

3.8.2.2 Power Swing Detection

The function detects the out-of-step oscillation according to the change of the voltage at oscillation center, and simultaneously evaluates the amplitude and period of oscillation and the power angle to decide whether to operate.

Calculation of the voltage of power swing center can be done through the following fomula:

$$U_{\cos} = U_1\cos(\varphi + \delta)$$

Where:

φ is the angle difference between positive-sequence voltage and positive-sequence current.

δ is the line positive-sequence impedance angle, set by the setting LinAng.

$\mathrm{U}_{\cos}$ have the following waveforms (converted to per unit value):

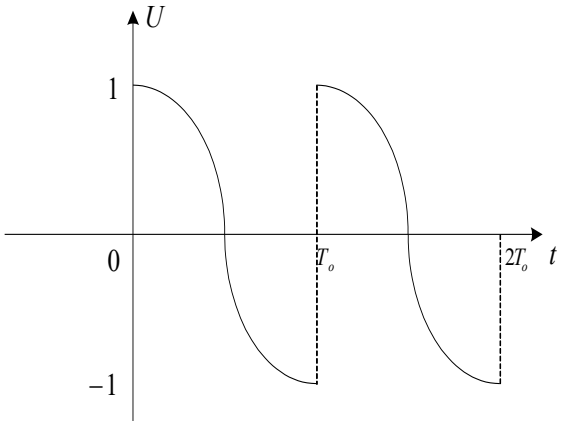


Figure 3.8.1 Voltage at Accelerate Side

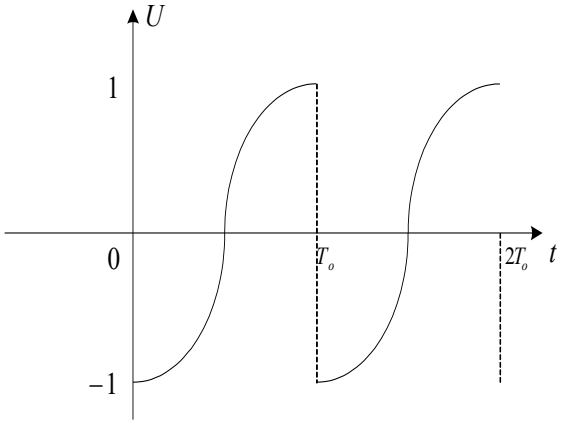


Figure 3.8.2 Voltage at Decelerate Side

The two voltage waveforms above satisfy the following equations:

$$U_{\cos\_accel}(t) = \cos\left(\frac{\pi}{T_0}t\right)$$

$$U_{\cos\_decel}(t) = -\cos\left(\frac{\pi}{T_0}t\right)$$

Where:

T_0 is the oscillation period.

Divide the waveform of U_{cos} into 6 areas within one oscillation period:

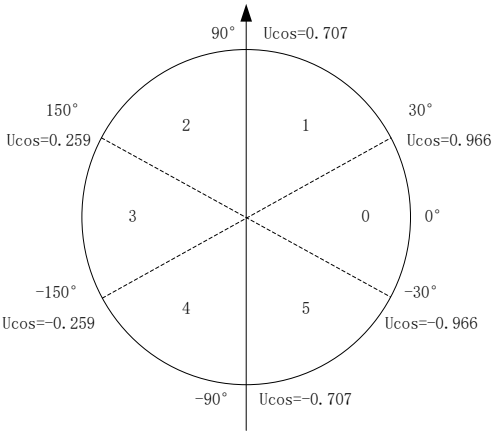


Figure 3.8.3 Phase Division of Vector Diagram

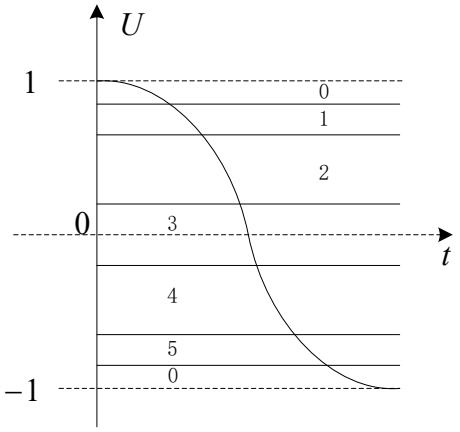


Figure 3.8.4 Division of Waveform

Where in area 0: $|U_{cos}| > 0.966$

Area 1: $0.707 < U_{cos} < 0.966$

Area 2: $0.259 < U_{cos} < 0.707$

Area 3: $-0.259 < U_{cos} < 0.259$

Area 4: $-0.707 < U_{cos} < -0.259$

Area 5: $-0.966 < U_{cos} < -0.707$

U_{cos} falls into each area for an equal time $T_0/6$ in one oscillation period.

In the accelerate side, U_{cos} swing across the areas in the following order:

$$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 0$$

In the decelerate side, U_{cos} swing across the areas in the following order:

$$0 \rightarrow 5 \rightarrow 4 \rightarrow 3 \rightarrow 2 \rightarrow 1 \rightarrow 0$$

The 78O function records the history of areas that U_{cos} once passed and compare it with the above order. If the order is the same, the function's internal flag Pswing_Cond will be set to 1.

High speed tripping:

In some situations, 78O is required to operate as soon as possible when a loss of synchronization is detected, for which the function provides a high-speed tripping criterion:

The function simply detects if U_{cos} have crossed through area 3 in the above order, for example:

$$5 \rightarrow 4 \rightarrow 3 \rightarrow 2$$

And the absolute value of U_{cos} is greater than 10V.

If the two conditions are met, the function's internal flag Pswing_Inst_Cond will be set to 1.

Notice that high speed trip will only be enable if the setting 78O_InstTrp_Ena is set to 1.

3.8.2.3 Power Swing Center Locating and Direction Determination

Power swing center location determination criterion:

When U_{cos} falls into area 3 and the positive-sequence voltage is below the threshold voltage setting 78O_Op_LowVol for 10ms, the function considered the swing center to be somewhere within the protection zone and the function's internal flag 78O_Pswing_Loc will be set to 1.

Power swing center direction determination criterion:

When the absolute value of U_{cos} is less than 0.1Un, the power swing center is considered to be in the forward direction if the phase angle $30° < \mathrm{Angle}(U_1/I_1) < 150°$, and reverse direction if $-150° < \mathrm{Angle}(U_1/I_1) < -30°$.

Notice that direction criterion will be automatically satisfied if the direction determination is not enable. And if the setting 78O_Dir_Ena is set to 1, the direction criterion will also be satisfied if 78O_Dir_Mod is set to 0.

3.8.2.4 Tripping Angle Determination

When all the other operation conditions are met, if U_{cos} falls into area 3 while the phase angle $150° < \mathrm{Angle}(U_1/I_1) < 210°$, tripping signal will be blocked until U_{cos} cross through area 3.

3.8.2.5 Power Swing Cycle Counting

The threshold setting of oscillation cycle number 78O_Op_Pswing_Num is an important parameter in the function. 78O will need more than the setting number of swing cycles counting to operate. 78O_Op_Pswing_Num should be set to 1 if fast disconnecting is required; 78O_Op_Pswing_Num should be set to 3 or 4 in order to cooperate with the out-of-step protection of adjacent lines, which ensures that 78O will not operate before the disconnection of the adjacent line; After the out-of-step oscillation, it is hoped that the out-of-step system can be pulled back into synchronization, in this case, 78O_Op_Pswing_Num should be set to 5 to 10 which can leave enough time for the system recovery. In short, the choice of 78O_Op_Pswing_Num should be based on the actual situation of the system and the cooperation with other protection device.

3.8.2.6 Abnormal Condition Blocking of the Function

78O will be blocked in the following conditions:

- When three-phase fault occurs in the power system.
- When the zero-sequence or negative-sequence voltage or current is in abnormal condition.
- When U_{cos} stays in any area for more than 1.5 seconds.

Notice that all the internal flag will be reset if abnormal condition is detected and the oscillation cycle counting will be set to 0 too.

3.8.3 Logic

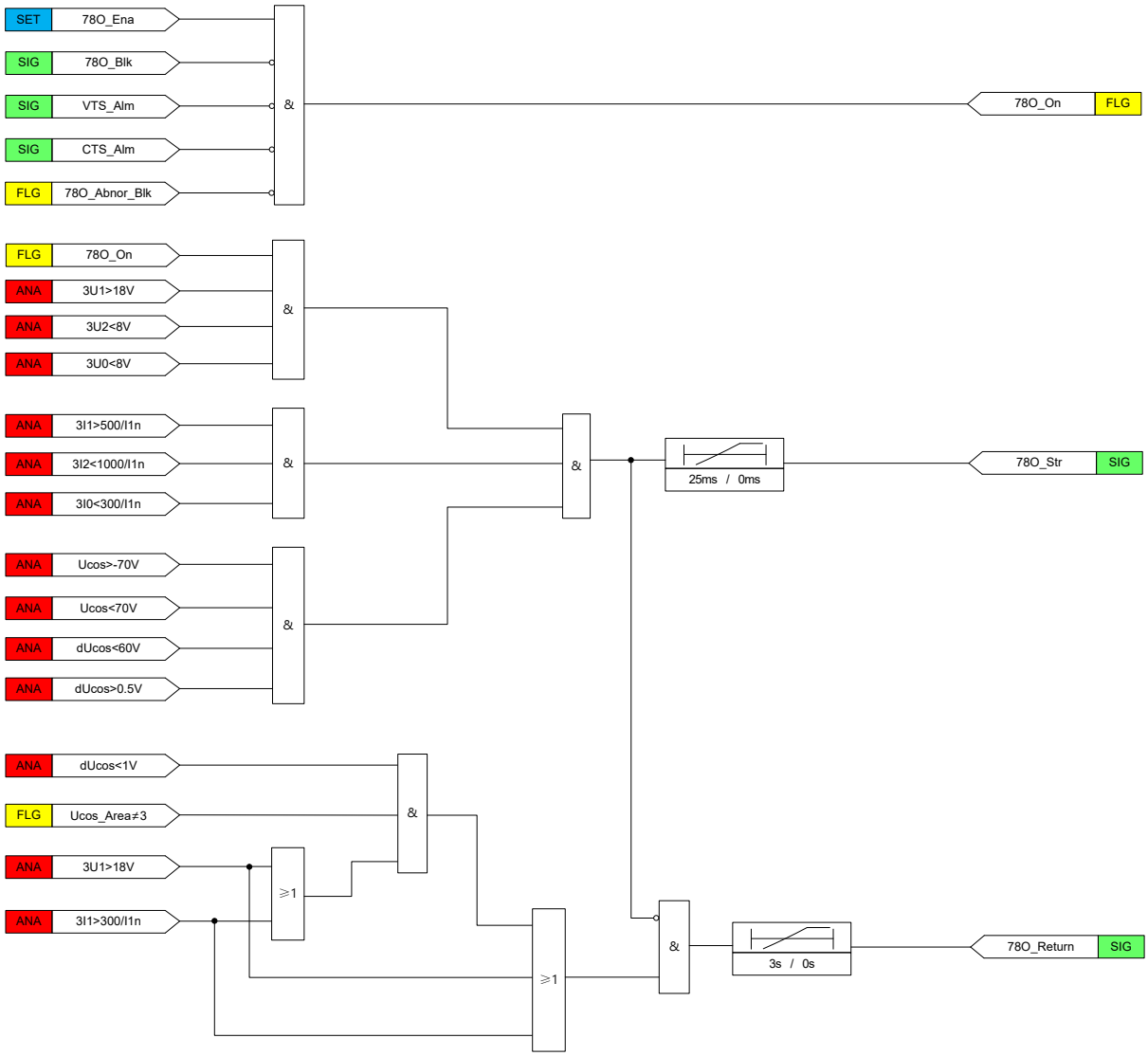


Figure 3.8.5 78O Start

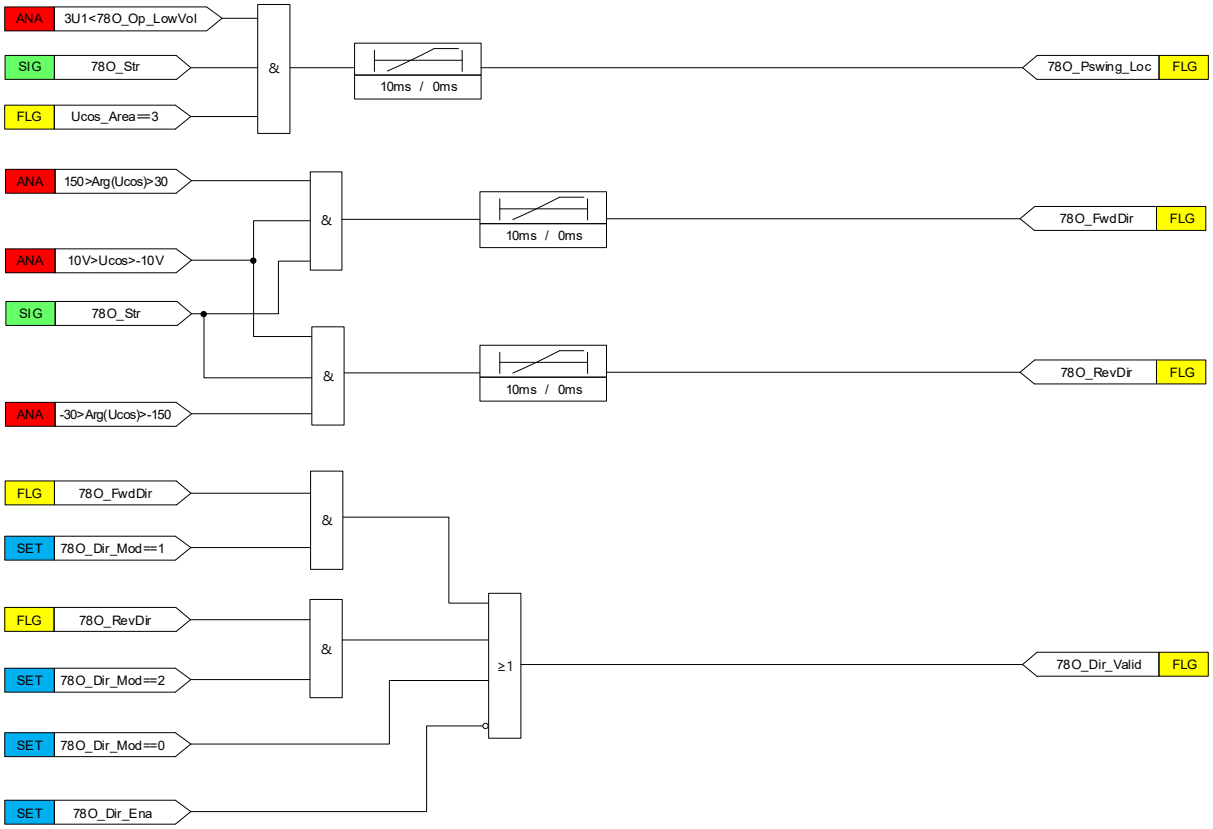


Figure 3.8.6 78O Direction element

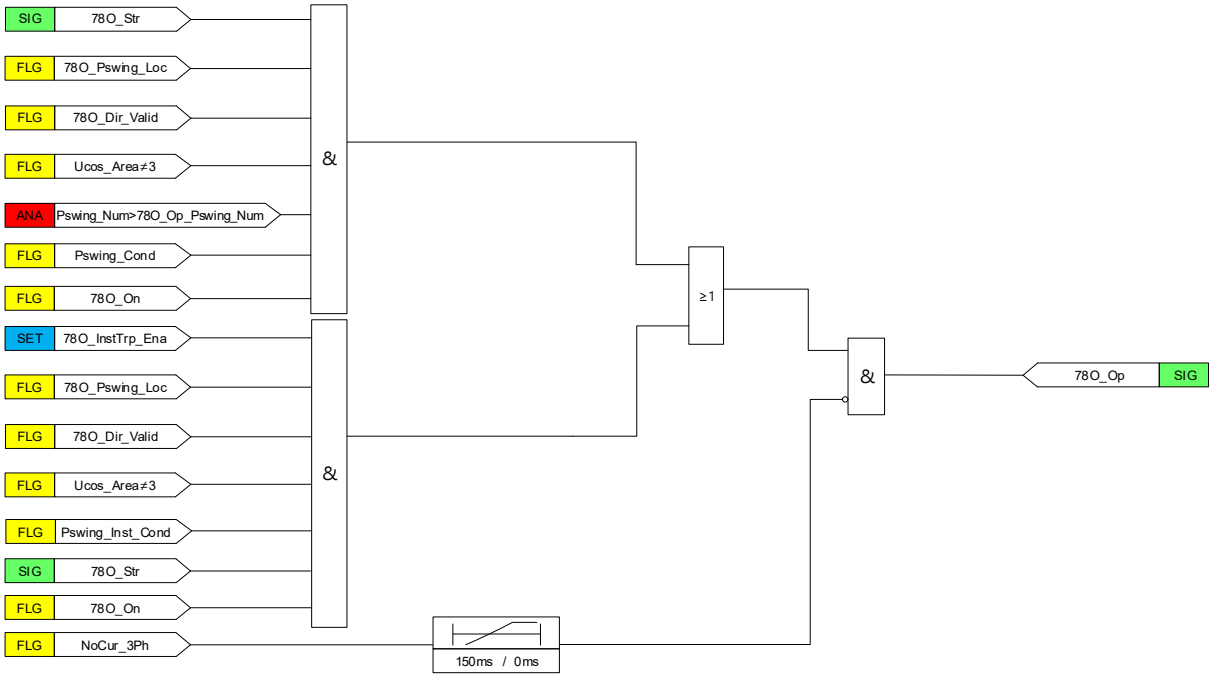


Figure 3.8.7 78O Operation

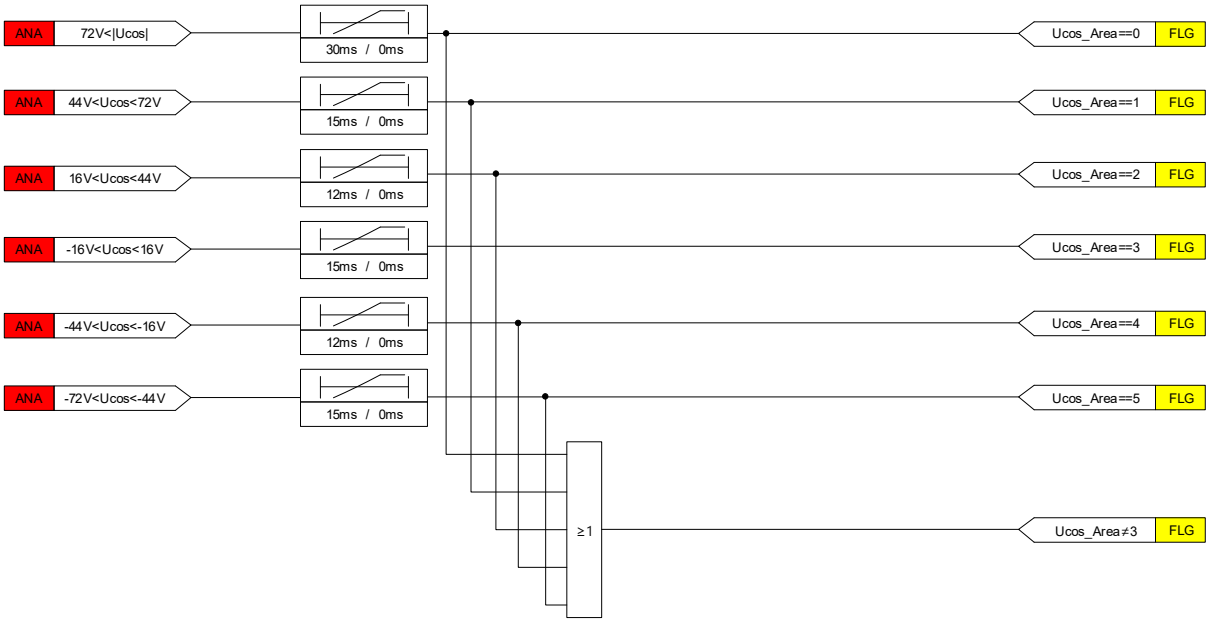


Figure 3.8.8 78O Ucos Area Detection

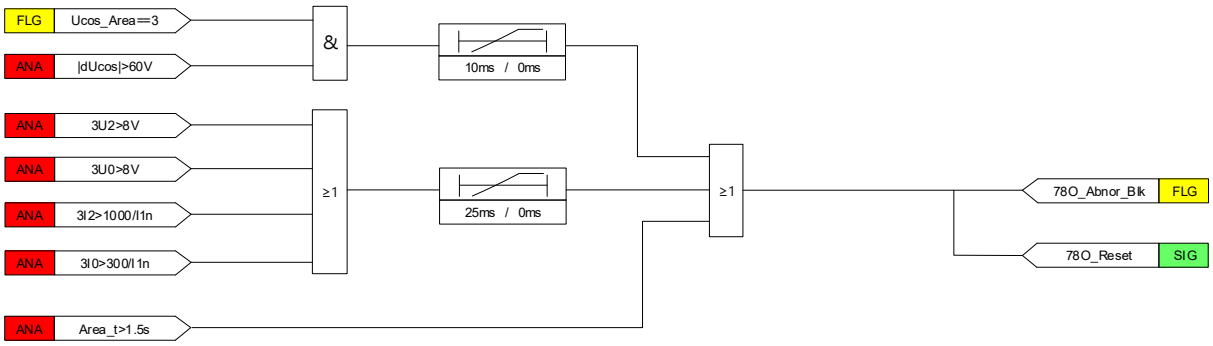


Figure 3.8.9 Abnormal Condition Blocking of 78O

3.8.4 Settings

Table 3.8-3 78O Settings

NO	Name	Range	Unit	Step	Default	Description
1	78O_Ena	0 or 1	-	1	0	Enabling/disabling of out-of-step protection: 0: disable 1: enable
2	78O_InstTrp_Ena	0 or 1	-	1	0	Enabling/disabling high speed trip of out-of-speed protection 0: disable 1: enable
3	78O_Dir_Ena	0 or 1	-	1	0	Enabling/disabling direction determination of out-of-step protection: 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
4	78O_Op_LowVol	0.00~1.00	Un	0.01	0.3	Low voltage threshold of out-of-step protection
5	78O_Op_Pswing_Num	1~15	-	1	3	Threshold number of power swing cycle counting
6	78O_Dir_Mod	0, 1, 2	-	1	1	Direction option for out-of-step protection: 0: Non-Directional 1: Forward 2: Reverse

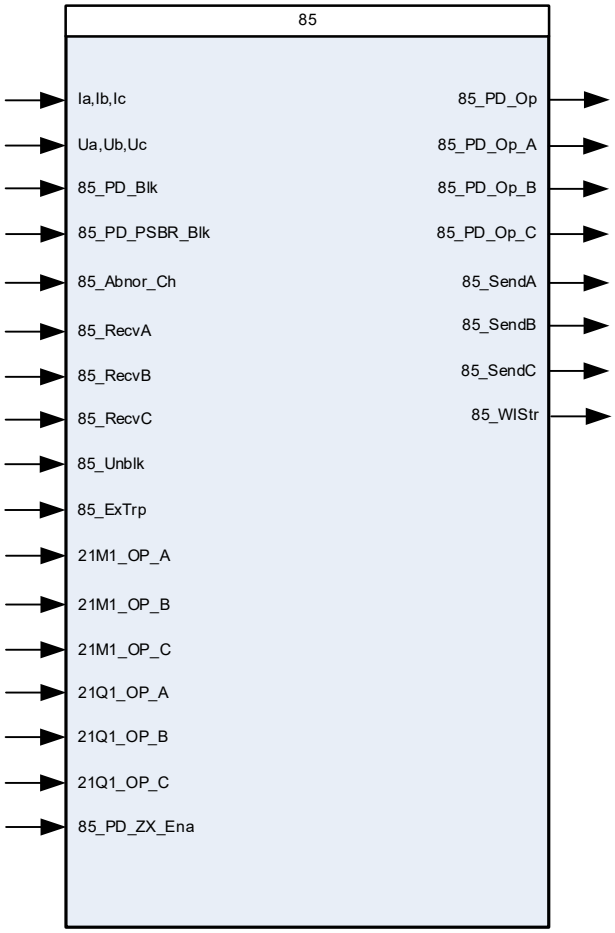
3.9 Scheme communication logic for distance protection 85

3.9.1 Overview

The instant distance protection with underreaching setting is impossible to isolate the fault at remote end of the line, while distance protection with overreaching setting needs a time delay to grade with downstream protection to maintain discrimination. Pilot distance protection that exchanges distance protection information at both ends of the line can remove the fault within this line quickly, and will not operate for external fault.

Pilot protection requires communication channel to exchange the protection information at both ends. The channel may be dedicated or multiplexed channel through optical fiber or any other communication media.

3.9.1.1 Function Block



3.9.1.2 Signals

Table 3.9-1 Pilot distance protection Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	85_PD_Blk	Block signal of pilot distance protection
4	85_PD_PSBR_Blk	Blocking power swing blocking releasing of pilot distance protection
5	85_Abnor_Ch	Input signal of indicating that pilot channel is abnormal for pilot distance protection
6	85_RecvA	Input signal of receiving permissive signal via pilot channel for pilot distance protection(only for three-phase command scheme) , or input signal of receiving permissive signal of A-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)

NO.	Signal	Description
7	85_RecvB	Input signal of receiving permissive signal of B-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)
8	85_RecvC	Input signal of receiving permissive signal of C-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)
9	85_Unblk	Unblocking signal of pilot distance protection
10	85_ExTrp	Input signal of initiating sending permissive signal from external tripping signal for pilot distance protection
11	21M1_Op_A	Operation signal from phase A from 21M zone 1
12	21M1_Op_B	Operation signal from phase B from 21M zone 1
13	21M1_Op_C	Operation signal from phase C from 21M zone 1
14	21Q1_Op_A	Operation signal from phase A from 21Q zone 1
15	21Q1_Op_B	Operation signal from phase B from 21Q zone 1
16	21Q1_Op_C	Operation signal from phase C from 21Q zone 1
17	85_PD_ZX_Ena	Input signal of enabling zone extension

Table 3.9-2 Pilot distance protection Output Signals

NO.	Signal	Description
1	85_PD_Op	Operation signal from pilot distance protection
2	85_PD_Op_A	Operation signal from phase A
3	85_PD_Op_B	Operation signal from phase B
4	85_PD_Op_C	Operation signal from phase C
5	85_SendA	Output signal of sending permissive signal of pilot distance protection(only for three-phase command scheme) , or output signal of sending A-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
6	85_SendB	Output signal of sending B-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
7	85_SendC	Output signal of sending C-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
8	85_WIStr	Start signal of weak infeed logic of pilot distance protection

3.9.2 Protection Principle

Pilot distance protection determines whether it will send the signal to the remote end according to the discrimination result of the distance element or direction element. Pilot distance protection can

be divided into permissive scheme and blocking scheme according to whether the signal sent is used to permit tripping or block tripping. For permissive scheme, it can be divided into overreaching mode or underreaching mode according to the setting of distance element and scheme selected, furthermore, it will provide the unblocking scheme as auxiliary function. For overreaching mode, current reversal logic and weak infeed logic are available for parallel line operation and weak power source situation respectively.

Pilot distance protection can be enabled or disabled by input signals, logic setting and blocking signal, as shown in Figure 3.9.1.

Figure 3.9.1 Enabling/disabling logic of pilot distance protection

Pilot distance protection receives and sends signals via pilot channel, and the logic of receiving signal is shown in Figure 3.9.2.

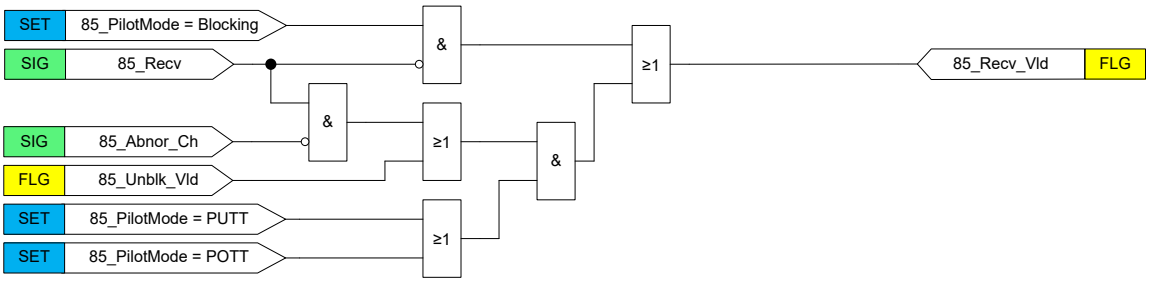


Figure 3.9.2 Logic diagram of receiving signal

Pilot distance protection has the following application modes:

3.9.2.1 Impedance Characteristic

An independent pilot zone distance protection is used for PUTT and POTT scheme. There is also a reverse pilot distance element available as an option for application of POTT on weak power source system.

The operation characteristic of pilot zone is same as that of zone 2, including mho and quadrilateral characteristic.

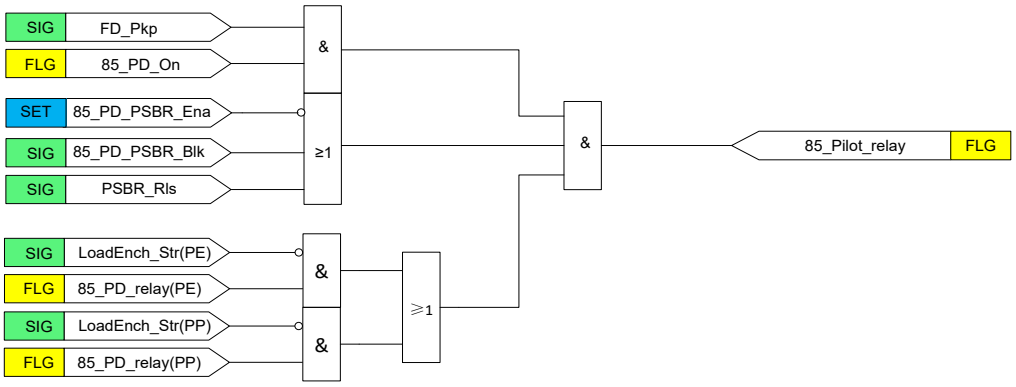


Figure 3.9.3 Logic diagram of pilot distance zone

Where:

PSBR_Rls: is the signal of power swing blocking releasing signal

85_PD_relay(PE) means that measured impedance by phase-to-earth pilot distance protection is within the range determined by the setting 85_PD_MhoImp_Op (Mho characteristic) OR 85_PD_QuadImp_Op (Quad characteristic).

85_PD_relay(PP) means that measured impedance by phase-to- phase pilot distance protection is within the range determined by the setting 85_PD_MhoImp_Op (Mho characteristic) OR 85_PD_QuadImp_Op (Quad characteristic).

LoadEnch_Str (PE) means that load trapezoid characteristic for distance element is enabled and measured phase-to-earth impedance into the load area.

LoadEnch_Str (PP) means that load trapezoid characteristic for distance element is enabled and measured phase-to-phase impedance into the load area.

When an internal fault occurs, distance protection at weak source end may not operate due to small fault current. Thus, a reverse distance element is provided to coordinate with the independent pilot distance protection to implement weak infeed logic, ensure pilot distance protection can operate to send signal or trip in the weak end.

3.9.2.2 Zone Extension

When pilot channel failure or no pilot scheme protection is provided, the pilot distance protection is out of service. The fault outside zone 1 can only be cleared by zone 2 with a time delay. It cannot ensure that all faults are cleared instantaneously within protected line. Zone extension can clear the fault instantaneously within the whole line as a supplement of pilot distance protection. Different with pilot distance protection, zone extension can also operate for external close up fault in parallel line, but power supply can be restored by AR. So, zone extension should be blocked when AR is out of service and is not ready.

In order to prevent too many lines from disconnecting with system due to zone extension operate, when the circuit breaker is closed into permanent fault, zone extension should be blocked when AR operates. For transient fault, the line can be into service again after AR operates successfully. For permanent fault in either local line or parallel line, distance protection with a time delay will

operate.

Zone extension uses the setting of pilot distance zone (85 Pilot), and its operation characteristic can be Mho or Quad. And the logic of zone extension is shown in Figure 3.9.4.

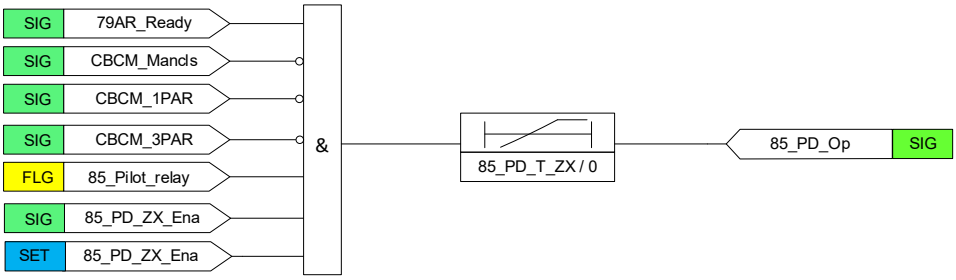


Figure 3.9.4 Logic diagram of zone extension

3.9.2.3 Permissive Underreaching Transfer Trip (PUTT)

Distance elements zone 1 (Z1) with underreaching setting and pilot zone (ZPilot) with overreaching setting are used for this scheme. Z1 element will send permissive signal to the remote end and release tripping after Z1 time delay expired. After receiving permissive signal with ZPilot element pickup, a tripping signal will be released.

The signal transmission element for PUTT is set according to underreaching mode, so current reversal need not be considered.

For PUTT, there may be a dead zone under weak power source condition. If the fault occurs outside Z1 zone at strong power source side, Z1 at weak power supply side may not operate to trip and transmit permissive signal, and pilot distance protection will not operate. Therefore, the system fault can only be removed by Z2 at strong power source side with time delay.

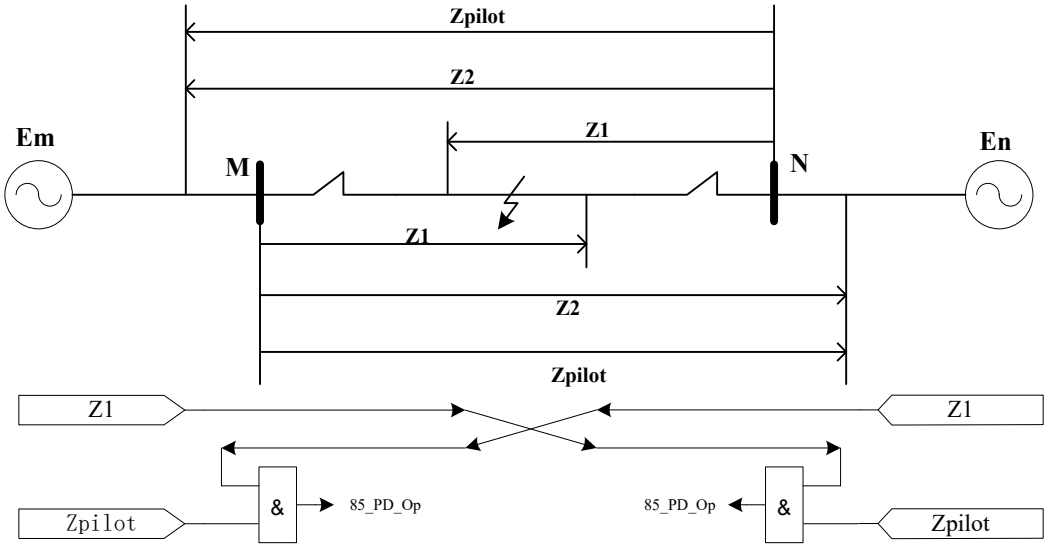


Figure 3.9.5 Simple schematic of PUTT

Pilot distance protection always adopts pilot channel 1, and the logic of PUTT is shown in Figure 3.9.6.

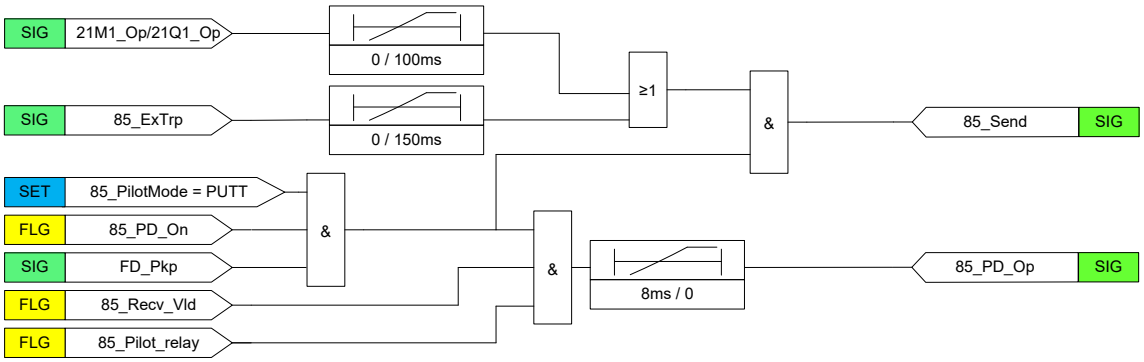


Figure 3.9.6 Logic diagram of pilot distance protection (PUTT)

3.9.2.4 Permissive Overreaching Transfer Trip (POTT)

ZPilot will send permissive signal to remote end once it picks up and release tripping signal upon receiving permissive signal from the remote end.

When POTT is applied on parallel lines arrangement and the ZPilot setting covers 50% of the parallel line, there may be a problem under current reversal condition, settings for current reversal condition should be considered.

Under weak power source condition, the problem of dead zone at weak power source end is eliminated by the weak infeed logic.

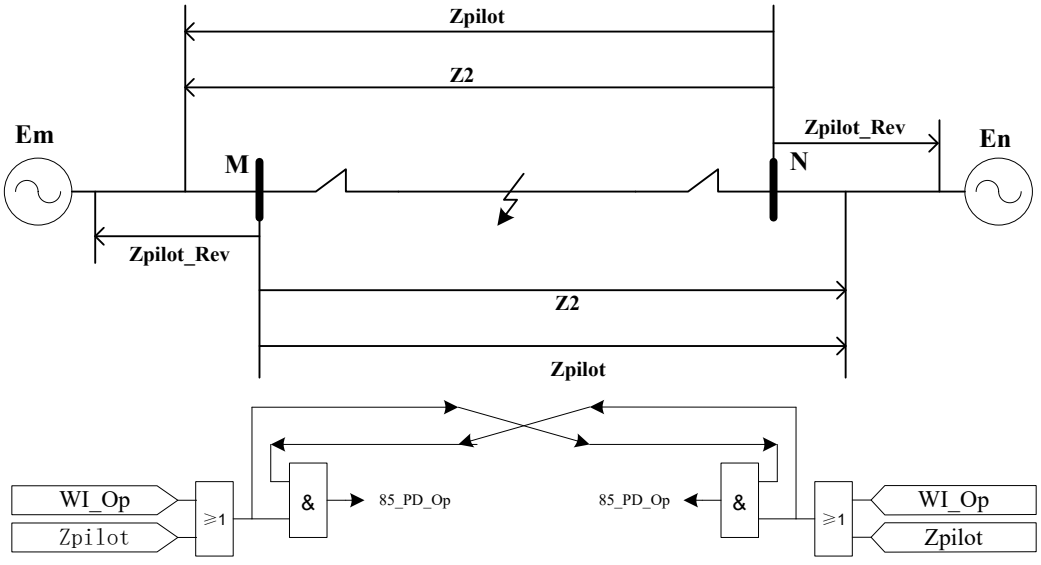


Figure 3.9.7 Simple schematic of POTT

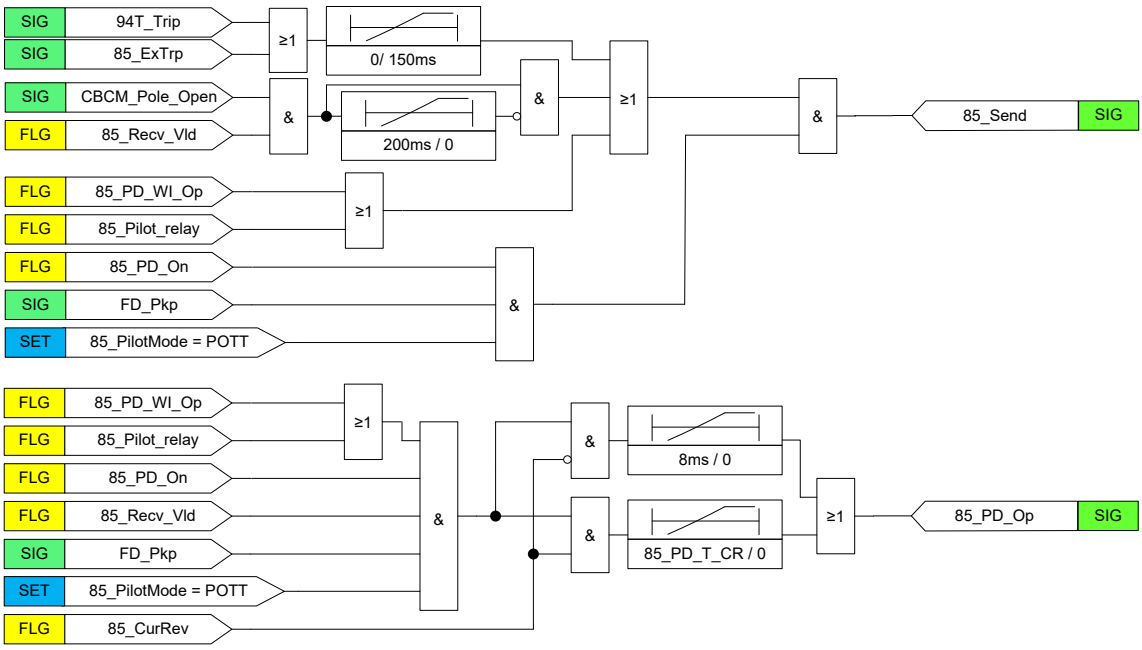


Figure 3.9.8 Logic diagram of pilot distance protection (POTT)

3.9.2.5 Blocking

Permissive scheme has high security, but it relies on pilot channel seriously. Pilot distance protection will not operate when there is an internal fault with abnormal channel. Blocking scheme could be considered as an alternative.

Blocking scheme takes use of pilot distance element Zpilot operation to terminate sending of blocking signal. Blocking signal will be sent once fault detector picks up without pilot zone Zpilot operation. Pilot distance protection will operate with a short time delay if pilot distance element operates and not receiving blocking signal after timer expired.

The setting of pilot zone element Zpilot in Blocking scheme is overreaching, so current reversal condition should be considered. However, the short time delay of pilot distance protection has an enough margin for current reversal, that this problem has been resolved.

The short time delay must consider channel delay and with a certain margin to set. As shown in Figure 3.9.9, an external fault happens to line MN. The fault is behind the device at M side, for blocking scheme, the device at M side will send blocking signal to the device at N side. If channel delay is too long, the device at side N has operated before receiving blocking signal. Hence, the time delay of pilot distance protection adopted in blocking scheme should be set according to channel delay.

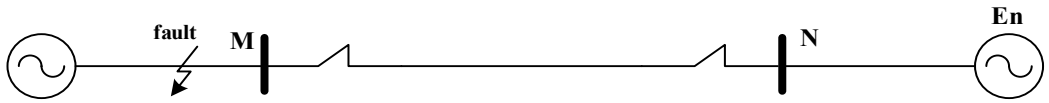


Figure 3.9.9 Simple schematic of system fault

For blocking scheme, pilot distance protection will operate when there is an internal fault with

abnormal channel, however, it is possible that pilot distance protection issues an undesired trip when there is an external fault with abnormal channel.

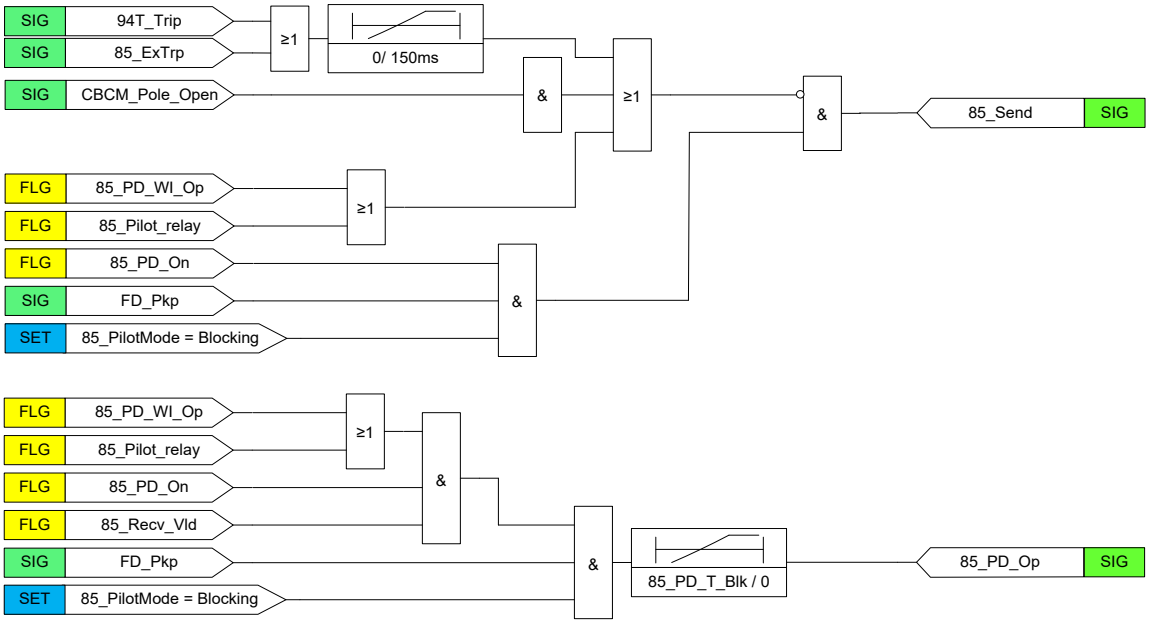


Figure 3.9.10 Logic diagram of pilot distance protection (Blocking)

Current reversal logic is only used for permissive scheme. For blocking scheme, the time delay of pilot distance protection has enough margin for current reversal, so current reversal need not be considered.

3.9.2.6 Unblocking

Permissive scheme will trip only when it receives permissive signal from the remote end. However, it may not receive permissive signal from the remote end when pilot channel fails. For this case, pilot distance protection can adopt unblocking scheme. Under normal conditions, the signaling equipment works in the pilot frequency, and when the device operates to send permissive signal, the signaling equipment will be switched to high frequency. While pilot channel is blocked, the signaling equipment will receive neither pilot frequency signal nor high frequency signal. The signaling equipment will provide a contact to the device as unblocking signal. When the device receives unblocking signal from the signaling equipment, it will recognize channel failure, and unblocking signal will be taken as permissive signal temporarily.

The unblocking function can only be used together with PUTT and POTT.

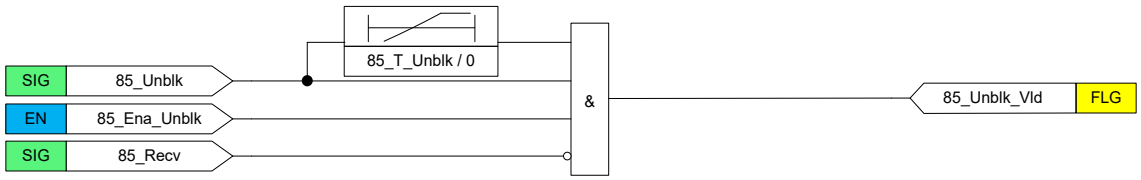


Figure 3.9.11 Logic diagram for unblocking

3.9.2.7 Current Reversal

When there is a fault in one of the parallel lines, the direction of the fault current may change during the sequence tripping of the circuit breaker at both ends as shown in Figure 3.9.12: When a fault occurs on line C–D near breaker D, the fault current through line A-B to D will flow from A to B. When breaker D is tripped, but breaker C is not tripped, the fault current in line A-B will then flow from B to A. This process is the current reversal.

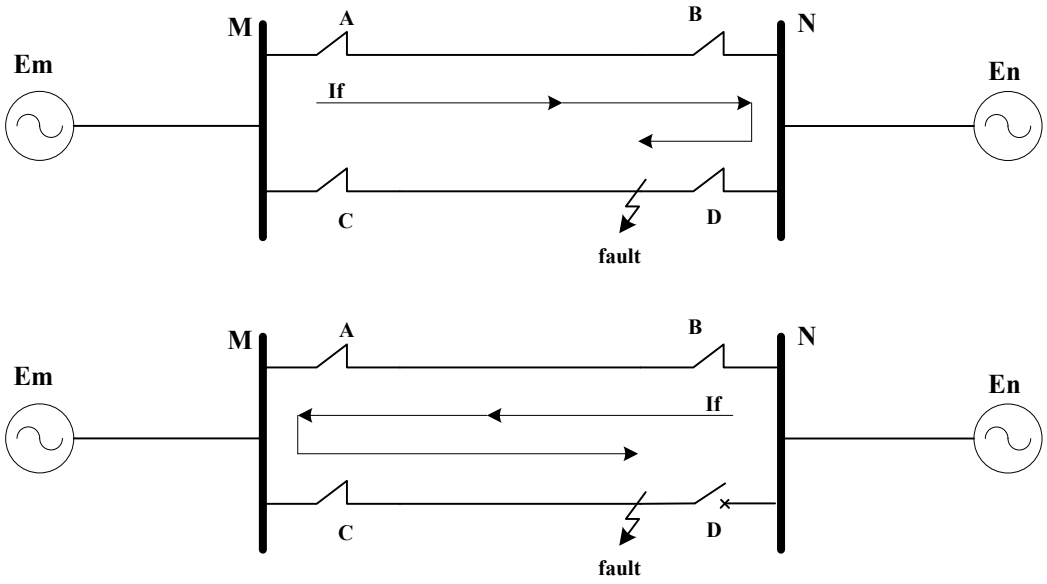


Figure 3.9.12 Current reversal

Referring to above figure, when pilot reverse zone pickup without pilot forward zone pickup, the current reversal blocking logic is enabled after t1 delay.

The time delay of t1 (85_T_DPU_CR) shall be set the shortest possible but allowing sufficient time for pilot forward zone pickup, generally set as 3ms.

Once the current reversal logic is enabled, the healthy line device B transfer tripping is blocked. The logic will be disabled by either the drop-off of pilot reverse zone or the pickup of pilot forward zone. A time delay t2 (85_T_DDO_CR) is required to avoid maloperation for the case that the pilot forward zone (or forward element of pilot directional earth-fault protection) of device B picks up before the pilot reverse zone drops off. Considering the channel propagation delay and the pickup and drop-off time difference of pilot forward zone (or pilot directional earth-fault element) with margin, t2 is generally set as 50ms.

Because the time delay of pilot distance protection has an enough margin to current reversal, current reversal blocking only used for permissive scheme not blocking scheme.

Considering the pickup and drop off time difference of distance elements and the channel time delay between the device A and the device B, the maloperation due to current reversal shall be eliminated by setting the time delay. The reverse direction element of the device is not required for this method, the channel time delay and the tripping time of adjacent breaker shall be taken into account comprehensively.

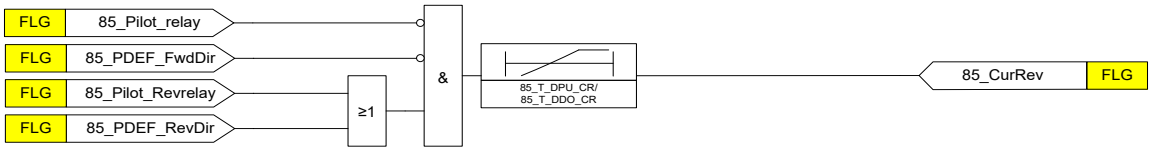


Figure 3.9.13 Logic diagram of current reversal blocking

Once the current reversal logic is enabled, the time delay pilot protection will set to the setting 85_PD_T_CR.

3.9.2.8 Weak Infeed

In case of a fault in line at one end of which there is a weak power source, the fault current supplied to the fault point from the weak power source is very small or even nil, and the conventional distance element could not operate. The weak infeed logic combines the protection information from the strong power source end and the electric feature of the local end to cope with the case.

The weak infeed logic can be only applied for Blocking and POTT. The weak infeed logic has options for echo or both echo and tripping.

When the weak infeed logic is enabled, distance forward and reverse element and direction element of directional earth-fault protection do not operate with the voltage lower than the setting 85_Vol_WI after the device picks up, upon receiving signal from remote end, the weak infeed logic will echo the signal back to remote end for 200ms if the weak infeed echo is enabled, the weak infeed end will echo signal and release tripping according to the logic.

ZPilot_Rev at weak source end must coordinate with ZPilot_Set of the remote end. The coverage of ZPilot_Rev must exceed that of ZPilot_Set of the remote end. ZPilot_Rev only activates in the protection calculation when the weak infeed logic is enabled. In case of the weak infeed logic not enabled, the setting coordination is not required.

If the device does not pick up, and the weak infeed logic is enabled, upon receiving signal from remote end with the voltage lower than the setting 85_Vol_WI, the weak infeed logic will echo back to remote end for 200ms. When either weak infeed echo or weak infeed tripping is enabled, then the weak infeed logic is deemed to be enabled. During the device pick up, the weak infeed logic is shown in Figure 3.9.14.

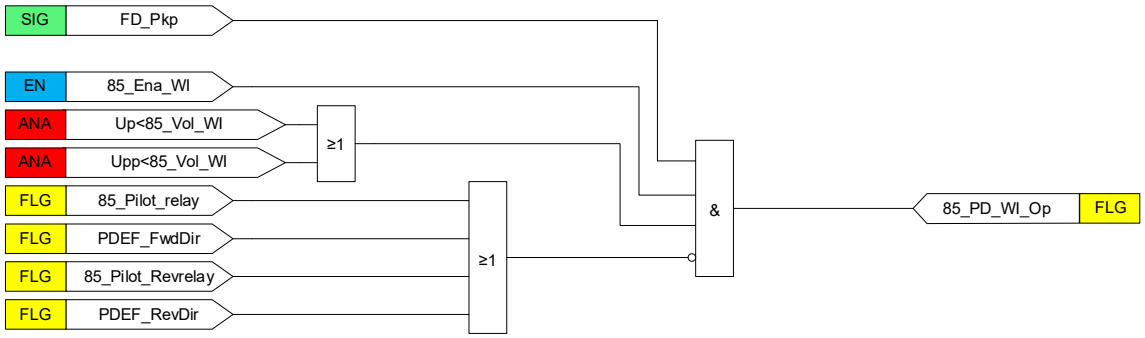


Figure 3.9.14 Weak infeed logic during pick up

For weak infeed end, the device may not pick up when a fault happens to the protected line. If the

device does not pick up, the setting 85_Ena_WI_Pkp is used to determine that weak infeed echo logic without pickup or weak infeed trip logic without pickup is executed. The logic is shown in Figure 3.9.15.

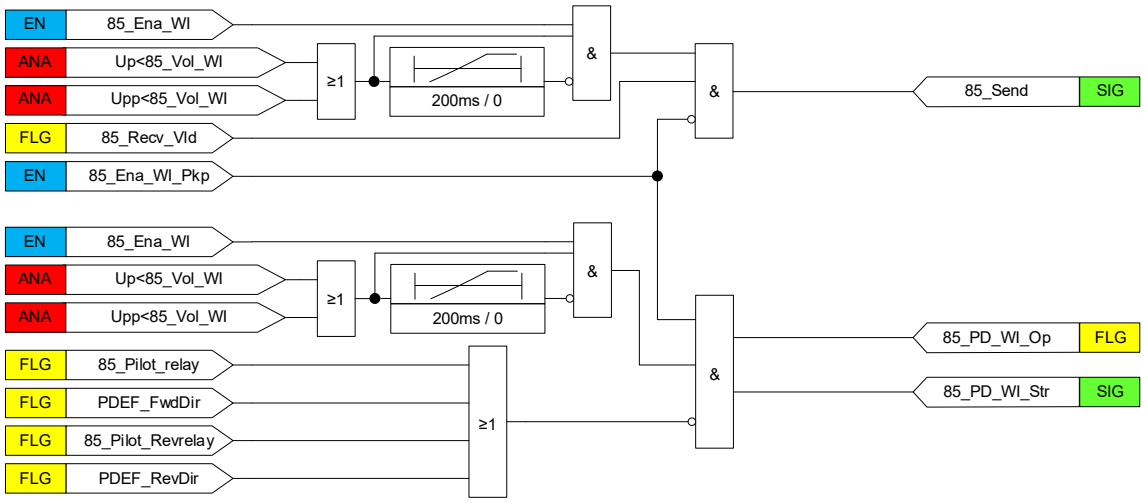


Figure 3.9.15 Weak infeed logic without pick up

3.9.2.9 CB Echo

A feature is also provided which enables fast tripping to be maintained along the whole length of the protected line, even when one terminal is open. The device will initiate sending a pulse of 200ms permissive signal when signal receive condition is met during CB is in open position. This logic will be terminated immediately once the device picks up.

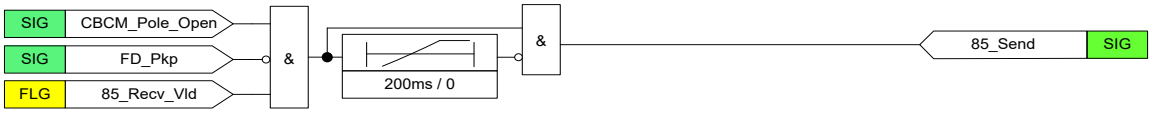


Figure 3.9.16 CB echo logic

3.9.3 Settings

Table 3.9-3 Pilot distance protection Settings

NO	Name	Range	Unit	Step	Default	Description
1	85_PilotMode	0: POTT 1: PUTT 2: Blocking	-	1	0	Option of pilot scheme
2	85_Ch_PhSeg	0 or 1	-	1	0	Option of phase-segregated signal scheme or three-phase signal scheme 0: three-phase signal scheme 1: phase-segregated signal scheme
3	85_Ena_Unblk	0 or 1	-	1	0	Enabling/disabling unblocking scheme

NO	Name	Range	Unit	Step	Default	Description
						0: disable 1: enable
4	85_Ena_WI	0 or 1	-	1	0	Enabling/disabling weak infeed scheme 0: disable 1: enable
5	85_Ena_WI_Pkp	0 or 1	-	1	0	Enabling/disabling the device pick up at weak infeed end. For weak infeed end, If the device does not pick up for internal fault, it is used to enable the device pick up. 0: disable 1: enable
6	85_PD_Ena	0 or 1	-	1	0	Enabling/disabling pilot distance protection 0: disable 1: enable
7	85_PD_PSBR_Ena	0 or 1	-	1	0	Enabling/disabling pilot distance protection controlled by PSBR 0: disable 1: enable
8	85_PD_PEQuad_Ena	0 or 1	-	1	0	Enabling/disabling quadrilateral characteristic of phase-to-earth pilot distance protection 0: disable 1: enable
9	85_PD_PPQuad_Ena	0 or 1	-	1	0	Enabling/disabling quadrilateral characteristic of phase-to-phase pilot distance protection 0: disable 1: enable
10	85_PD_ZX_Ena	0 or 1	-	1	0	Enabling/disabling zone extension of pilot distance protection 0: disable 1: enable
11	85_PD_ZAng	10~89	deg	0.01	85	Phase angle of positive-sequence impedance for pilot distance zone
12	85_PD_Kz	0~10.000		0.001	0.67	Zero-sequence compensation coefficient magnitude for pilot distance zone

NO	Name	Range	Unit	Step	Default	Description
13	85_PD_KzAng	0~360.00	deg	0.01	0	Zero-sequence compensation coefficient angle for pilot distance zone
14	85_PD_MhoImp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of pilot distance protection (Mho characteristic)
15	85_PD_MhoImp_Rev	(0.05~500)/In	ohm	0.01	8	Impedance setting of pilot distance protection in reverse direction (Mho characteristic)
16	85_PD_Ang_Alpha	5~45	deg	0.01	25	Angle of blinder in fourth quadrant for forward direction (Quad characteristic)
17	85_PD_Ang_Beta	0~85	deg	0.01	30	Angle of blinder in second quadrant for forward direction (Quad characteristic)
18	85_PD_X0Comp_Ang	0~30	deg	0.01	12	Zero sequence reactance compensation angle (Quad characteristic)
19	85_PD_QuadImp_Op	(0.05~500)/In	ohm	0.01	8	Impedance setting of pilot distance protection (Quad characteristic)
20	85_PD_QuadImp_Rev	(0.05~500)/In	ohm	0.01	8	Impedance setting of pilot distance protection in reverse direction (Quad characteristic)
21	85_PD_QuadR_Op	(0.05~500)/In	ohm	0.01	8	Resistance setting of pilot distance protection (Quad characteristic)
22	85_PD_QuadR_Rev	(0.05~500)/In	ohm	0.01	8	Resistance setting of pilot distance protection in reverse direction (Quad characteristic)
23	85_Vol_WI	0~Unn	V	0.01	30	Undervoltage setting of weak infeed logic
24	85_PD_T_Blk	0.000~1.000	s	0.001	0.03	Time delay for blocking scheme of pilot distance protection operation
25	85_PD_T_ZX	0.000~10.000	s	0.001	0.03	Time delay for zone extension of pilot distance protection operation
26	85_PD_T_CR	0.000~1.000	s	0.001	0.03	Time delay for current reversal protection
27	85_T_DPU_CR	0.000~1.000	s	0.001	0.003	Time delay pickup for current reversal logic

NO	Name	Range	Unit	Step	Default	Description
28	85_T_DDO_CR	0.000~1.000	s	0.001	0.05	Time delay dropoff for current reversal logic
29	85_T_Unblk	0.000~10.000	s	0.001	0.03	Pickup time delay of unblocking scheme for pilot channel

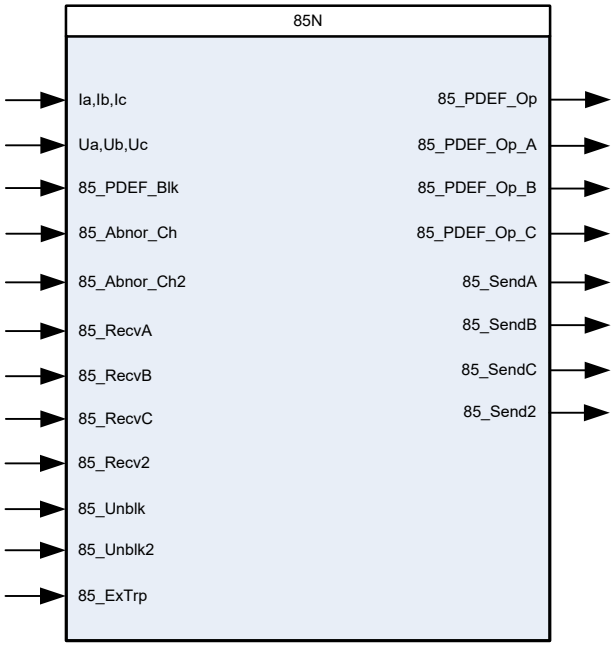
3.10 Scheme communication logic for directional earth fault protection 85N

3.10.1 Overview

Directional earth fault protection needs to coordinate with downstream protection with definite or inverse time delay so it cannot clear an internal fault quickly. Pilot directional earth-fault protection takes use of directional earth fault elements on both ends, it can detect high resistance fault and maintain high-speed operation.

Pilot directional earth-fault protection can be used independently, for example, no distance protection is equipped with the device but fast operation is required for the whole line, or it is used as backup protection of pilot distance protection to enhance the sensitivity for an earth fault with high fault resistance.

3.10.1.1 Function Block



3.10.1.2 Signals

Table 3.10-1 Pilot directional earth-fault protection Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input

NO.	Signal	Description
3	85_PDEF_Blk	Block signal of pilot directional earth-fault protection
4	85_Abnor_Ch	Input signal of indicating that pilot channel is abnormal for pilot directional earth-fault protection
5	85_Abnor_Ch2	Input signal of indicating that pilot channel is abnormal for pilot directional earth-fault protection when pilot directional earth-fault protection adopting independent pilot channel
6	85_RecvA	Input signal of receiving permissive signal via pilot channel for pilot distance protection(only for three-phase command scheme) , or input signal of receiving permissive signal of A-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)
7	85_RecvB	Input signal of receiving permissive signal of B-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)
8	85_RecvC	Input signal of receiving permissive signal of C-phase via pilot channel for pilot distance protection (only for phase-segregated command scheme)
9	85_Recv2	Input signal of receiving permissive signal via pilot channel for pilot directional earth-fault protection when pilot directional earth-fault protection adopting independent pilot channel
10	85_Unblk	Unblocking signal of pilot directional earth-fault protection
11	85_Unblk2	Unblocking signal of pilot directional earth-fault protection when pilot directional earth-fault protection adopting independent pilot channel
12	85_ExTrp	Input signal of initiating sending permissive signal from external tripping signal for pilot directional earth-fault protection

Table 3.10-2 Pilot directional earth-fault protection Output Signals

NO.	Signal	Description
1	85_PDEF_Op	Operation signal from pilot directional earth-fault protection
2	85_PDEF_Op_A	Operation signal from phase A
3	85_PDEF_Op_B	Operation signal from phase B
4	85_PDEF_Op_C	Operation signal from phase C
5	85_SendA	Output signal of sending permissive signal of pilot distance protection(only for three-phase command scheme) ,

NO.	Signal	Description
		or output signal of sending A-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
6	85_SendB	Output signal of sending B-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
7	85_SendC	Output signal of sending C-phase permissive signal of pilot distance protection (only for phase-segregated command scheme)
8	85_Send2	Output signal of sending permissive signal of pilot directional earth-fault protection when pilot directional earth-fault protection adopting independent pilot channel

3.10.2 Protection Principle

Sending permissive signal (or terminating sending signal) to the opposite end is controlled by forward direction element. Current reversal logic is available for parallel line operation and CB echo logic is provided once pilot directional earth fault protection is enabled. Current reversal logic is only used for permissive scheme. For blocking scheme, current reversal need not be considered because there is a settable time delay in pilot directional earth-fault protection.

Pilot directional earth-fault protection can be enabled or disabled by input signals, logic setting and blocking signal, as shown in Figure 3.10.1.

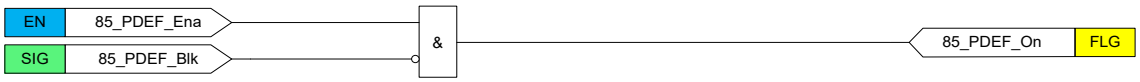


Figure 3.10.1 Enabling/disabling logic of pilot directional earth-fault protection

Pilot directional earth-fault protection comprises permissive scheme and blocking scheme. It can share pilot channel 1 (the setting 85_PDEF_IndepCh_Ena is set as "0") with pilot distance protection, or uses independent pilot channel 2 (the setting 85_PDEF_IndepCh_Ena is set as "1") by the setting 85_PDEF_IndepCh_Ena. For underreach mode, pilot directional earth-fault always adopts independent pilot channel 2. The logic of receiving signal is shown in Figure 3.10.2.

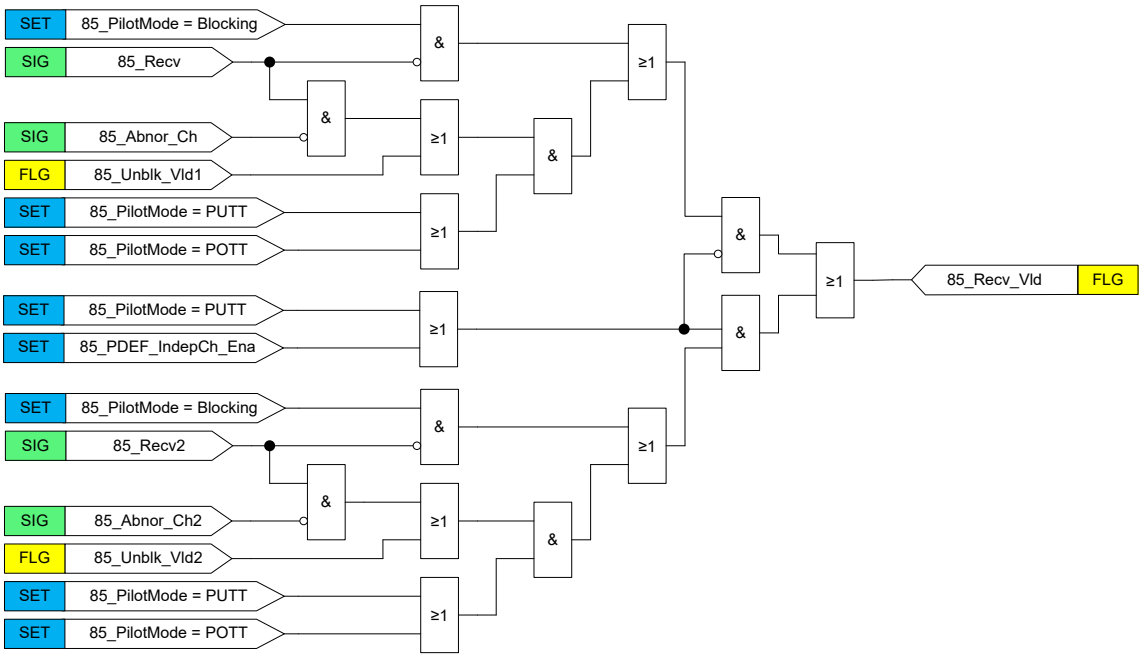


Figure 3.10.2 Logic diagram of receiving signal

3.10.2.1 Directional earth-fault Element

The residual current is pre-processed by a discrete Fourier filter. Thus, the phasor of the fundamental frequency component of the residual current is derived. The phasor magnitude is used within the earth-fault protection to compare it with the set current value of the settings FD_ResCur_Str.

The direction check is performed based on the following equation of forward direction:

$$90^{\circ} \leq \arg\frac{3I0 \times \dot{e}^{JRCA}}{3U0} \leq 270^{\circ}$$

Also, it can be calculated by following equation:

$$-90^{\circ} \leq \text{angle}(3I0) + RCA - \text{angle}(3U0) \leq 270^{\circ}$$

Where:

RCA: Line zero-sequence impedance angle, set by the setting LinAng0

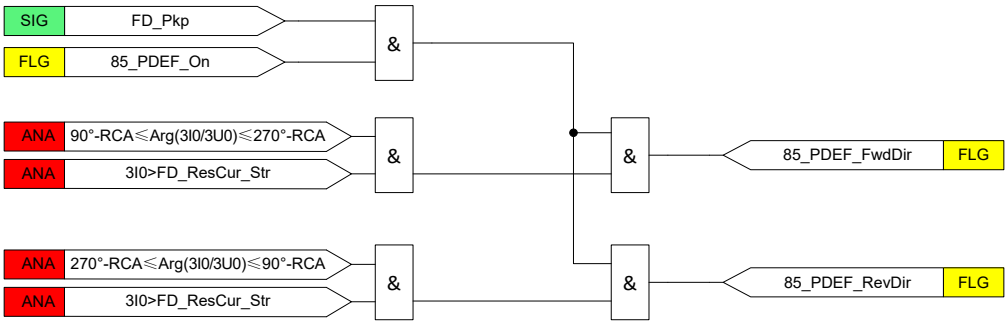


Figure 3.10.3 Logic diagram of directional earth-fault element

3.10.2.2 Permissive Transfer Trip (PTT)

Pilot protection with permissive scheme receives permissive signal from the device of remote end, so as to combine with local discrimination condition to accelerate tripping, so it has high security. Operation of forward directional earth fault element is used to send permissive signal to the remote end when the protection is enabled and will release tripping signal upon receiving permissive signal from the remote end with further guarded by no operation of reverse directional earth fault element. This ensures the security of the protection.

The following figure shows the schematic of permissive transfer trip.

For blocking scheme, pilot directional earth-fault protection will operate when there is an internal fault with abnormal channel, however, it is possible that pilot directional earth-fault protection issues an undesired trip when there is an external fault with abnormal channel.

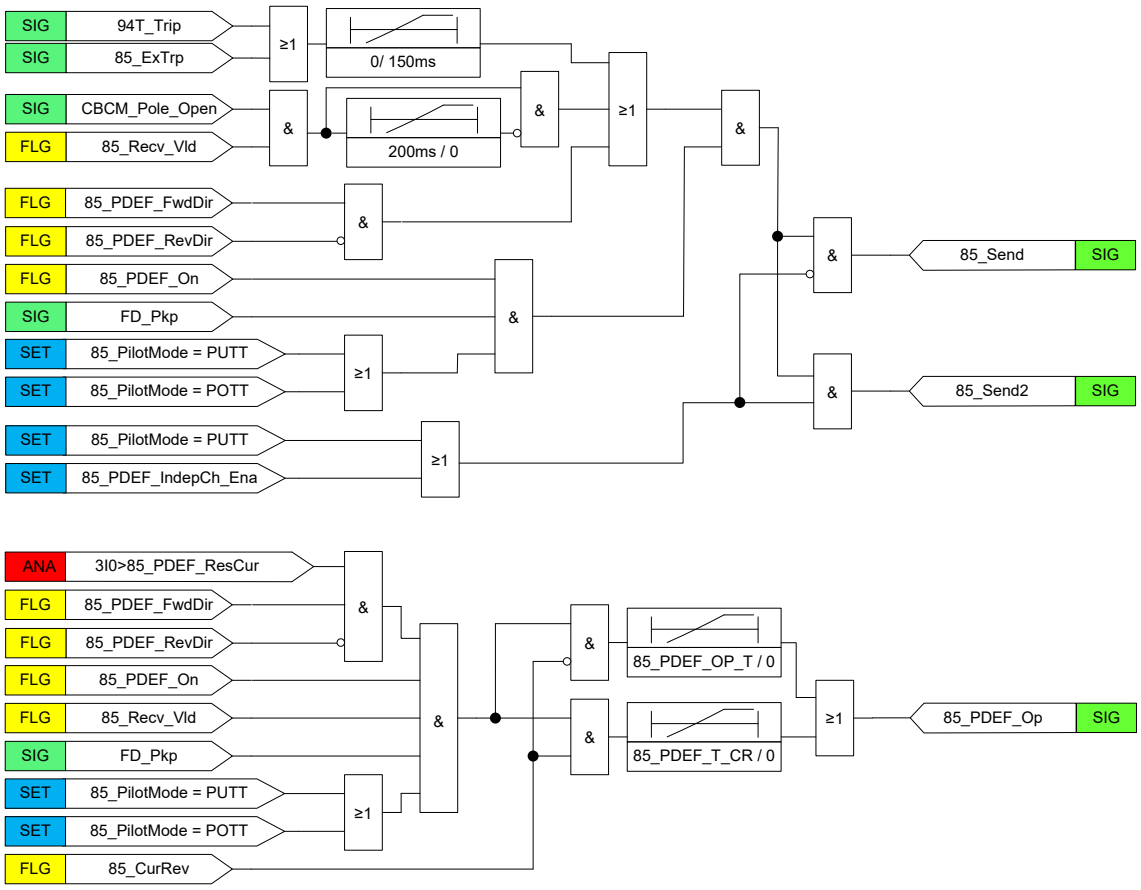


Figure 3.10.4 Logic diagram of permissive scheme

3.10.2.3 Blocking

Permissive scheme has high security, but it relies on pilot channel seriously. Pilot directional earth-fault protection will not operate when there is an internal fault with abnormal channel. Blocking scheme could be considered as an alternative.

Blocking scheme sends blocking signal when fault detector picks up and zero-sequence forward element does not operate or both zero-sequence forward element and zero-sequence reverse

element do not operate. Pilot directional earth-fault protection will operate if forward directional zero-sequence overcurrent element operates and not receiving blocking signal.

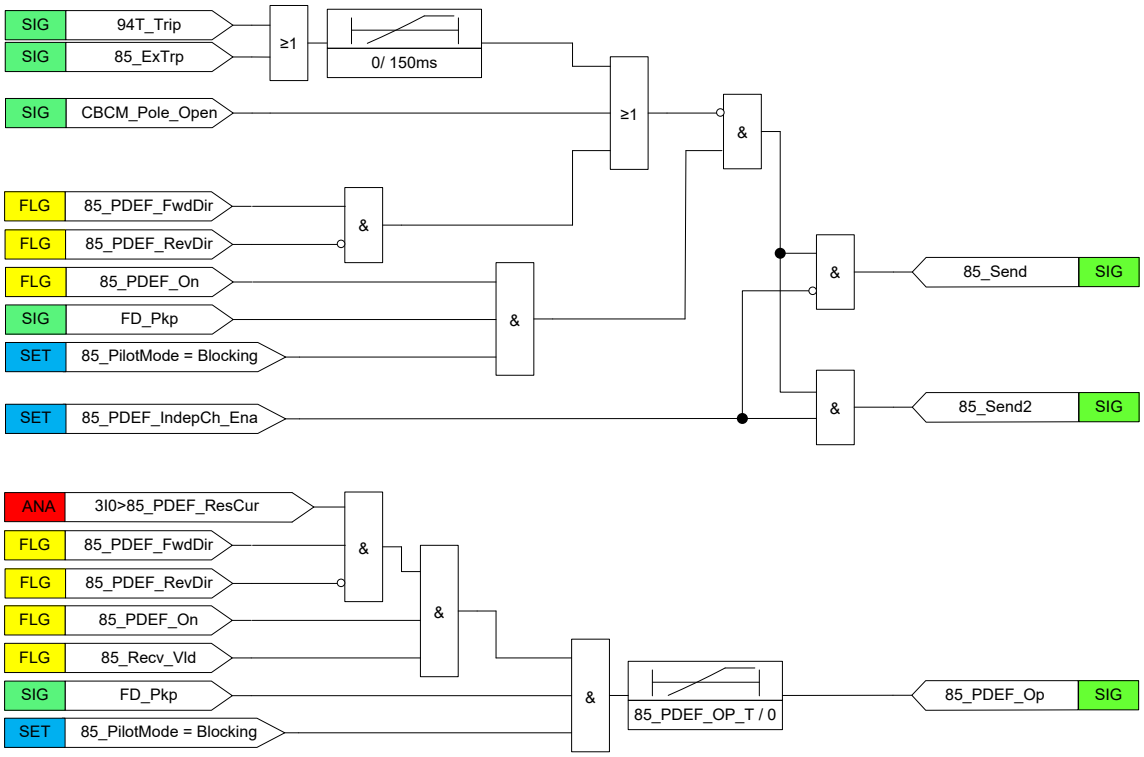


Figure 3.10.5 Logic diagram of DEF (Blocking scheme)

Because the time delay of pilot directional earth-fault protection has enough margin for current reversal, so blocking scheme should not consider the current reversal condition.

3.10.2.4 Unblocking

The unblocking scheme can only be used together with permissive scheme. The logic of unblocking is shown in Figure 3.10.6.

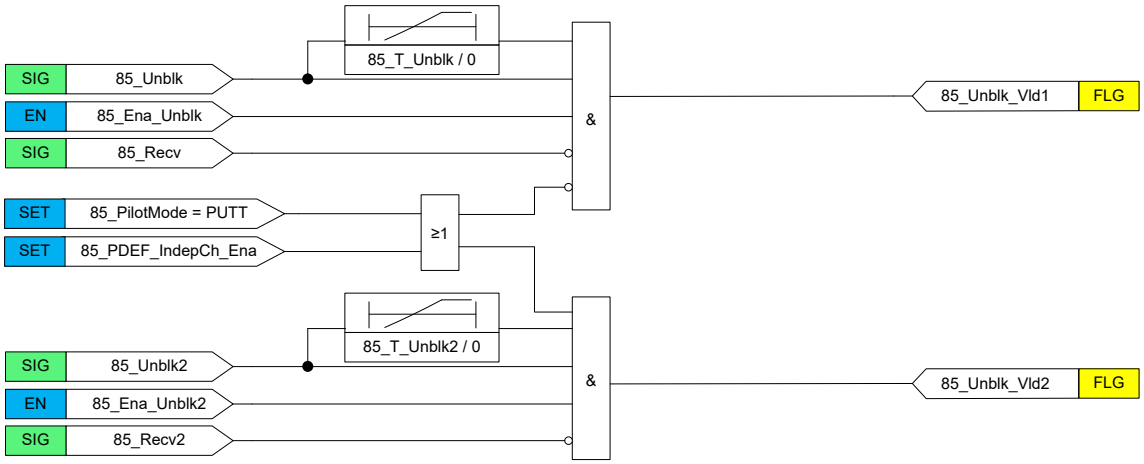


Figure 3.10.6 Logic diagram for unblocking

3.10.2.5 Current Reversal

The reach of directional earth-fault protection is difficult to define. There may have problem for pilot direction earth-fault protection applied on parallel line arrangement due to current reversal phenomenon. Current reversal blocking logic using time delay method is adopted in the device. It is the same logic as pilot distance protection. The only difference is that different settings are used if independent channel is selected. When adopting independent pilot channel 2, t1 and t2 are the settings 85_T_DPU_CR2 and 85_T_DDO_CR2 respectively, which should be considered individually from channel 1.When sharing pilot channel 1 with pilot distance protection, t1 and t2 are the settings 85_T_DPU_CR and 85_T_DDO_CR respectively.

3.10.2.6 CB Echo

The logic of CB echo is the same logic as pilot distance protection.

3.10.3 Settings

Table 3.10-3 Pilot directional earth-fault protection Settings

NO	Name	Range	Unit	Step	Default	Description
1	85_PDEF_Ena	0 or 1	-	1	0	Enabling/disabling pilot directional earth-fault protection 0: disable 1: enable
2	85_PDEF_IndepCh_Ena	0 or 1	-	1	0	Enabling/disabling independent channel for pilot directional earth-fault protection 0: pilot directional earth-fault protection sharing same channel with pilot distance protection 1: pilot directional earth-fault adopting independent pilot channel
3	85_Ena_Unblk2	0 or 1	-	1	0	Enabling/disabling unblocking scheme when pilot directional earth-fault protection adopts independent pilot channel 0: disable 1: enable
4	85_PDEF_ResCur	(0.05~30.00)×In	A	0.01	2	Current setting of pilot directional earth-fault protection
5	85_PDEF_Op_T	0.000~10.000	s	0.001	0.03	Time delay for pilot directional earth-fault operation
6	85_PDEF_T_CR	0.000~1.000	s	0.001	0.03	Time delay for current reversal protection

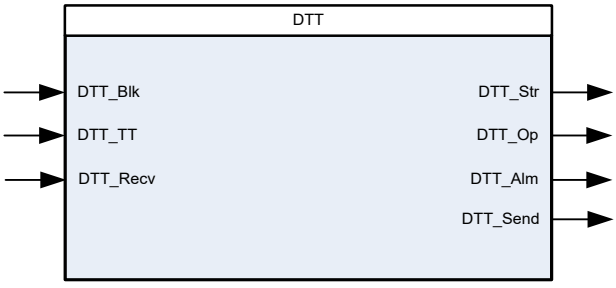
NO	Name	Range	Unit	Step	Default	Description
7	85_T_DPU_CR2	0.000~1.000	s	0.001	0.003	Time delay pickup for current reversal logic when pilot directional earth-fault protection adopts independent pilot channel
8	85_T_DDO_CR2	0.000~1.000	s	0.001	0.05	Time delay dropoff for current reversal logic when pilot directional earth-fault protection adopts independent pilot channel
9	85_T_Unblk2	0.000~10.000	s	0.001	0.03	Pickup time delay of unblocking scheme for pilot channel when pilot directional earth-fault protection adopts independent pilot channel

3.11 Direct Transfer Trip Logic DTT

3.11.1 Overview

According to actual conditions, the binary input contact of initiating sending transfer trip signal at local side of the device can be connected separately or in parallel by the output contact of the “bus differential protection”, “reactor protection” or “failure protection”. The direct transfer trip signal receive from the remote side is the signal that the remote side requires the device at local side to trip.

3.11.1.1 Function Block



3.11.1.2 Signals

Table 3.11-1 Direct transfer trip protection Input Signals

NO.	Signal	Description
1	DTT_Blk	Block signal of DTT
2	DTT_TT	Input signal of initiating sending transfer trip signal from external tripping signal for DTT

NO.	Signal	Description
3	DTT_Recv	Input signal of receiving transfer trip signal via pilot channel for DTT

Table 3.11-2 Direct transfer trip protection Output Signals

NO.	Signal	Description
1	DTT_Str	General start signal of DTT
2	DTT_Op	Operation signal from DTT
3	DTT_Alm	Input signal of receiving transfer trip is abnormal
4	DTT_Send	Output signal of sending transfer trip signal of DTT

3.11.2 Protection Principle

Direct transfer trip can be controlled by local fault detector by logic settings DTT_FD_Ctrl_Ena. In addition, the input signal DTT_Recv is always supervised, and the device will issue an alarm DTT_Alm and block direct transfer trip once the input signal is energized for longer than the setting time DTT_Op_T add 4s.

3.11.3 Logic

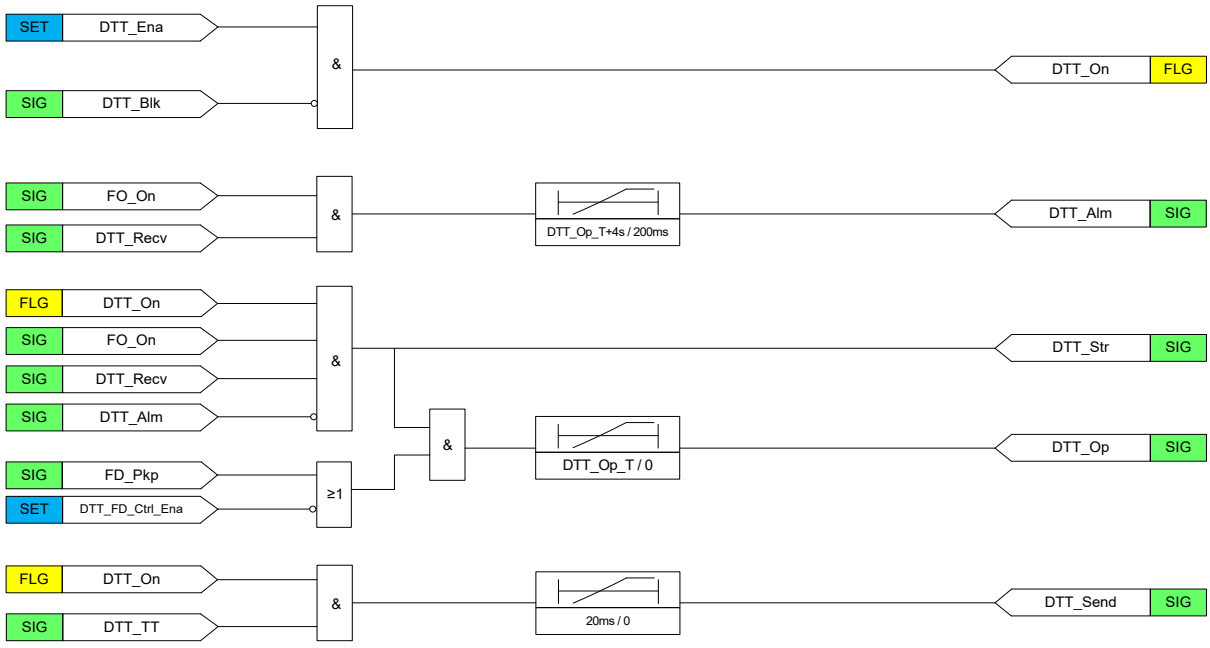


Figure 3.11.1 Logic Diagram for DTT

3.11.4 Settings

Table 3.11-3 DTT Settings

NO	Name	Range	Unit	Step	Default	Description
1	DTT_Ena	0 or 1	-	1	0	Enabling/disabling direct transfer trip protection 0: disable

NO	Name	Range	Unit	Step	Default	Description
						1: enable
2	DTT_FD_Ctrl_Ena	0 or 1	-	1	0	Enabling/disabling direct transfer trip protection controlled by local fault detector element 0: disable 1: enable
3	DTT_Op_T	0.000~600.000	s	0.001	1	Time delay for direct transfer trip operation

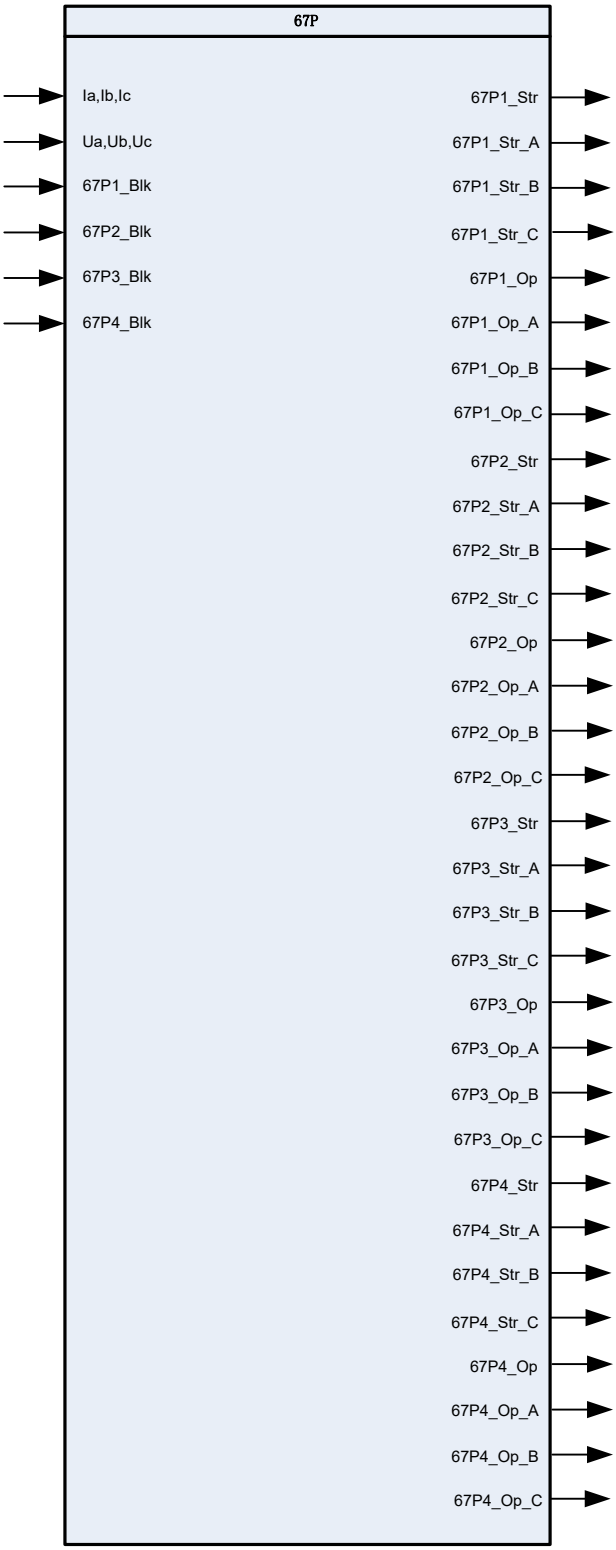
3.12 Three Phase Directional Overcurrent Protection 67P

3.12.1 Overview

When a fault occurs in power system, current in the faulty phase will usually increase. By detecting the fault current, three-phase directional overcurrent 67P can discover short circuits in the system. It can be used as backup protection in addition to the main protection. 67P has the following characteristics:

- Each of the four stages in 67P has independent logic, threshold current, and settable time delays.
- All four stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.
- Direction control element can be set to control all stages of 67P protection among three options: non-directional, forward direction and reverse direction.

3.12.1.1 Function Block



3.12.1.2 Signals

Table 3.12-1 67P Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	67P1_Blk	Block signal of 67P stage1
4	67P2_Blk	Block signal of 67P stage2
5	67P3_Blk	Block signal of 67P stage3
6	67P4_Blk	Block signal of 67P stage4

Table 3.12-2 67P Output Signals

NO.	Signal	Description
1	67P1_Str	Common start signal from stage1
2	67P1_Str_A	Start signal from stage1 phase A
3	67P1_Str_B	Start signal from stage1 phase B
4	67P1_Str_C	Start signal from stage1 phase C
5	67P1_Op	Operation signal from stage1
6	67P1_Op_A	Operation signal from stage1 phase A
7	67P1_Op_B	Operation signal from stage1 phase B
8	67P1_Op_C	Operation signal from stage1 phase C
9	67P2_Str	Common start signal from stage2
10	67P2_Str_A	Start signal from stage2 phase A
11	67P2_Str_B	Start signal from stage2 phase B
12	67P2_Str_C	Start signal from stage2 phase C
13	67P2_Op	Operation signal from stage2
14	67P2_Op_A	Operation signal from stage2 phase A
15	67P2_Op_B	Operation signal from stage2 phase B
16	67P2_Op_C	Operation signal from stage2 phase C
17	67P3_Str	Common start signal from stage3
18	67P3_Str_A	Start signal from stage3 phase A
19	67P3_Str_B	Start signal from stage3 phase B
20	67P3_Str_C	Start signal from stage3 phase C
21	67P3_Op	Operation signal from stage3
22	67P3_Op_A	Operation signal from stage3 phase A
23	67P3_Op_B	Operation signal from stage3 phase B
24	67P3_Op_C	Operation signal from stage3 phase C
25	67P4_Str	Common start signal from stage4
26	67P4_Str_A	Start signal from stage4 phase A
27	67P4_Str_B	Start signal from stage4 phase B

NO.	Signal	Description
28	67P4_Str_C	Start signal from stage4 phase C
29	67P4_Op	Operation signal from stage4
30	67P4_Op_A	Operation signal from stage4 phase A
31	67P4_Op_B	Operation signal from stage4 phase B
32	67P4_Op_C	Operation signal from stage4 phase C

3.12.2 Protection Principle

3.12.2.1 Phase Overcurrent Element

In the phase overcurrent element, the amplitude of phase current vector I_a, I_b and I_c are compared to the threshold value of 67P in each stage.

The phase overcurrent element will operate when the following criterions are met:

$$I_\phi > 67\text{Px\_Cur\_Op}$$

Where:

I_ϕ is the measured phase current.

67Px_Cur_Op is the current threshold value of stage x (x=1, 2, 3, or 4) of overcurrent element.

If a phase current is larger than the threshold current, 67Px_Str_A, 67Px_Str_B, and 67Px_Str_C signals are activated without delay. And the signal 67Px_Str will activate if any of the 67Px_Str_A, 67Px_Str_B, and 67Px_Str_C activates.

3.12.2.2 Direction Control Element

The direction element has a uniform effect on every stage of function 67P as described in the logic diagram. It means that every stage of a function receives the same direction result. And each stage can be set in the forward direction, reverse direction or no direction.

The process of direction determination is independent of the direction-determination procedure of other functions, for example, earth fault overcurrent protection 67N.

Every phase has a separate direction-measuring element. If the positive directional criteria in a phase are met, the direction determination result of this phase is set to FwdDir as in the logic diagram. If there are multiphase short circuits, all measuring elements involved perform direction determination independently.

The directional measuring element uses the short-circuit current I_r of the phase concerned and the polarized phase voltage U_r (as the reference voltage) to determine the direction. This means that the direction can still be determined unambiguously and correctly, even if a close up 1 or 2-phase fault occurs and short-circuit voltages collapse completely.

The characteristic angle 67P_RCA determine the most sensitive forward angle of phase current and phase-to-phase current.

The direction check is performed based on the following equation of forward direction:

$$-90^{\circ} \leq \arg\frac{\dot{I}_r \times \dot{e}^{jRCA}}{\dot{U}_r} \leq 90^{\circ}$$

Also, it can be calculated by following equation:

$$-90^{\circ} \leq \text{angle(Ir)} + \text{RCA} - \text{angle(Ur)} \leq 90^{\circ}$$

When the conditions in the formula are met, the result of the direction is set to FwDir as in the logic diagram, otherwise, the current direction polarized by U is reverse direction.

The polarizing voltage is available as long as the memory phase voltage exceeds 70%Un. If the memory phase voltage reduces to less than 70%Un, the device uses positive-sequence voltage as polarized voltage. When the positive-sequence voltage exceeds 10%Un, the polarizing voltage is available. So the directional element can be used for all unsymmetrical faults including close-in faults. If the positive-sequence voltage reduces to less than 10%Un, the device uses phase voltage as polarizing voltage. If the phase voltage is less than 70%Un, the polarizing voltage is invalid.

If the polarizing voltage is invalid, the direction element endures until the phase current decreases below the I_LINE(0.05In).

The following table shows which polarized voltage and phase current are used for direction-determination purposes.

Table 3.12-3 Direction description

Direction	Current	Polarized Voltage
Phase A	Ia	UaM/U1a/Ua
Phase B	Ib	UbM/U1b/Ub
Phase C	Ic	UcM/U1c/Uc

UaM is the memory voltage value of phase A.

U1a is the positive-sequence voltage value of phase A.

Ua is the current voltage value of phase A.

3.12.2.3 Harmonic Control Element

In order to prevent effects of inrush current on phase overcurrent protection, harmonic control element can be selected for each stage of phase overcurrent element by configuring logic setting 67Px_Harm2_Blk.

When the percentage of second harmonic component to fundamental component of phase current is greater than the setting 67P_Harm2_K_Blk, harmonic blocking element operates to block stage x of phase overcurrent protection if corresponding logic setting 67Px_Harm2_Blk is enabled.

When the fundamental component of phase current is greater than the setting 67P_Harm2_Cur_Rls, phase overcurrent protection will be unblocked by harmonic control element.

If fundamental component of phase current is lower than the minimum operating current (0.1In) then harmonic calculation is not carried out and harmonic blocking element does not operate.

For harmonic control element, the harmonic blocking mode can be selected through the setting 67P_Harm2_Blk_Mod, it can support phase blocking, cross blocking, and maximum phase blocking. The corresponding relationship is shown in the following table.

Table 3.12-4 Harmonic blocking mode

Harmonic blocking mode		Harmonic blocking criterion		
		Phase A	Phase B	Phase C
0	Phase blocking	Ia_2nd/Ia>	Ib_2nd/Ib>	Ic_2nd/Ic>
1	Cross blocking	(Ia_2nd/Ia>) or (Ib_2nd/Ib>) or (Ic_2nd/Ic>)		
2	Maximum phase blocking	MAX (Ia_2nd, Ib_2nd, Ic_2nd)/Ia>	MAX (Ia_2nd, Ib_2nd, Ic_2nd)/Ib>	MAX (Ia_2nd, Ib_2nd, Ic_2nd)/Ic>

Where:

Ia, Ib, Ic are the fundamental current.

Ia_2nd, Ib_2nd, Ic_2nd are the secondary harmonic current.

3.12.2.4 Definite-Time Delay

When the setting 67Px_Op_Curve_Type is set to 0, it means stage x of function 67P has definite time delay. The function will give out the operation signal after the setting time 67Px_Op_T if the stage x of the function start.

Each stage of 67P has a settable definite time delay independently.

3.12.2.5 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

User can select the operating characteristic from various inverse-time characteristic curves via setting 67Px_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 67Px_T_Min, then the operating time of the protection changes to the value of setting 67Px_T_Min automatically.

When 67Px_Cur_Mul_Ena is set to 1 and inverse-time characteristic is selected, if calculated current is more than Cur_Mul*I_p, then the operating time of the protection changes to the time delay calculated by the fault current I=Mul_Cur*I_p automatically.

Where:

Mul_Cur is the setting 67Px_Cur_Mul. (x=1, 2, 3, or 4)

I_p is current setting 67Px_Cur_Op (x=1, 2, 3, or 4)

It is necessary to consider coordination of the 67Px_Cur_Mul and 67Px_T_Min settings. The

67Px_T_Min should be less than the time delay calculated by the fault current I=Mul_Cur*I_p, when 67Px_Cur_Mul_Ena is set to 1.

3.12.2.6 Enable and Blocking of the Function

The direction determination can be blocked if a voltage circuit failure occurs and the setting 67Px_VTS_Blk is set to 1.

Each stage can be set to block the direction function independently by the setting 67x_VTS_Blk.

The direction block can only be functional when the device's internal supervision function voltage circuit failure detection is set on by VTS_Ena.

3.12.3 Logic

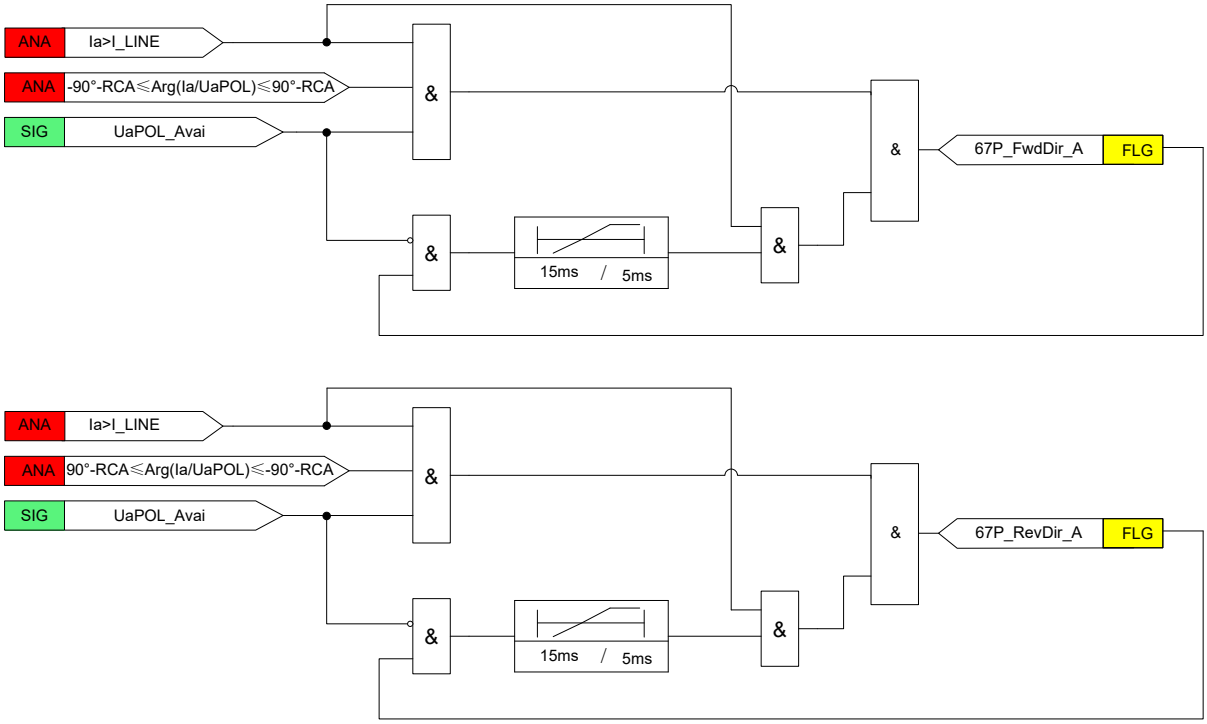


Figure 3.12.1 Logic Diagram for 67P Directional Function

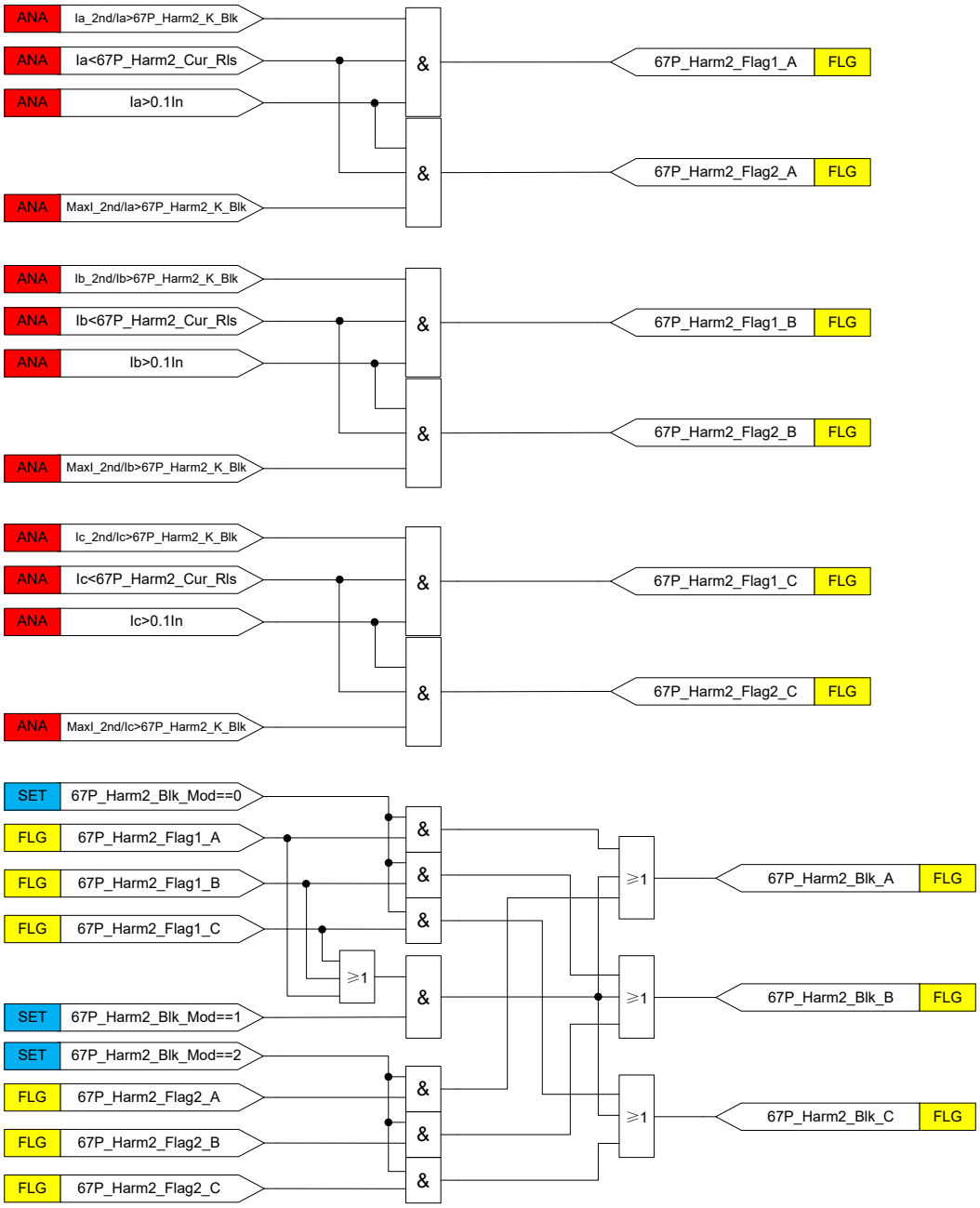


Figure 3.12.2 Logic Diagram for 67P Harmonic Control Element

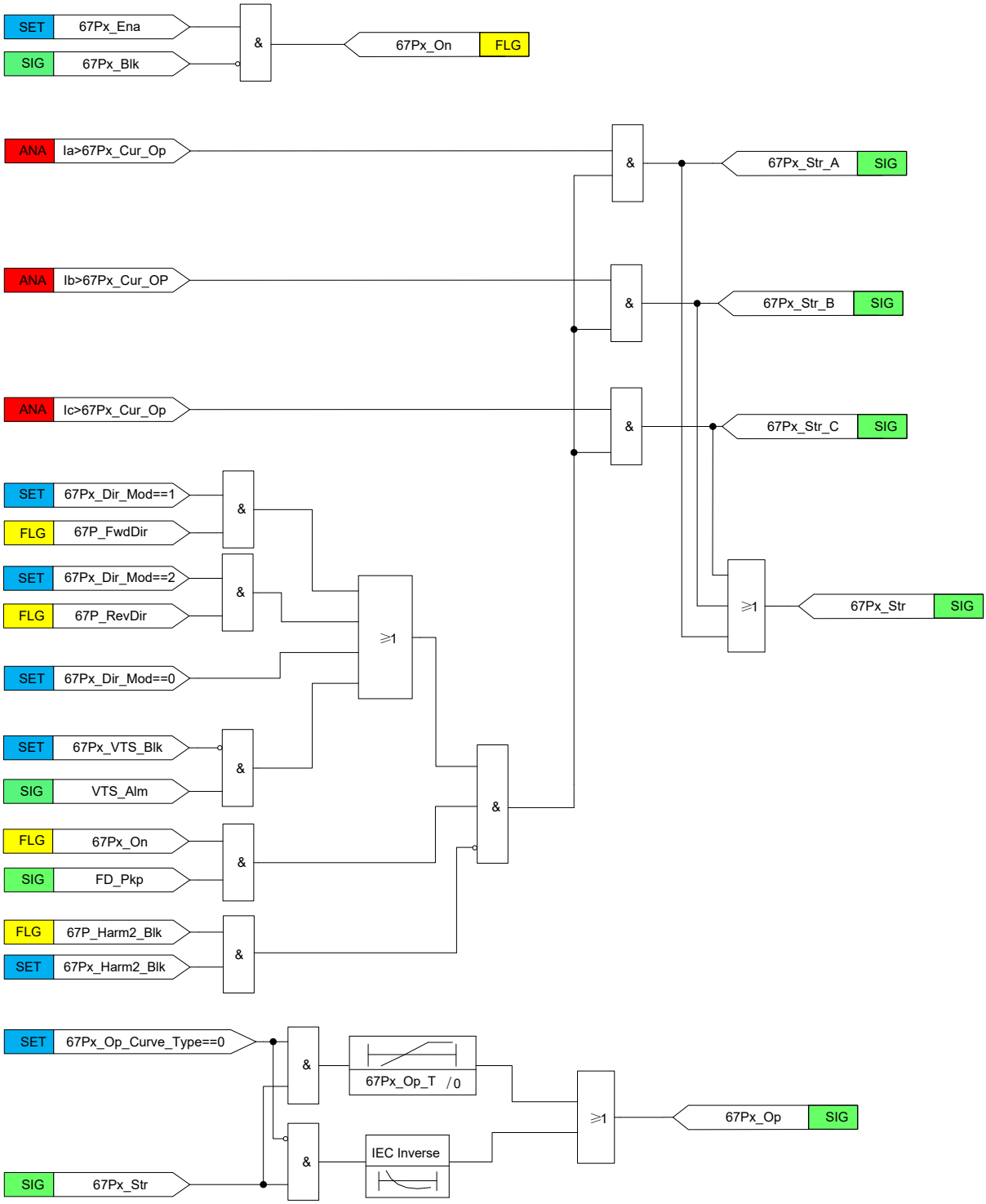


Figure 3.12.3 Logic Diagram for 67P

3.12.4 Settings

Table 3.12-5 67P Settings

NO	Name	Range	Unit	Step	Default	Description
1	67P_RCA	30~89	deg	0.01	80	The characteristic angle of directional phase overcurrent element
2	67P_Harm2_K_Blk	0.100~1.000	-	0.001	0.2	The coefficient of second harmonics of harmonic control element
3	67P_Harm2_Cur_Rls	(2.00~30.00)×In	A	0.01	20	The current setting of releasing harmonic control element
4	67P_Harm2_Blk_Mod	0~2	-	1	0	The option of harmonic Blocking mode. 0 : phase blocking(PhaseBlk) 1 : cross blocking(CrossBlk) 2 : maximum phase blocking (MaxPhaseBlk)
5	67Px_Ena	0 or 1	-	1	0	Enabling/disabling stage x of phase overcurrent protection (x=1, 2, 3, 4) 0: disable 1: enable
6	67Px_VTS_Blk	0 or 1	-	1	0	Enabling/Disabling stage x of phase overcurrent protection direction function blocked by VT circuit failure (x=1, 2, 3, 4) 0: disable 1: enable
7	67Px_Harm2_Blk	0 or 1	-	1	0	Enabling/Disabling stage x of phase overcurrent protection controlled by harmonic control element.(x=1, 2, 3, 4) 0: disable 1: enable
8	67Px_Cur_Mul_Ena	0 or 1	-	1	0	Enabling/Disabling stage x of phase overcurrent protection IDMT time delay is calculated by 67Px_Cur_Mul.(x=1, 2, 3, 4) 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
9	67Px_Cur_Op	(0.05~30.00)×In	A	0.01	20	Current setting for stage x of phase overcurrent protection(x=1, 2, 3, 4)
10	67Px_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of phase overcurrent protection (x=1, 2, 3, 4)
11	67Px_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time phase overcurrent protection(x=1, 2, 3, 4)
12	67Px_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time phase overcurrent protection(x=1, 2, 3, 4)
13	67Px_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic phase overcurrent protection (x=1, 2, 3, 4)
14	67Px_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic phase overcurrent protection (x=1, 2, 3, 4)
15	67Px_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic phase overcurrent protection (x=1, 2, 3, 4)
16	67Px_Cur_Mul	20.0~40.0	-	0.1	30	It used to IDMT with I=67Px_Cur_Mul*Ip, when I> 67Px_Cur_Mul*Ip, the IDMT time delay is calculated by 67Px_Cur_Mul. It is invalid if it is not configured or the 67Px_Cur_Mul_Ena is disable. (x=1, 2, 3, 4)

NO	Name	Range	Unit	Step	Default	Description
17	67Px_Dir_Mod	0~2	-	1	0	Direction option for stage x of phase overcurrent protection 0: Non-directional(x=1, 2, 3, 4) 1: Forward 2: Reverse
18	67Px_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2, 3, 4): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

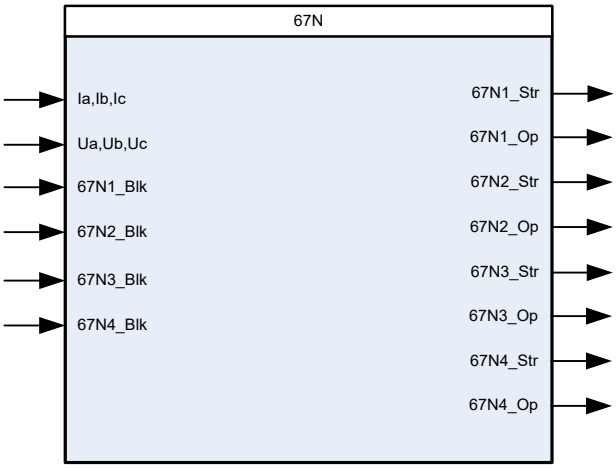
3.13 Directional Earth Fault Overcurrent Protection 67N

3.13.1 Overview

Directional four stages residual overcurrent protection 67N can be used as main protection for phase-to-earth faults. It can also be used to provide a backup protection in case of the primary protection being out of service due to communication failure. 67N protection has the following characteristics:

- Each of the four stages in 67N has independent logic, threshold current, and settable time delays.
- All four stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.
- Direction control element can be set to control all stages of 67N protection among three options: non-directional, forward direction and reverse direction.

3.13.1.1 Function Block



3.13.1.2 Signals

Table 3.13-1 67N Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	67N1_Blk	Block signal of 67N stage1
4	67N2_Blk	Block signal of 67N stage2
5	67N3_Blk	Block signal of 67N stage3
6	67N4_Blk	Block signal of 67N stage4

Table 3.13-2 67N Output Signals

NO.	Signal	Description
1	67N1_Str	Common start signal from stage1
2	67N1_Op	Operation signal from stage1
3	67N2_Str	Common start signal from stage2
4	67N2_Op	Operation signal from stage2
5	67N3_Str	Common start signal from stage3
6	67N3_Op	Operation signal from stage3
7	67N4_Str	Common start signal from stage4
8	67N4_Op	Operation signal from stage4

3.13.2 Protection Principle

3.13.2.1 Zero-sequence Overcurrent Element

The residual current is pre-processed by a discrete Fourier filter. Thus the phasor of the fundamental frequency component of the residual current is derived. The phasor magnitude is used within the 67N protection to compare it with the set operation current value of the four stages

(67Nx_ResCur_Op, x=1,2,3,4).

If the residual current is larger than the set operation current and the stage is used in non-directional mode a signal from the comparator for this stage is set to true. This signal will, without delay, activate the output signal 67Nx_Str (x=1,2,3,4) for this stage.

The operation criterion for each stage of 67N protection is:

$$3I0 > 67\text{Nx\_ResCur\_Op}$$

Where:

$3I0$ is the calculated residual current.

67Nx_ResCur_Op is the current threshold of stage x (x=1, 2, 3, or 4) of earth fault protection.

3.13.2.2 Direction Control Element

The setting 67N_PolarizedU is used to select the polarized voltage of direction control element, and two kinds of polarized voltages between "3U0" and "U2" can be selected.

By setting the characteristic angle 67N_RCA to determine the most sensitive forward angle of zero-sequence current. The direction check is performed based on the following equation of forward direction:

The polarized voltage is set as "3U0"

$$90^\circ \leq \arg\frac{3I0 \times \dot{e}^{JRCA}}{3U0} \leq 270^\circ$$

Also, it can be calculated by following equation:

$$90^\circ \leq \text{angle(3I0)} + \text{RCA} - \text{angle(3U0)} \leq 270^\circ$$

The polarized voltage is set as "U2"

$$90^\circ \leq \arg\frac{I2 \times \dot{e}^{JRCA}}{U2} \leq 270^\circ$$

Also, it can be calculated by following equation:

$$90^\circ \leq \text{angle(I2)} + \text{RCA} - \text{angle(U2)} \leq 270^\circ$$

3.13.2.3 Harmonic Control Element

In order to prevent effects of inrush current on earth fault protection, harmonic control element can be selected for each stage of earth fault element by configuring logic setting 67Nx_Harm2_Blk.

When the percentage of second harmonic component to fundamental component of residual current is greater than the setting 67N_Harm2_K_Blk, harmonic blocking element operates to block stage x of earth fault protection if corresponding logic setting 67Nx_Harm2_Blk is enabled.

When the fundamental component of zero-sequence current is greater than the setting 67N_Harm2_Cur_Rls, earth fault protection will be unblocked by harmonic control element.

If fundamental component of residual current is lower than the minimum operating current (0.1In) then harmonic calculation is not carried out and harmonic blocking element does not operate.

3.13.2.4 Definite-Time Delay

Each stage of 67N has a settable definite time delay independently. When the setting 67Nx_Op_Curve_Type is set to 0, it means stage x of function 67P has a definite-time delay. The function will give out the operation signal after the setting time 67Nx_Op_T expires if the stage x of 67N picks up.

3.13.2.5 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

User can select the operating characteristic from various inverse-time characteristic curves via setting 67Nx_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 67Nx_T_Min, then the operating time of the protection changes to the value of setting 67Nx_T_Min automatically.

When 67Nx_Cur_Mul_Ena is set to 1 and inverse-time characteristic is selected, if calculated current is more than Cur_Mul*I_p, then the operating time of the protection changes to the time delay calculated by the fault current $3I_0$=Mul_Cur*I_p automatically.

Where:

Mul_Cur is the setting 67Nx_Cur_Mul. (x=1, 2, 3, or 4)

I_p is current setting 67Nx_Cur_Op (x=1, 2, 3, or 4)

It is necessary to consider coordination of the 67Nx_Cur_Mul and 67Px_T_Min settings. The 67Nx_T_Min should be less than the time delay calculated by the fault current $3I_0$=Mul_Cur*I_p, when 67Nx_Cur_Mul_Ena is set to 1.

3.13.2.6 Enable and Blocking of the Function

Each stage of 67N protection can be blocked when certain abnormal conditions are detected if the setting 67Nx_Abnor_Blk is set to 1. If 67Nx_Abnor_Blk is set to 0, 67N protection will always start if the zero-sequence overcurrent element picks up disregards of the direction determination result. Abnormal conditions are listed below:

- when the system is under pole disagreement condition, for 1-pole AR, earth fault protection will operate. If the logic setting 67Nx_Abnor_Blk is set to “1”, the stage x of earth fault protection will be blocked.
- When manually closing circuit breaker, three phases of the circuit breaker maybe not operate simultaneously, and SOTF protection should operate. If the logic setting 67Nx_Abnor_Blk is

set to “1”, the stage x of earth fault protection will be blocked.

- VT circuit failure. If the logic setting 67Nx_Abnor_Blk is set to “1”,the stage x of earth fault protection will be blocked.

67N function can be blocked by CT circuit failure alarm signal if the setting 67Nx_CTS_Blk is set to 1.

3.13.3 Logic

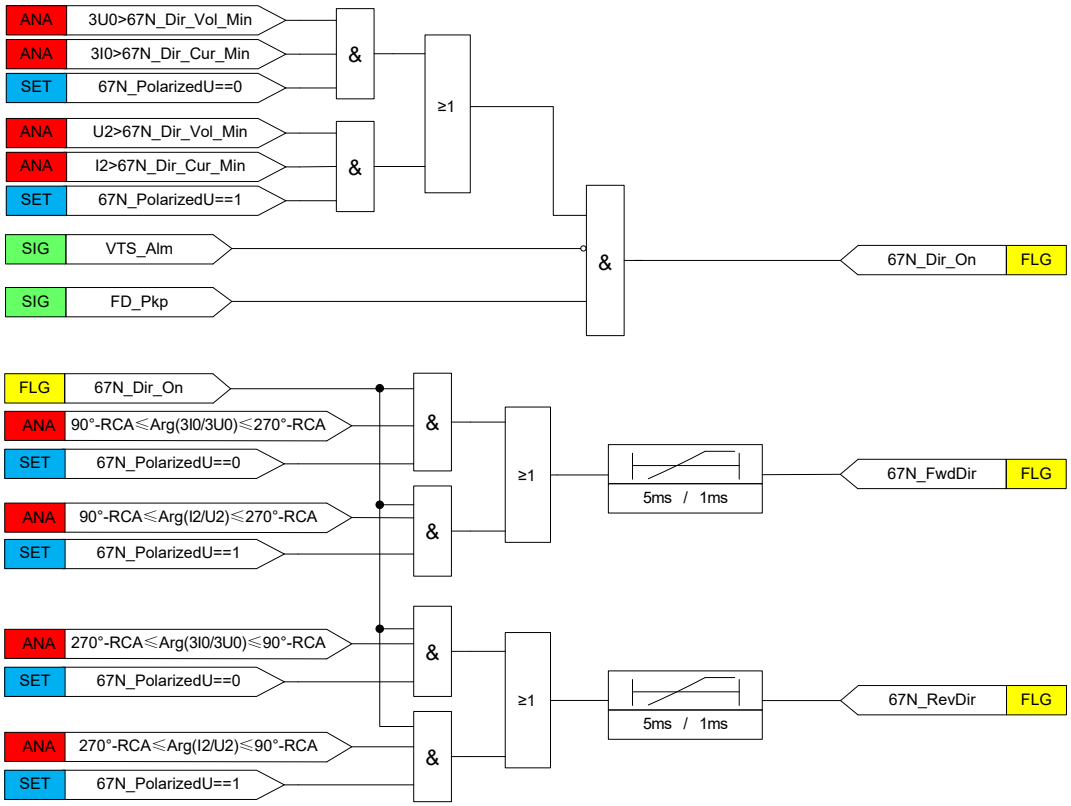


Figure 3.13.1 Logic Diagram for 67N Directional Function

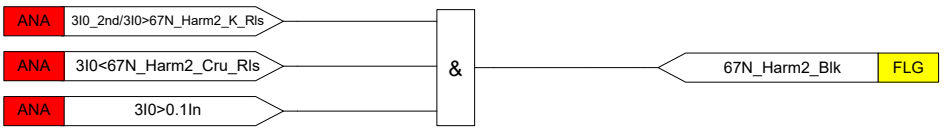


Figure 3.13.2 Logic Diagram for 67N Harmonic Control Element

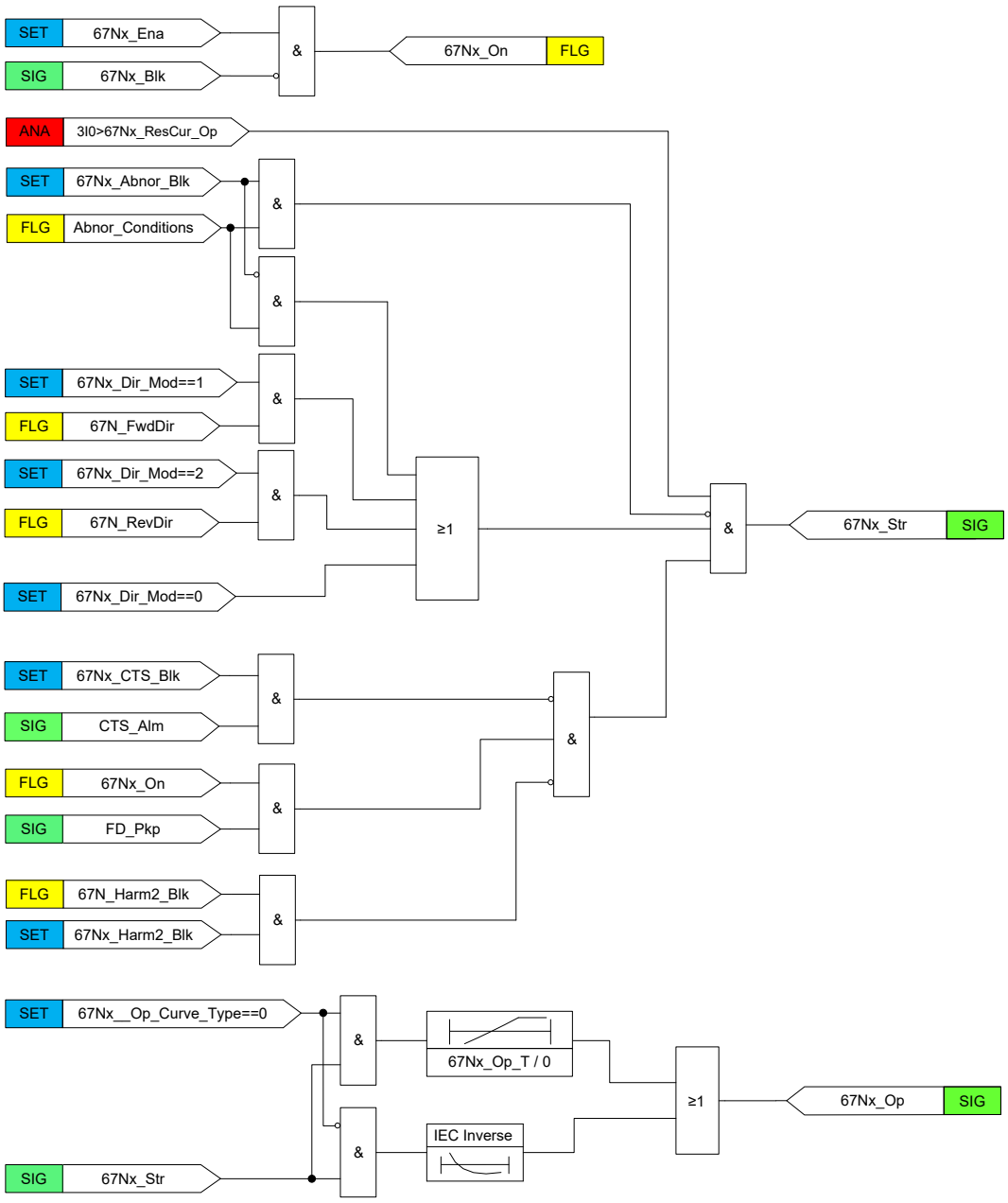


Figure 3.13.3 Logic Diagram of 67N

3.13.4 Settings

Table 3.13-3 67N Settings

NO	Name	Range	Unit	Step	Default	Description
1	67N_RCA	30~89	deg	0.01	80	The characteristic angle of directional earth fault element
2	67N_PolarizedU	0 or 1	-	1	0	The voltage polarization mode of direction control element 0 : zero-sequence voltage is used as polarized voltage(3U0) 1 : negative-sequence voltage is used as polarized voltage(U2)
3	67N_Dir_Cur_Min	(0.05~1.00) ×In	A	0.01	0.2	The minimum operating current setting of direction control element
4	67N_Dir_Vol_Min	1.00~10.00	V	0.01	1	The minimum operating voltage setting of direction control element
5	67N_Harm2_K_Blk	0.100~1.000	-	0.001	0.2	The coefficient of second harmonics of harmonic control element
6	67N_Harm2_Cur_Rls	(2.00~30.00) ×In	A	0.01	20	The current setting of releasing harmonic control element
7	67Nx_Ena	0 or 1	-	1	0	Enabling/disabling stage x of earth fault protection (x=1, 2, 3, 4) 0: disable 1: enable
8	67Nx_CTS_Blk	0 or 1	-	1	0	Enabling/disabling blocking for stage x of earth fault protection under CT failure conditions(x=1, 2, 3, 4) 0: disable 1: enable
9	67Nx_Abnor_Blk	0 or 1	-	1	0	Enabling/disabling blocking for stage x of earth fault protection under abnormal conditions(x=1, 2, 3, 4) 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
10	67Nx_Harm2_Blk	0 or 1	-	1	0	Enabling/Disabling stage x of earth fault protection controlled by harmonic control element(x=1, 2, 3, 4) 0: disable 1: enable
11	67Nx_Cur_Mul_Ena	0 or 1	-	1	0	Enabling/Disabling stage x of earth fault protection IDMT time delay is calculated by 67Px_Cur_Mul.(x=1, 2, 3, 4) 0: disable 1: enable
12	67Nx_ResCur_Op	(0.05~30.00) ×In	A	0.01	20	Current setting for stage x of earth fault protection(x=1, 2, 3, 4)
13	67Nx_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of earth fault protection(x=1, 2, 3, 4)
14	67Nx_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time earth fault protection (x=1, 2, 3, 4)
15	67Nx_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time earth fault protection (x=1, 2, 3, 4)
16	67Nx_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic earth fault protection(x=1, 2, 3, 4)
17	67Nx_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic earth fault protection(x=1, 2, 3, 4)
18	67Nx_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic earth fault protection(x=1, 2, 3, 4)
19	67Nx_Cur_Mul	20.0~40.0	-	0.1	30	It used to IDMT with $3I_0$=67Nx_Cur_Mul*Ip, when $3I_0$> 67Nx_Cur_Mul*Ip, the IDMT time delay is calculated by 67Nx_Cur_Mul. It is invalid if it is

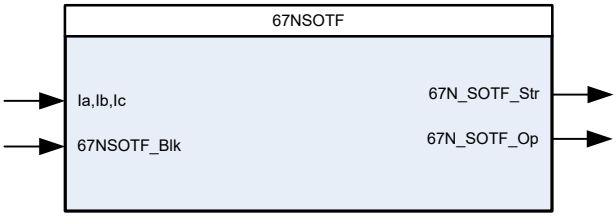
NO	Name	Range	Unit	Step	Default	Description
						not configured or the 67Nx_Cur_Mul_Ena is disable. (x=1, 2, 3, 4)
20	67Nx_Dir_Mod	0~2	-	1	0	Direction option for stage x of earth fault protection(x=1, 2, 3, 4) 0: Non-directional 1: Forward 2: Reverse
21	67Nx_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2, 3, 4): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.14 Residual Current SOTF Protection 67NSOTF

3.14.1 Overview

Zero-sequence current switch onto fault protection is integrated into 67N function. The setting 67N_SOTF_Ena has to set to 1 in order to enable the SOTF feature. When the circuit breaker is closing there is a risk to close it onto a permanent fault, for example during an auto-reclosing sequence. The SOTF logic will enable fast fault clearance during such situations.

3.14.1.1 Function Block



3.14.1.2 Signals

Table 3.14-1 67NSOTF Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	67NSOTF_Blk	Block signal of 67NSOTF

Table 3.14-2 67NSOTF Output Signals

NO.	Signal	Description
1	67N_SOTF_Str	Start signal from earth fault switch onto fault function
2	67N_SOTF_Op	Operation from earth fault switch onto fault function

3.14.2 Protection Principle

The residual current is pre-processed by a discrete Fourier filter. Thus the phasor of the fundamental frequency component of the residual current is derived. The phasor magnitude is used within the 67NSOTF protection to compare it with the set operation current value.

The operation criterion for each stage of 67N protection is:

$$3I0 > 67\text{N\_ResCur\_Op\_SOTF}$$

Where:

$3I0$ is the calculated residual current.

67N_ResCur_Op_SOTF is the current threshold of 67NSOTF protection.

The function will give out the operation signal after 100ms expires if 67NSOTF picks up.

For in-line transformer application, large inrush current generated during manual closing and auto-reclosing will lead to an undesired operation of residual current SOTF protection. Second harmonic blocking can be selected by the setting 67N_SOTF_Harm2_Blk to prevent maloperation due to inrush current. The harmonic control element is same to 67N.

3.14.3 Logic

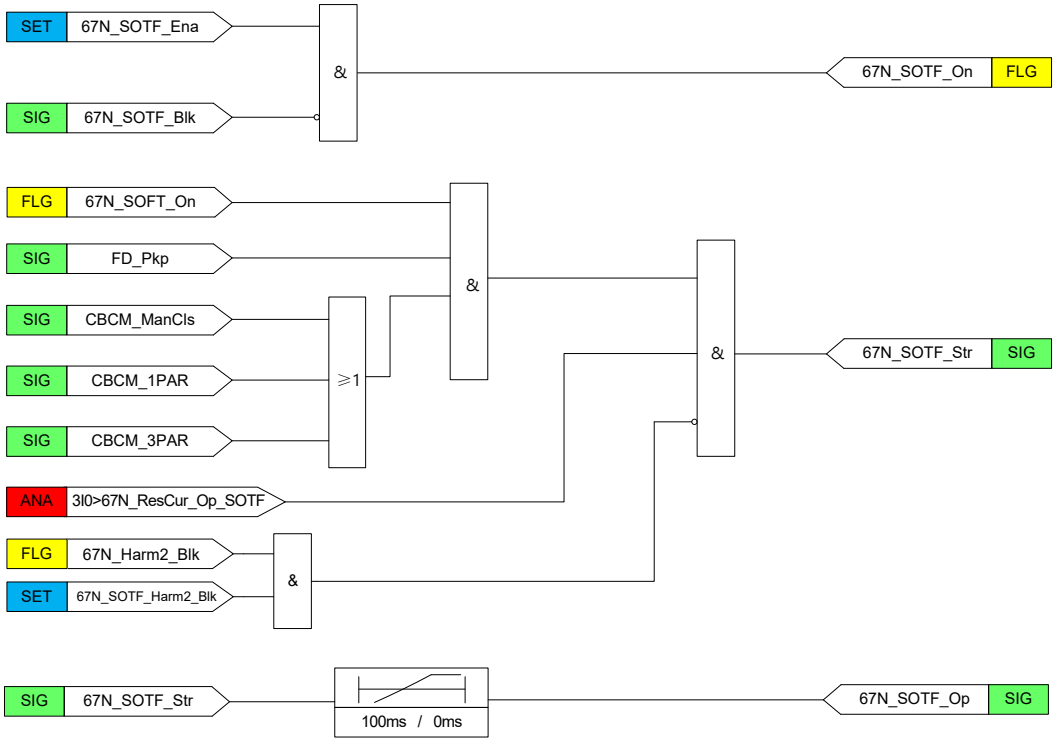


Figure 3.14.1 Logic Diagram of 67NSOTF

3.14.4 Settings

Table 3.14-3 67NSOTF Settings

NO	Name	Range	Unit	Step	Default	Description
1	67N_SOTF_Ena	0 or 1	-	1	0	Enabling/Disabling of the switch onto fault protection of 67N
2	67N_SOTF_Harm2_Blk	0 or 1	-	1	0	Enabling/Disabling the switch onto fault protection of 67N controlled by harmonic control element 0: disable 1: enable
3	67N_ResCur_Op_SOTF	(0.05~30.00)×In	A	0.01	20	Current setting for earth fault protection when switch onto fault

3.15 Directional Negative-sequence Overcurrent Protection 67I2

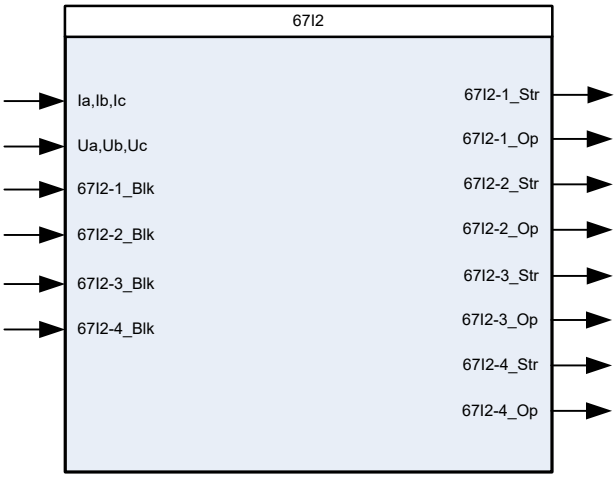
3.15.1 Overview

When an asymmetric short-circuit fault occurs in the power system or the power system is under asymmetrical three-phase operation, the power system will generate negative-sequence current.

Negative-sequence overcurrent will cause generator, motor and other equipment serious damage. Directional negative-sequence overcurrent protection 67I2 has the following characteristics:

- Each of the four stages in 67I2 has independent logic, threshold current, and settable time delays.
- All four stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.
- Direction control element can be set to control all stages of 67I2 protection among three options: non-directional, forward direction and reverse direction.

3.15.1.1 Function Block



3.15.1.2 Signals

Table 3.15-1 67I2 Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	67I2-1_Blk	Block signal of 67I2 stage1
4	67I2-2_Blk	Block signal of 67I2 stage2
5	67I2-3_Blk	Block signal of 67I2 stage3
6	67I2-4_Blk	Block signal of 67I2 stage4

Table 3.15-2 67I2 Output Signals

NO.	Signal	Description
1	67I2-1_Str	Common start signal from stage1
2	67I2-1_Op	Operation signal from stage1
3	67I2-2_Str	Common start signal from stage2
4	67I2-2_Op	Operation signal from stage2

NO.	Signal	Description
5	67I2-3_Str	Common start signal from stage3
6	67I2-3_Op	Operation signal from stage3
7	67I2-4_Str	Common start signal from stage4
8	67I2-4_Op	Operation signal from stage4

3.15.2 Protection Principle

3.15.2.1 Fault detector

Each stage is controlled by the fault detector based on negative-sequence current. Negative-sequence overcurrent protection can operate when the fault detector based on negative-sequence current operate and it is enabled.

3.15.2.2 Negative-sequence Overcurrent Element

The negative-sequence current is pre-processed by a discrete Fourier filter. Thus the phasor of the fundamental frequency component of the negative-sequence current is derived. The phasor magnitude is used within the 67I2 protection to compare it with the set operation current value of the four stages (67I2-x_NegCur_Op, x=1,2,3,4).

If the negative-sequence current is larger than the set operation current and the stage is used in non-directional mode a signal from the comparator for this stage is set to true. This signal will, without delay, activate the output signal 67I2-x_Str (x=1,2,3,4) for this stage.

The operation criterion for each stage of 67I2 protection is:

$$I_2 > 67I2 - \text{x\_NegCur\_Op}$$

Where:

I_2 is the negative-sequence current.

67I2-x_NegCur_Op is the current threshold of stage x (x=1, 2, 3, or 4) of negative-sequence overcurrent protection.

3.15.2.3 Direction Control Element

By setting the characteristic angle 67I2_RCA to determine the most sensitive forward angle of negative-sequence current. The direction check is performed based on the following equation of forward direction:

$$90^\circ \leq \arg\frac{I2 \times \dot{e}^{jRCA}}{U2} \leq 270^\circ$$

Also, it can be calculated by following equation:

$$-90^\circ \leq \text{angle}(I2) + \text{RCA} - \text{angle}(U2) \leq 270^\circ$$

3.15.2.4 Definite-Time Delay

Each stage of 67I2 has a settable definite time delay independently. When the setting 67I2-

x_Op_Curve_Type is set to 0, it means stage x of function 67P has a definite-time delay. The function will give out the operation signal after the setting time 67I2-x_Op_T expires if the stage x of 67I2 picks up.

3.15.2.5 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

User can select the operating characteristic from various inverse-time characteristic curves via setting 67I2-x_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 67I2-x_T_Min, then the operating time of the protection changes to the value of setting 67I2-x_T_Min automatically.

When 67I2-x_Cur_Mul_Ena is set to 1 and inverse-time characteristic is selected, if calculated current is more than Cur_Mul*I_p, then the operating time of the protection changes to the time delay calculated by the fault current I_2=Mul_Cur*I_p automatically.

Where:

Mul_Cur is the setting 67I2-x_Cur_Mul. (x=1, 2, 3, or 4)

I_p is current setting 67I2-x_Cur_Op (x=1, 2, 3, or 4)

It is necessary to consider coordination of the 67I2-x_Cur_Mul and 67I2-x_T_Min settings. The 67I2-x_T_Min should be less than the time delay calculated by the fault current I_2=Mul_Cur*I_p, when 67I2-x_Cur_Mul_Ena is set to 1.

3.15.2.6 Enable and Blocking of the Function

Each stage of 67I2 protection can be blocked when certain abnormal conditions are detected if the setting 67I2-x_Abnor_Blk is set to 1. If 67I2-x_Abnor_Blk is set to 0, 67I2 protection will always start if the negative-sequence overcurrent element picks up disregards of the direction determination result. Abnormal conditions are listed below:

- When the system is under pole disagreement condition, for 1-pole AR, 67I2 will operate. If the logic setting 67I2-x_Abnor_Blk is set to “1”, the stage x of 67I2 will be blocked.
- When manually closing circuit breaker, three phases of the circuit breaker maybe not operate simultaneously, and SOTF protection should operate. If the logic setting 67I2-x_Abnor_Blk is set to “1”, the stage x of 67I2 will be blocked.
- VT circuit failure. If the logic setting 67I2-x_Abnor_Blk is set to “1”, the stage x of 67I2 will be blocked.

67I2 function can be blocked by CT circuit failure alarm signal if the setting 67I2-x_CTS_Blk is set

to 1.

3.15.3 Logic

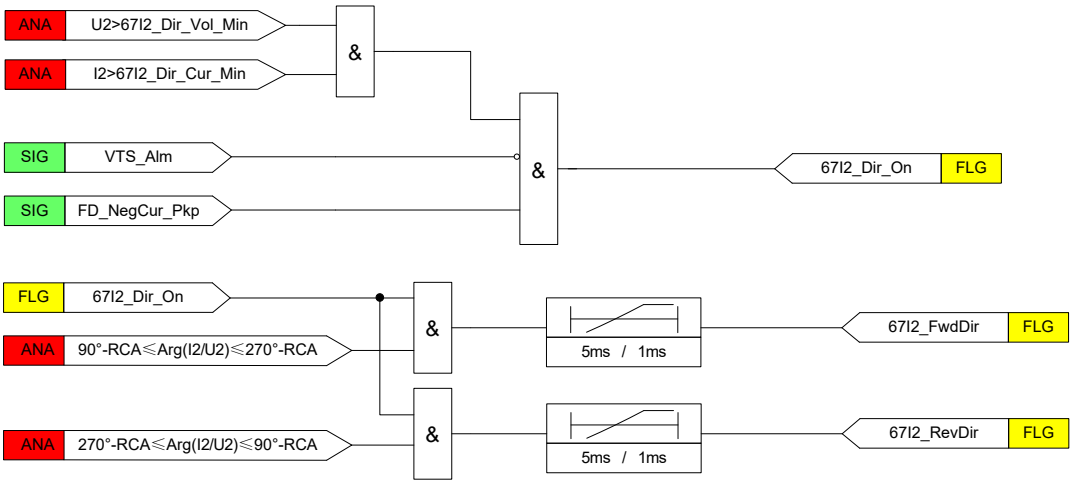


Figure 3.15.1 Logic Diagram for 67I2 Directional Function

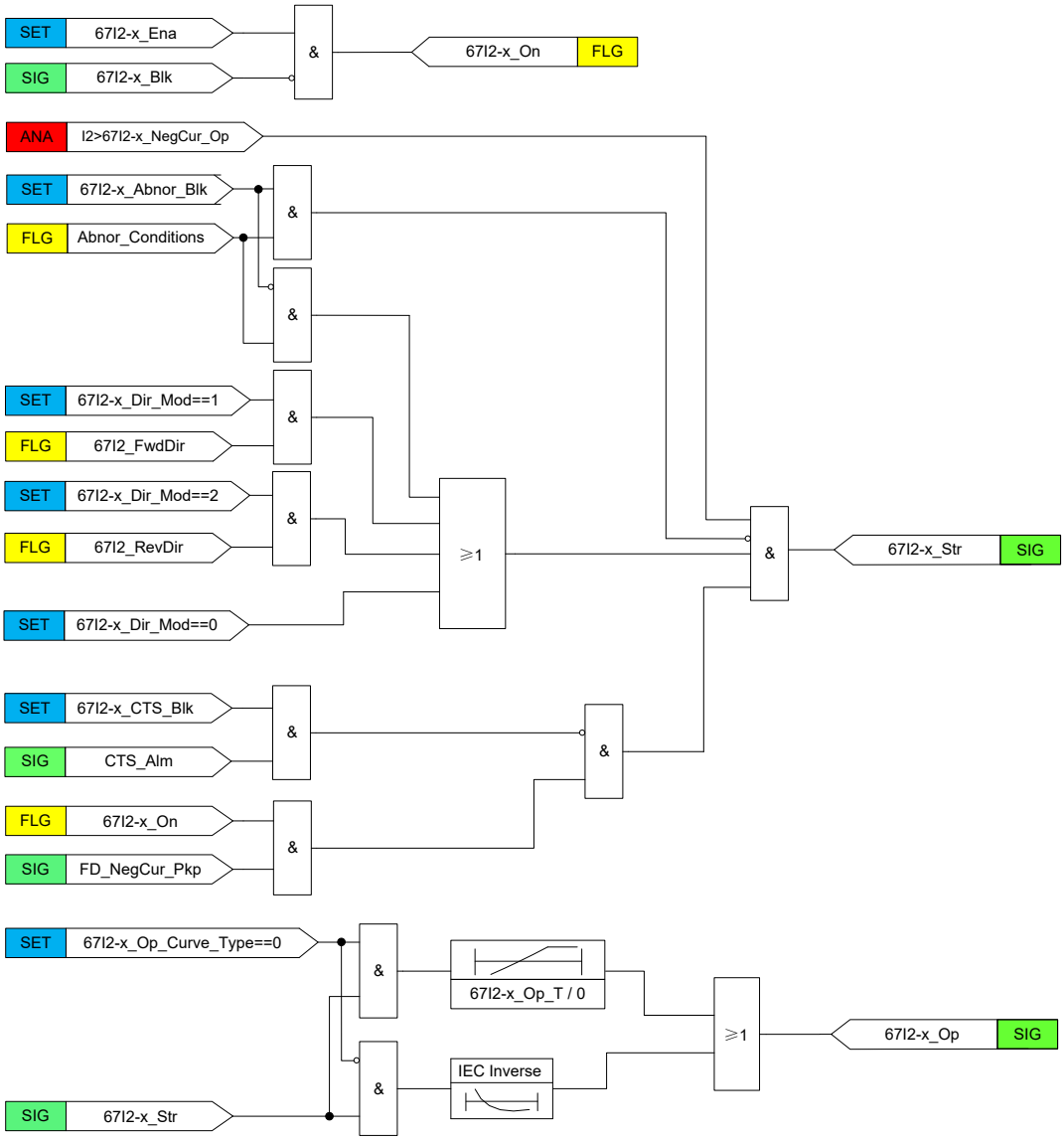


Figure 3.15.2 Logic Diagram of 67I2

3.15.4 Settings

Table 3.15-3 67I2 Settings

NO	Name	Range	Unit	Step	Default	Description
1	67I2_RCA	30~89	deg	0.01	80	The characteristic angle
2	67I2_Dir_Cur_Min	(0.05~1.00) ×In	A	0.01	0.2	The minimum operating current setting of direction control element
3	67I2_Dir_Vol_Min	1.00~10.00	V	0.01	1	The minimum operating voltage setting of direction control element

NO	Name	Range	Unit	Step	Default	Description
4	67I2-x_Ena	0 or 1	-	1	0	Enabling/disabling stage x of negative-sequence overcurrent protection (x=1, 2, 3, 4) 0: disable 1: enable
5	67I2-x_CTS_Blk	0 or 1	-	1	0	Enabling/disabling blocking for stage x of negative-sequence overcurrent protection under CT failure conditions (x=1, 2, 3, 4) 0: disable 1: enable
6	67I2-x_Abnor_Blk	0 or 1	-	1	0	Enabling/disabling blocking for stage x of negative-sequence overcurrent protection under abnormal conditions (x=1, 2, 3, 4) 0: disable 1: enable
7	67I2-x_Cur_Mul_Ena	0 or 1	-	1	0	Enabling/Disabling stage x of negative-sequence overcurrent protection IDMT time delay is calculated by 67I2-x_Cur_Mul. (x=1, 2, 3, 4) 0: disable 1: enable
8	67I2-x_NegCur_Op	(0.05~30.00) ×In	A	0.01	20	Current setting for stage x of negative-sequence overcurrent protection(x=1, 2, 3, 4)
9	67I2-x_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of negative-sequence overcurrent protection(x=1, 2, 3, 4)
10	67I2-x_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time negative-sequence overcurrent protection (x=1, 2, 3, 4)
11	67I2-x_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time negative-sequence protection (x=1, 2, 3, 4)

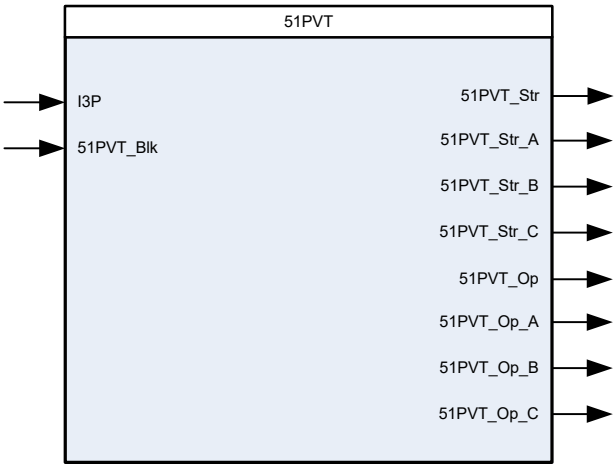
NO	Name	Range	Unit	Step	Default	Description
12	67I2-x_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic negative-sequence protection (x=1, 2, 3, 4)
13	67I2-x_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic negative-sequence protection (x=1, 2, 3, 4)
14	67I2-x_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic negative-sequence protection (x=1, 2, 3, 4)
15	67I2-x_Cur_Mul	20.0~40.0	-	0.1	30	It used to IDMT with I_2=67I2-x_Cur_Mul*Ip, when I_2> 67I2-x_Cur_Mul*Ip, the IDMT time delay is calculated by 67I2-x_Cur_Mul. It is invalid if it is not configured or the 67I2-x_Cur_Mul_Ena is disable. (x=1, 2, 3, 4)
16	67I2-x_Dir_Mod	0~2	-	1	0	Direction option for stage x of negative-sequence overcurrent protection (x=1, 2, 3, 4) 0: Non-directional 1: Forward 2: Reverse
17	67I2-x_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2, 3, 4): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.16 Phase Overcurrent Protection for VT Circuit Failure 51PVT

3.16.1 Overview

When protection VT circuit fails, distance protection will be disabled. As a substitute, definite-time or inverse-time phase overcurrent protection will be enabled automatically.

3.16.1.1 Function Block



3.16.1.2 Signals

Table 3.16-1 51PVT Input Signals

NO.	Signal	Description
1	I3P	Three-phase current input
2	51PVT_Blk	Block signal of the function

Table 3.16-2 51PVT Output Signals

NO.	Signal	Description
1	51PVT_Str	Common start signal
2	51PVT_Str_A	Start signal from phase A
3	51PVT_Str_B	Start signal from phase B
4	51PVT_Str_C	Start signal from phase C
5	51PVT_Op	Operation signal
6	51PVT_Op_A	Operation signal from phase A
7	51PVT_Op_B	Operation signal from phase B
8	51PVT_Op_C	Operation signal from phase C

3.16.2 Protection Principle

3.16.2.1 Phase Overcurrent Element

In the phase overcurrent element, the amplitude of phase current vector I_a, I_b and I_c are compared to the threshold value of 51PVT. The phase overcurrent element will operate when the following criterions are met:

$$I_{\phi} > 51\text{PVT\_Cur\_Op}$$

Where:

I_{ϕ} is the measured phase current.

51PVT_Cur_Op is the current threshold value.

If a phase current is larger than the threshold current, 51PVT_Str_A, 51PVT_Str_B, and 51PVT_Str_C signals are activated without delay. And the signal 51PVT_Str will activate if any of the 51PVT_Str_A, 51PVT_Str_B, and 51PVT_Str_C activates.

3.16.2.2 Definite-Time Delay

When the setting 51PVT_Op_Curve_Type is set to 0, function has definite time delay. The function will give out the operation signal after the setting time delay 51PVT_Op_T if the function start.

3.16.2.3 Inverse-Time Delay Characteristic

The function can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

User can select the operating characteristic from various inverse-time characteristic curves by setting 51PVT_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 51PVT_T_Min, then the operating time of the protection changes to the value of setting 51PVT_T_Min automatically.

When 51PVT_Cur_Mul_Ena is set to 1 and inverse-time characteristic is selected, if calculated current is more than Cur_Mul*I_p, then the operating time of the protection changes to the time delay calculated by the fault current I=Mul_Cur*I_p automatically.

Where:

Mul_Cur is the setting 51PVT_Cur_Mul.

I_p is current setting 51PVT_Cur_Op

It is necessary to consider coordination of the 51PVT_Cur_Mul and 51PVT_T_Min settings. The 51PVT_T_Min should be less than the time delay calculated by the fault current I=Mul_Cur*I_p, when 51PVT_Cur_Mul_Ena is set to 1.

3.16.2.4 Enable and Blocking of the Function

The function is enabled only when VTS alarm occurs and the setting 51PVT_Ena is set to 1. The function can be blocked by the binary input signal 51PVT_Blk.

3.16.3 Logic

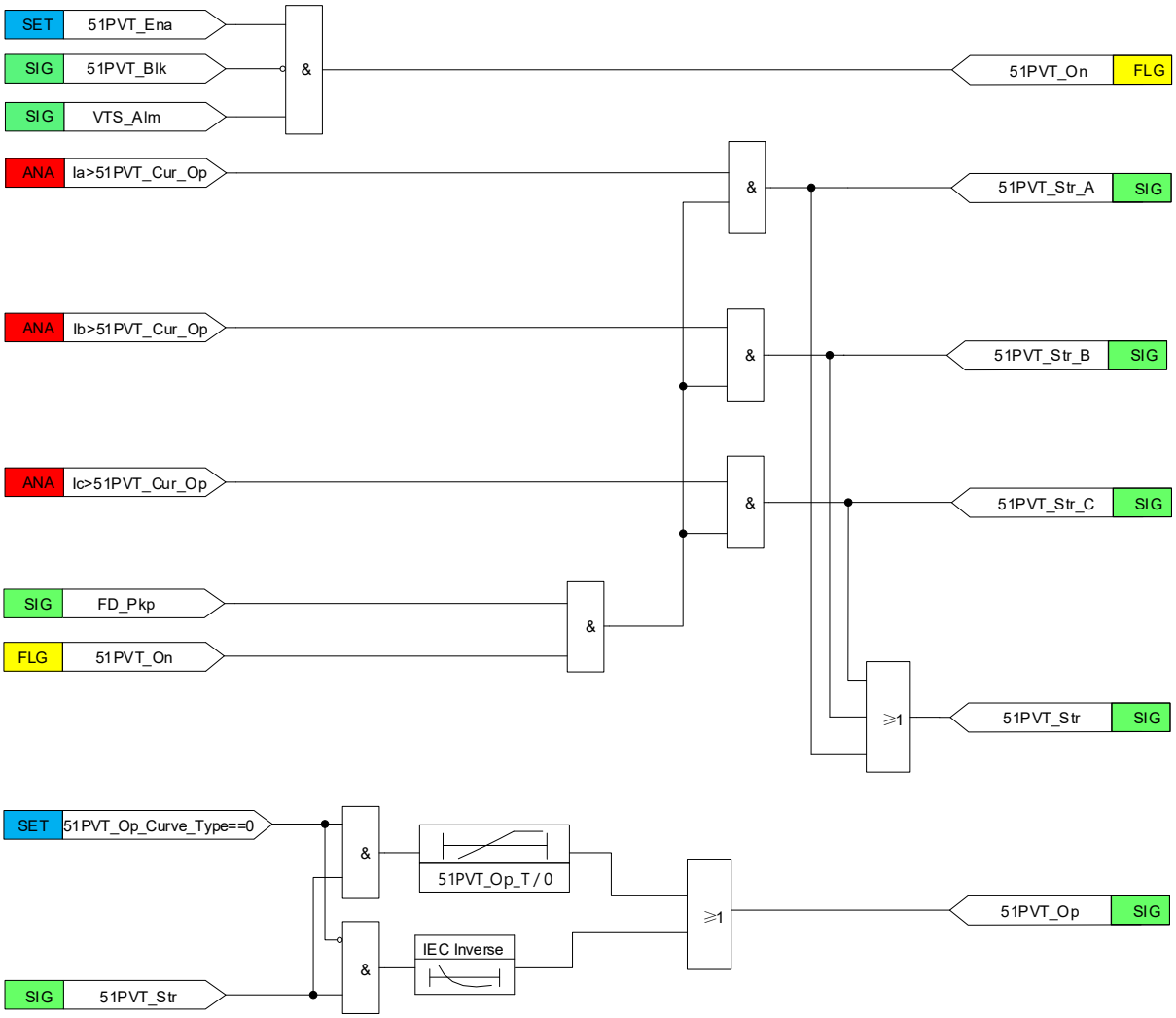


Figure 3.16.1 Logic Diagram for 51PVT

3.16.4 Settings

Table 3.16-3 51PVT Settings

NO	Name	Range	Unit	Step	Default	Description
1	51PVT_Ena	0 or 1	-	1	0	Enabling/disabling of the function 0: disable 1: enable
2	51PVT_Cur_Mul_Ena	0 or 1	-	1	0	Enabling/Disabling of the IDMT time delay is calculated by 51PVT_Cur_Mul. 0: disable

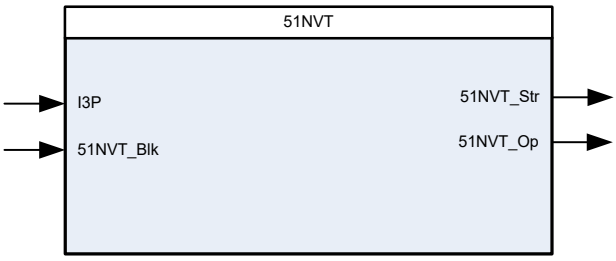
NO	Name	Range	Unit	Step	Default	Description
						1: enable
3	51PVT_Cur_Op	(0.05~30.00)×In	A	0.01	20	Operating current
4	51PVT_Op_T	0.000~100.000	s	0.001	10	Definite Time delay
5	51PVT_T_Mult	0.010~200.000	-	0.001	10	Time multiplier
6	51PVT_T_Min	0.000~60.000	s	0.001	10	Minimum operating time
7	51PVT_Curve_Alpha	0.010~5.000	-	0.001	1	α in customized inverse-time characteristic
8	51PVT_Curve_C	0.000~20.000	-	0.001	0	C in customized inverse-time characteristic
9	51PVT_Curve_K	0.005~200.000	-	0.001	13.5	K in customized inverse-time characteristic
10	51PVT_Cur_Mul	20.0~40.0	-	0.1	30	It used to IDMT with I=51PVT_Cur_Mul*Ip, when I> 51PVT_Cur_Mul*Ip, the IDMT time delay is calculated by 51PVT_Cur_Mul. It is invalid if it is not configured or the 51PVT_Cur_Mul_Ena is disable.
11	51PVT_Op_Curve_Type	1~17	-	1	0	The operation curve type setting: including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.17 Earth Fault Overcurrent Protection for VT Circuit Failure 51NVT

3.17.1 Overview

When protection VT circuit fails, distance protection will be disabled. As a substitute, definite-time or inverse-time zero-sequence overcurrent protection will be enabled automatically.

3.17.1.1 Function Block



3.17.1.2 Signals

Table 3.17-1 51NVT Input Signals

NO.	Signal	Description
1	I3P	Three-phase current input
2	51NVT_Blk	Block signal of the function

Table 3.17-2 51NVT Output Signals

NO.	Signal	Description
1	51NVT_Str	Common start signal
2	51NVT_Op	Operation signal

3.17.2 Protection Principle

3.17.2.1 Zero-sequence Overcurrent Element

In the zero-sequence overcurrent element, the amplitude of zero-sequence current is compared to the threshold value of 51NVT. The overcurrent element will operate when the following criterions are met:

$3I_0 > 51\text{NVT\_Cur\_Op}$

Where:

$3I_0$ is the measured phase current.

51NVT_Cur_Op is the current threshold value.

If zero-sequence current is larger than the threshold current, 51NVT_Str is activated without delay.

3.17.2.2 Definite-Time Delay

When the setting 51NVT_Op_Curve_Type is set to 0, function has definite time delay. The function will give out the operation signal after the setting time delay 51NVT_Op_T if the function start.

3.17.2.3 Inverse-Time Delay Characteristic

The function can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

User can select the operating characteristic from various inverse-time characteristic curves by setting 51NVT_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 51NVT_T_Min, then the operating time of the protection changes to the value of setting 51NVT_T_Min automatically.

When 51NVT_Cur_Mul_Ena is set to 1 and inverse-time characteristic is selected, if calculated current is more than Cur_Mul*I_p, then the operating time of the protection changes to the time delay calculated by the fault current $3I_0$=Mul_Cur*I_p automatically.

Where:

Mul_Cur is the setting 51NVT_Cur_Mul.

I_p is current setting 51NVT_Cur_Op

It is necessary to consider coordination of the 51NVT_Cur_Mul and 51NVT_T_Min settings. The 51NVT_T_Min should be less than the time delay calculated by the fault current $3I_0$=Mul_Cur*I_p, when 51NVT_Cur_Mul_Ena is set to 1.

3.17.2.4 Enable and Blocking of the Function

The function is enabled only when VTS alarm occurs and the setting 51NVT_Ena is set to 1. The function can be blocked by the input signal 51NVT_Blk.

3.17.3 Logic

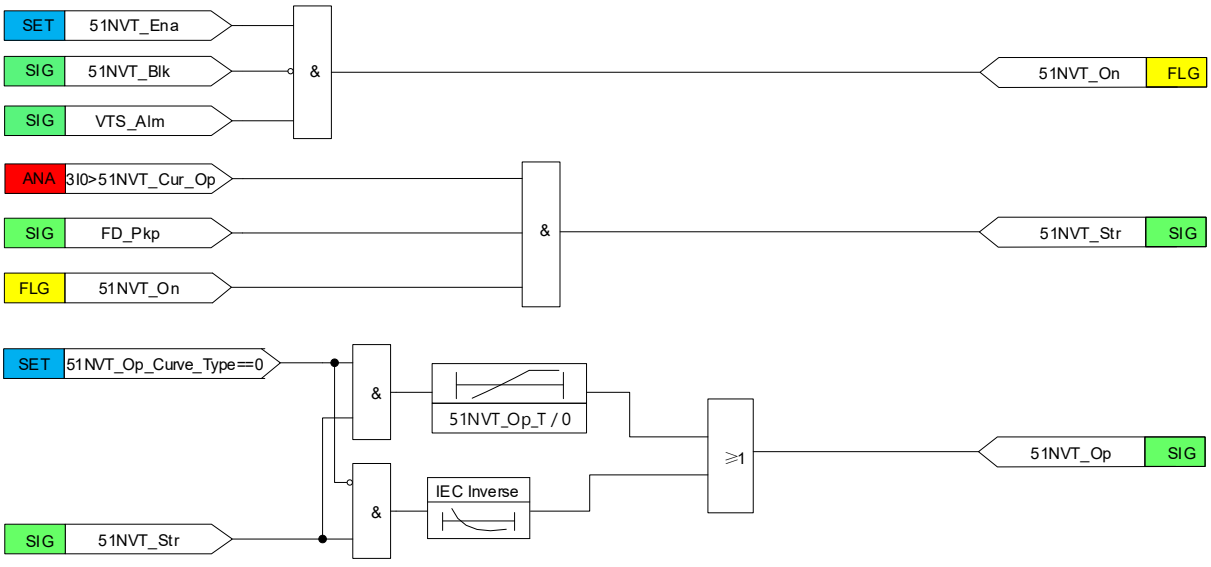


Figure 3.17.1 Logic Diagram for 51NVT

3.17.4 Settings

Table 3.17-3 51NVT Settings

NO	Name	Range	Unit	Step	Default	Description
1	51NVT_Ena	0 or 1	-	1	0	Enabling/disabling of the function 0: disable 1: enable
2	51NVT_Cur_Mul_Ena	0 or 1	-	1	0	Enabling/Disabling of the IDMT time delay is calculated by 51NVT_Cur_Mul. 0: disable 1: enable
3	51NVT_Cur_Op	(0.05~30.00)×In	A	0.01	20	Operating current
4	51NVT_Op_T	0.000~100.000	s	0.001	10	Definite Time delay
5	51NVT_T_Mult	0.010~200.000		0.001	10	Time multiplier
6	51NVT_T_Min	0.000~60.000	s	0.001	10	Minimum operating time
7	51NVT_Curve_Alpha	0.010~5.000	-	0.001	1	α in customized inverse-time characteristic
8	51NVT_Curve_C	0.000~20.000	-	0.001	0	C in customized inverse-time characteristic
9	51NVT_Curve_K	0.005~200.000	-	0.001	13.5	K in customized inverse-time characteristic
10	51NVT_Cur_Mul	20.0~40.0	-	0.1	30	It used to IDMT with $3I_0$=51NVT_Cur_Mul*Ip, when $3I_0$>51NVT_Cur_Mul*Ip, the IDMT time delay is calculated by 51NVT_Cur_Mul. It is invalid if it is not configured or the 51NVT_Cur_Mul_Ena is disable.
11	51NVT_Op_Curve_Type	1~17	-	1	0	The operation curve type setting: including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.18 Breaker Failure Protection 50BF

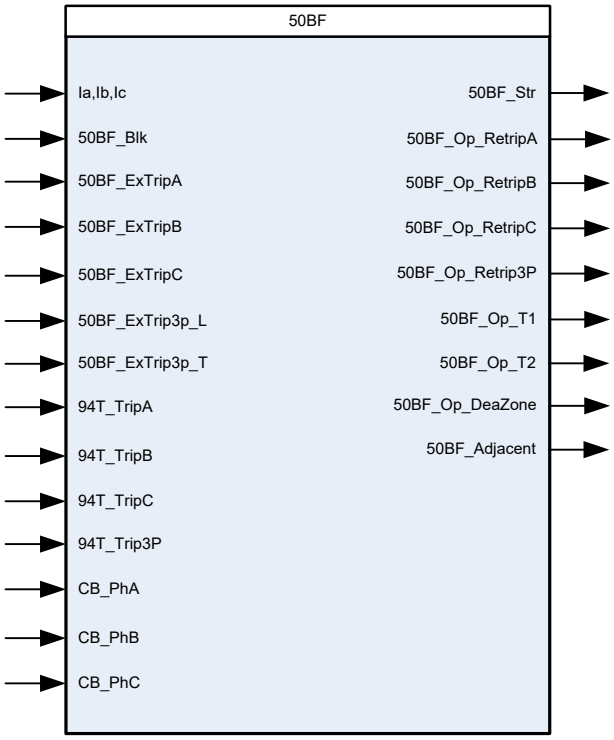
3.18.1 Overview

Breaker failure protection 50BF can provide a backup protection in case of tripping failure of the circuit breaker. It can monitor the tripping of the associated circuit breaker and in a short time trip local and adjacent circuit breaker and ensure stable operation of the entire power grid to prevent equipment in power system from seriously damaged.

The start of 50BF is initiated by the internal protection function operation or by an external signal received from binary input. Along with the start, several current criterions are used to check whether the circuit breaker fails to open.

Generally, fault current is very large when multi-phase fault occurs between CT and circuit breaker (i.e. dead zone) and it will have a greater impact on the system. Breaker failure protection can operate after a longer time delay, in order to clear the dead zone fault quickly and improve the system stability, dead zone protection with shorter time delay (compared with breaker failure protection) is adopted.

3.18.1.1 Function Block



3.18.1.2 Signals

Table 3.18-1 50BF Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	50BF_Blk	Block signal of 50BF
3	50BF_ExTripA	Other trip signal of phase A from binary input

NO.	Signal	Description
4	50BF_ExTripB	Other trip signal of phase B from binary input
5	50BF_ExTripC	Other trip signal of phase C from binary input
6	50BF_ExTrip3p_L	Three-phase line trip signal from binary input
7	50BF_ExTrip3p_T	Transformer three-phase trip signal from binary input
8	94T_TripA	Tripping A-phase circuit breaker
9	94T_TripB	Tripping B-phase circuit breaker
10	94T_TripC	Tripping C-phase circuit breaker
11	94T_Trip3P	Tripping three-phase circuit breaker
12	CB_PhA	Normally closed contact of A-phase of circuit breaker
13	CB_PhB	Normally closed contact of B-phase of circuit breaker
14	CB_PhC	Normally closed contact of C-phase of circuit breaker

Table 3.18-2 50BF Output Signals

NO.	Signal	Description
1	50BF_Str	Start signal of 50BF
2	50BF_Op_RetripA	50BF protection operates to re-trip phase-A circuit breaker
3	50BF_Op_RetripB	50BF protection operates to re-trip phase-B circuit breaker
4	50BF_Op_RetripC	50BF protection operates to re-trip phase-C circuit breaker
5	50BF_Op_Retrip3P	50BF protection operates to re-trip three-phase circuit breaker
6	50BF_Op_T1	Breaker failure protection operates with the first time delay 50BF_Op_T1
7	50BF_Op_T2	Breaker failure protection operates with the second time delay 50BF_Op_T2
8	50BF_Op_DeaZone	Dead zone protection operates
9	50BF_Op_Adjacent	Adjacent three-phase circuit breaker tripping signal from 50BF

3.18.2 Protection Principle

3.18.2.1 Start of the 50BF Function

Internal start:

All protection functions that have to control the local circuit breaker integrated into this device starts the 50BF function. 50BF is started by the tripping of the protection stage. In case of phase selective tripping, the start will also be phase selective. In addition, circuit-breaker failure protection is started with 3-pole tripping of automatic reclosing.

External start:

The signal 50BF_ExTripA/B/C or 50BF_ExTrip3p_L/T received from binary input can be used to

start the function.

3.18.2.2 CB Position Check

A check is performed to decide whether the circuit breaker or the individual circuit breaker pole is closed. The current criterion with a settable threshold is available for this purpose. 50BF prefers the current criterion rather than circuit breaker auxiliary contact signal, for example, CB_Open which can also indicate CB position because the current criterion is most reliable for determining whether the CB or CB pole is closed.

If no current is detected at the start, 50BF will not pick up. When the current begins to flow while the start signal maintains, the function picks up.

Phase current criterions are listed below. A circuit-breaker pole is supposed to be closed, and the current criterion is considered to be fulfilled, as soon as one of the phase currents exceeds the phase current threshold value 50BF_Cur_Op.

$$Ia > 50\text{BF\_Cur\_Op}$$

$$Ib > 50\text{BF\_Cur\_Op}$$

$$Ic > 50\text{BF\_Cur\_Op}$$

In case of an internal three phase re-trip or external line trip, 50BF will pick up as long as one of the three conditions is met.

When the device received an external transformer trip signal, zero-sequence or negative-sequence current criterion can be used to determine the position of the circuit breaker.

$$3I0 > 50\text{BF\_ResCur\_Op}$$

$$I2 > 50\text{BF\_NegCur\_Op}$$

$\mathrm{Ia, Ib, Ic}$ are phase current

50BF_Cur_Op is the setting of phase current threshold

$\mathrm{3I0}$ is the zero-sequence current.

$\mathrm{I2}$ is the negative-sequence current.

50BF_ResCur_Op is the setting of zero-sequence current threshold.

50BF_NegCur_Op is the setting of negative-sequence current threshold.

The zero-sequence and negative-sequence criterion does not conflict with the phase current criterion, but an implement of it, which means when the device received an external transformer trip signal, 50BF will pick up as long as either of the phase current, zero-sequence or negative-sequence criterion could be met if the setting 50BF_NegCur_TP and 50BF_ResCur_TP is set to 1.

Notice that if the setting 50BF_ResCur_SP is set to 1, both phase current and zero-sequence current criterion need to be fulfilled to release the local re-trip signal 50BF_RetripA/B/C or 50BF_Retrip3P.

3.18.2.3 Definite-Time Delay

When 50BF is enabled and the setting 50BF_Retrip is set to 1, tripping 1-pole or 3-pole at the local circuit breaker can be repeated. Operation signal 50BF_RetripA/B/C or 50BF_Retrip3P is released after expiration of the settable time delay 50BF_Retirp_T.

When both the phase-segregated tripping contact from line protection and the corresponding phase overcurrent element operate, or both the three-phase tripping contact and any phase overcurrent element operate, breaker failure protection will send three-phase tripping command to trip local circuit breaker after time delay of 50BF_Op_T1 and trip all adjacent circuit breakers after time delay of 50BF_Op_T2.

3.18.2.4 Enable and Blocking of the Function

Notice that 50BF will not released the re-tripping operation signal if the superimposed or zero-sequence fault detector is not pickup. 50BF can also be blocked when receiving the signal 50BF_Blk.

3.18.2.5 Dead Zone Protection

For some wiring arrangement (for example, circuit breaker is located between CT and the line), if fault occurs between CT and circuit breaker, line protection can operate to trip circuit breaker quickly, but the fault have not been cleared since local circuit breaker is tripped. Here dead zone protection is needed in order to trip relevant circuit breaker.

The criterion for dead zone protection is: when dead zone protection is enabled, binary input of initiating dead zone protection is energized (by default, three-phase tripping signal is used to initiate dead zone protection), if overcurrent element for dead zone protection operates, then corresponding circuit breaker is tripped and three phases normally closed contact of the circuit breaker are energized, dead zone protection will operate to trip adjacent circuit breaker after a time delay.

3.18.3 Logic

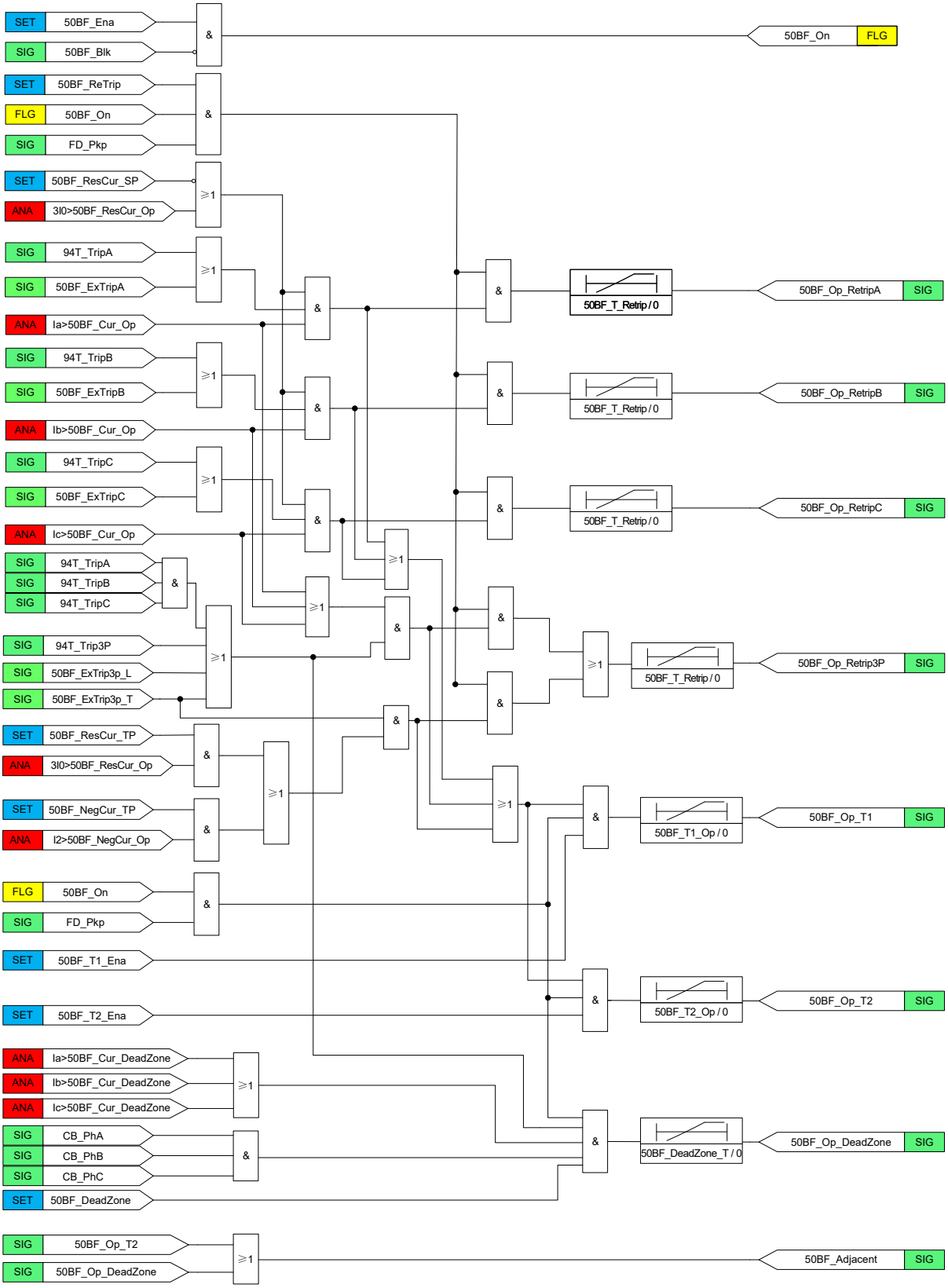


Figure 3.18.1 Logic Diagram of 50BF

3.18.4 Settings

Table 3.18-3 50BF Settings

NO	Name	Range	Unit	Step	Default	Description
1	50BF_Ena	0 or 1	-	1	0	Enabling/disabling breaker failure protection 0: disable 1: enable
2	50BF_ReTrip	0 or 1	-	1	0	Enabling/disabling re-trip function for breaker failure protection 0: disable 1: enable
3	50BF_T1_Ena	0 or 1	-	1	0	Enabling/disabling first time delay for breaker failure protection 0: disable 1: enable
4	50BF_T2_Ena	0 or 1	-	1	0	Enabling/disabling second time delay for breaker failure protection 0: disable 1: enable
5	50BF_DeadZone	0 or 1	-	1	0	Enabling/disabling dead zone function for breaker failure protection 0: disable 1: enable
6	50BF_ResCur_SP	0 or 1	-	1	0	Enabling/disabling zero-sequence current criterion for breaker failure protection initiated by single-phase tripping contact 0: disable 1: enable
7	50BF_ResCur_TP	0 or 1	-	1	0	Enabling/disabling zero-sequence current criterion for breaker failure protection initiated by three-phase tripping contact 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
8	50BF_NegCur_TP	0 or 1	-	1	0	Enabling/disabling negative-sequence current criterion for breaker failure protection initiated by three-phase tripping contact 0: disable 1: enable
9	50BF_Cur_Op	(0.05~30.00) ×In	A	0.01	20	Current setting of phase current criterion for breaker failure protection
10	50BF_ResCur_Op	(0.05~30.00) ×In	A	0.01	20	Current setting of zero-sequence current criterion for breaker failure protection
11	50BF_NegCur_Op	(0.05~30.00) ×In	A	0.01	20	Current setting of negative-sequence current criterion for breaker failure protection
12	50BF_Cur_DeadZone	(0.05~30.00) ×In	A	0.01	20	Current setting of phase current criterion for dead zone function
13	50BF_Retrip_T	0.000~100.000	s	0.001	0.05	Time delay of re-tripping for breaker failure protection
14	50BF_Op_T1	0.000~100.000	s	0.001	0.1	Time delay of first for breaker failure protection
15	50BF_Op_T2	0.000~100.000	s	0.001	0.2	Time delay of second for breaker failure protection
16	50BF_DeadZone_T	0.000~100.000	s	0.001	0.1	Time delay of dead zone function for breaker failure protection

3.19 Thermal Overload Protection 49

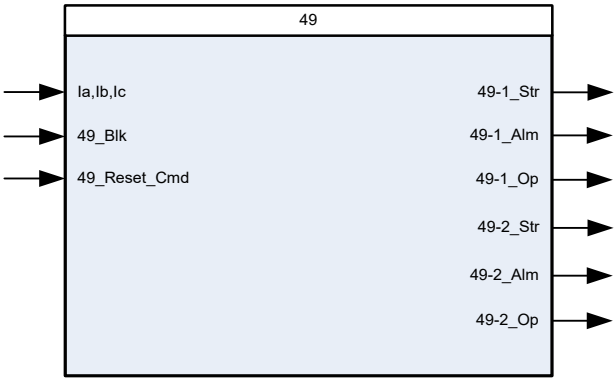
3.19.1 Overview

During overload operation of a transmission line (specially for cable), great current results in greater heat to lead temperature increase and if the temperature reaches too high values the equipment might be damaged.

Thermal overload protection 49 estimates the internal heat content (temperature) continuously. This estimation is made by using a thermal model with two time constants, which is based on current measurement.

When the temperature increases to the alarm value, the protection issues alarm signals to remind the operator for attention, and if the temperature continues to increase to the trip value, the protection sends trip command to disconnect the protected line.

3.19.1.1 Function Block



3.19.1.2 Signals

Table 3.19-1 49 Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three phase current input
2	49_Blk	Blocking signal of 49
3	49_Reset_Cmd	External command to reset the function

Table 3.19-2 49 Output Signals

NO.	Signal	Description
1	49-1_Str	Start signal of 49, stage 1
2	49-1_Alm	Alarm signal from 49, stage 1
3	49-1_Op	Operation signal from 49, stage 1
4	49-2_Str	Start signal of 49, stage 2
5	49-2_Alm	Alarm signal from 49, stage 2
6	49-2_Op	Operation signal from 49, stage 2

3.19.2 Operation Principle

The function provides a thermal overload model which is based on the IEC60255-8 standard. The thermal overload formulas are shown as below:

Cold curve:

$$\mathrm{T} = \tau \times \ln\left(\frac{I^2}{I^2 - k^2 \times I_B^2}\right)$$

Hot curve:

$$\mathrm{T} = \tau \times \ln\left(\frac{I^2 - I_p^2}{I^2 - k^2 \times I_B^2}\right)$$

Where:

T is the operation time delay for each stage.

τ is the thermal time constant of the protected equipment and can be changed via the setting 49_Tau

I_B is the full load current rating related to the setting 49_Cur_Op.

I is the RMS value of the largest phase current.

I_p is the steady state pre-loading before the function start. $I_p = 0$ results in the cold curve.

k is the factor associated to the thermal state formula according to IEC 60255-8, can set by 49-x_K.

The characteristic curve of thermal overload model is shown in the following figure:

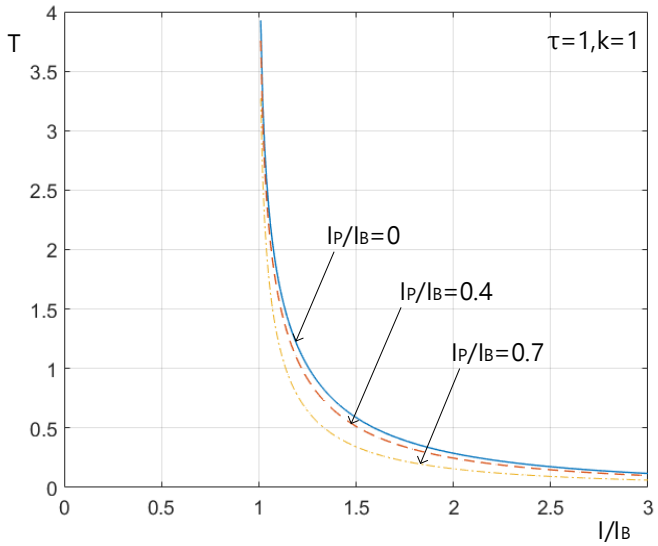


Figure 3.19.1 The characteristic curve of thermal overload model

The characteristic is adopted in the function. The calculation is carried out at zero of Ip, so users need not to set the value of Ip.

Thermal accumulation can be cleared by external input signal 49_Reset_Cmd.

3.19.3 Logic

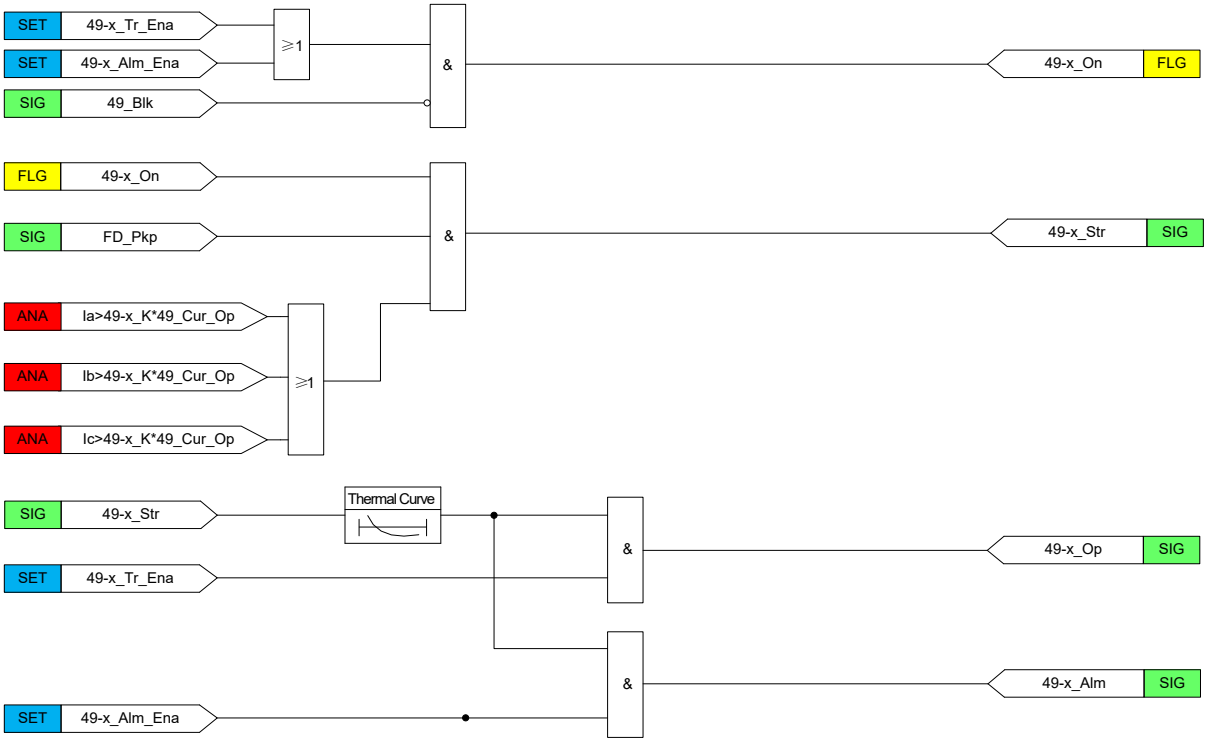


Figure 3.19.2 Logic Diagram of 49

3.19.4 Settings

Table 3.19-3 49 Settings

NO	Name	Range	Unit	Step	Default	Description
1	49_Tau	10~6000	s	1	100	The time constant setting of the IDMT overload protection
2	49_Cur_Op	(0.05~30.00)×In	A	0.01	20	The reference current setting of the thermal overload protection
3	49-1_Tr_Ena	0 or 1	-	1	0	Enabling/disabling of thermal overload protection, stage 1 for trip purpose 0: disable 1: enable
4	49-1_Alm_Ena	0 or 1	-	1	0	Enabling/disabling of thermal overload protection, stage 1 for alarm purpose 0: disable 1: enable
5	49-1_K	0.10~4.00	-	0.01	1	The factor setting for stage 1 of thermal overload protection which is associated to the thermal state formula

NO	Name	Range	Unit	Step	Default	Description
6	49-2_Tr_Ena	0 or 1	-	1	0	Enabling/disabling of thermal overload protection, stage 2 for trip purpose 0: disable 1: enable
7	49-2_Alm_Ena	0 or 1	-	1	0	Enabling/disabling of thermal overload protection, stage 2 for alarm purpose 0: disable 1: enable
8	49-2_K	0.10~4.00	-	0.01	1	The factor setting for stage 2 of thermal overload protection which is associated to the thermal state formula

3.20 Stub Differential Protection 87STB

3.20.1 Overview

The stub differential protection 87STB is to protect the zone between two current transformers and the line isolation switch. It is mainly applied to $1\frac{1}{2}$ circuit breaker layouts in 500kV or above voltage level power systems.

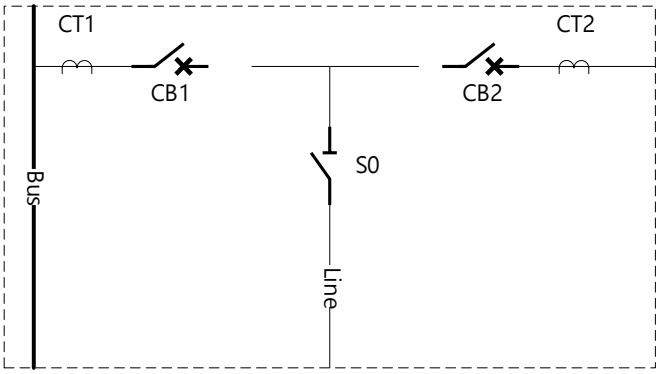
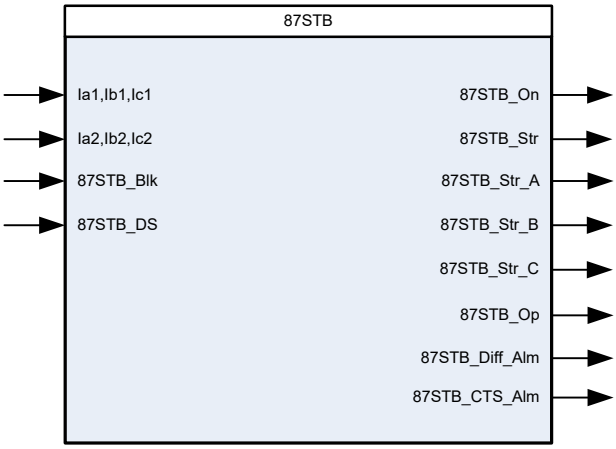


Figure 3.20.1

3.20.1.1 Function Block



3.20.1.2 Signals

Table 3.20-1 87STB Input Signals

NO.	Signal	Description
1	Ia1,Ib1,Ic1	Three-phase current from the first set of current transformer
2	Ia2,Ib2,Ic2	Three-phase current from the second set of current transformer
3	87STB_Blk	Blocking signal of 87STB
4	87STB_DS	Normally closed auxiliary contact of line disconnector

Table 3.20-2 87STB Output Signals

NO.	Signal	Description
1	87STB_On	Stub differential protection is enabled
2	87STB_Str	Start signal of 87STB
3	87STB_Str_A	Start signal from phase A
4	87STB_Str_B	Start signal from phase B
5	87STB_Str_C	Start signal from phase C
6	87STB_Op	Operation signal of 87STB
7	87STB_Diff_Alm	Alarm signal of differential current overreach from 87STB
8	87STB_CTS_Alm	Alarm signal of CT failure from 87STB

3.20.2 Operation Principle

3.20.2.1 Current Differential Protection Element

87STB uses the differential protection scheme to decide whether a fault is within the protection zone. The criterion of the differential protection is shown in the following equations:

$$\begin{cases} I_{Diff\,\phi} > 87STB\_Slope \times I_{Bias\,\phi} \\ I_{Diff\,\phi} > 87STB\_Cur\_Op \end{cases}$$

Where:

$I_{Diff\phi}$: The phase differential current($I_{Diff\phi} = \left|\dot{I}_{1\phi} + \dot{I}_{2\phi}\right|$)

$I_{Bias\phi}$: The phase restraint current($I_{Bias\phi} = \left|\dot{I}_{1\phi} - \dot{I}_{2\phi}\right|$)

The operation characteristics of the differential protection scheme are shown in the following figure:

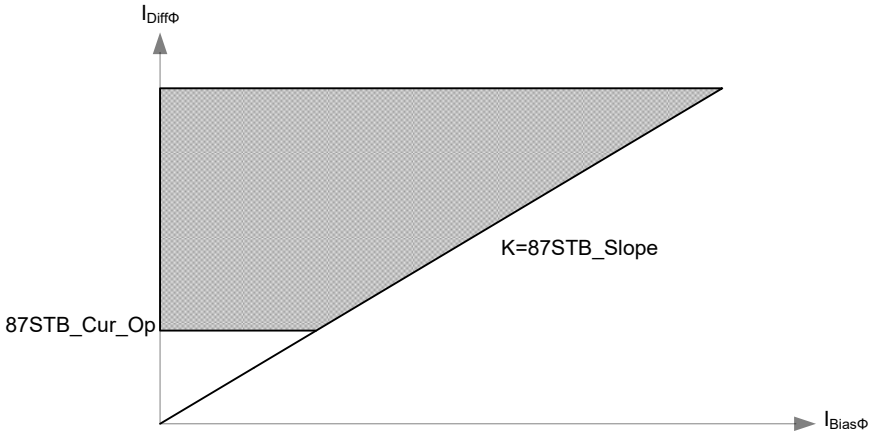


Figure 3.20.2 The operation characteristics of the differential protection scheme

3.20.2.2 CT Circuit Failure Detection

Without taking into account three-phase CT failure and simultaneous CT failure at both sides, in order to avoid judgment error of CT failure block caused by out-of-balance zero-sequence current of heavy-load current, the difference in CT characteristics between the two sides and the error caused by "null shift" at light-load current, CT failure is identified using the following criteria:

$$\left(3I_{0,1} - I_{OSET}\right) \times \left(3I_{0,2} - I_{OSET}\right) < 0$$

$$I_{OSET} = \left(0.1I_N, FD\_ResCur\_Str\right)_{min}$$

Where:

FD_ResCur_Str is the current setting of residual current fault detector element.

$3I_{0,1}$ is the calculated residual current of CT1

$3I_{0,2}$ is the calculated residual current of CT2

If the criterion is satisfied, the function will issue the CTS alarm with a 10 seconds delay. After the CT error disappears, the alarm will be cancelled after a 10 seconds delay.

3.20.2.3 Differential Current Overreach Alarm

In order to prevent the false trip caused by a failure of the device's AC input and data acquisition system, if the following operation criterion is met, and the differential protection doesn't operate, the function will issue the alarm with a 5 seconds delay. The alarm has no effect on the differential

protection function.

$$\begin{cases} I_{Diff\,\phi} > 0.15 \times I_{Bias\,\phi} \\ I_{Diff\,\phi} > 87STB\_Cur\_Alm \end{cases}$$

3.20.3 Logic

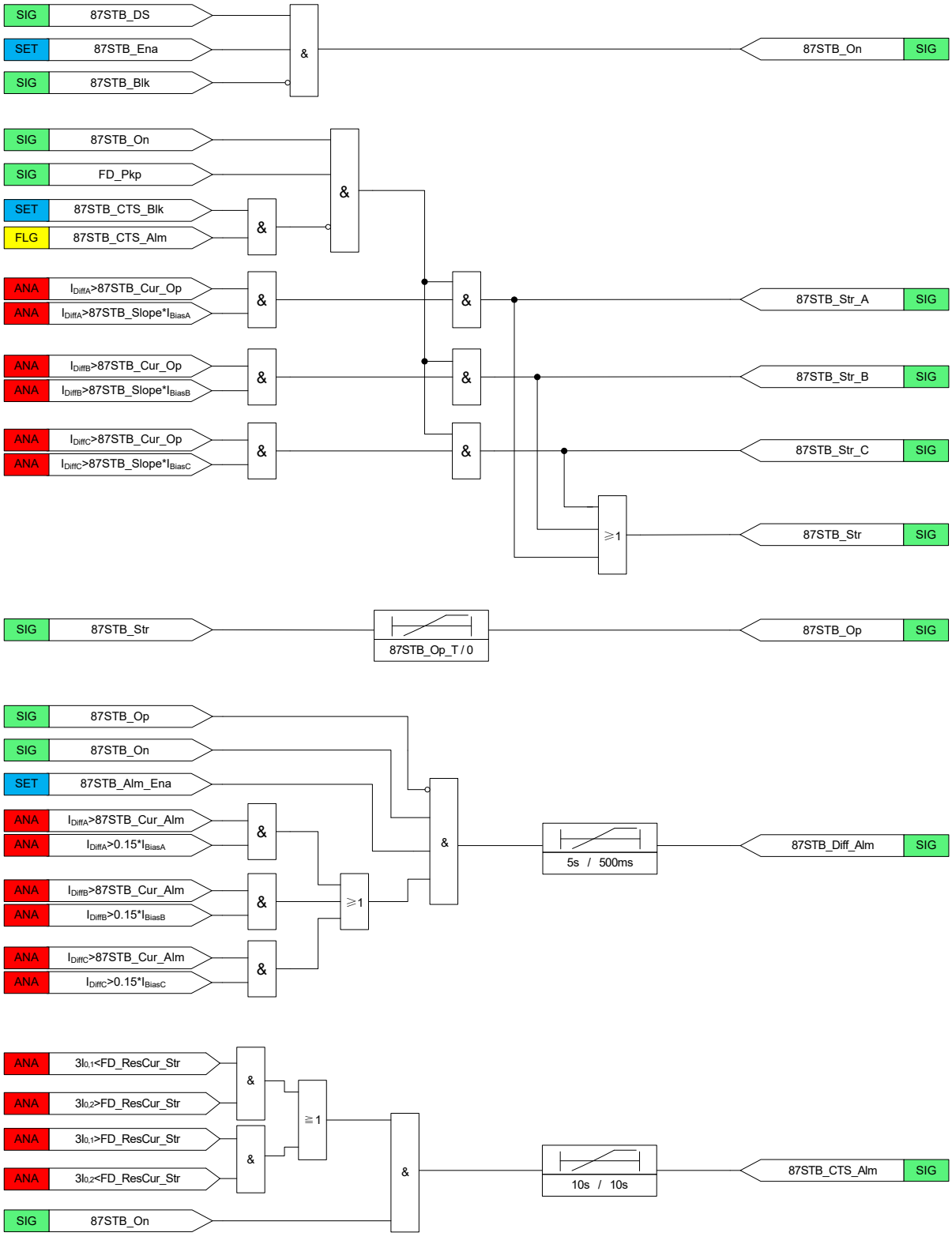


Figure 3.20.3 Logic Diagram of 87STB

3.20.4 Settings

Table 3.20-3 87STB Settings

NO	Name	Range	Unit	Step	Default	Description
1	87STB_Ena	0 or 1	-	1	0	Enabling/disabling stub differential protection 0: disable 1: enable
2	87STB_Alm_Ena	0 or 1	-	1	0	Enabling/disabling differential current alarm function 0: disable 1: enable
3	87STB_CTS_Blk	0 or 1	-	1	0	Enabling/disabling stub differential protection controlled by CT circuit failure 1: enable 0: disable
4	87STB_Cur_Op	(0.05~30.00)×In	A	0.01	20	Threshold current setting for differential current element
5	87STB_Cur_Alm	(0.05~30.00)×In	A	0.01	20	Current setting of differential current alarm
6	87STB_Slope	0.50~1.00	-	0.01	0.6	The slope of the characteristic curve in differential current element
7	87STB_Op_T	0.000~100.000	s	0.001	10	Time delay for stub differential protection

3.21 Pole Discordance Protection 52PD

3.21.1 Overview

The pole discordance of circuit breaker may occur during operation of a breaker with segregated operating gears for the three phases. The reason could be an interruption in the tripping/closing circuits, or mechanical failure. An open phase can cause negative and zero sequence currents which cause thermal stress on generator or motor and can cause unwanted operation of zero sequence or negative sequence current functions. Pole discordance protection 52PD is required to operate when pole discordance condition occurs.

3.21.1.1 Function Block

3.21.1.2 Signals

Table 3.21-1 52PD Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	52PD_Blk	Block signal of 52PD

Table 3.21-2 52PD Output Signals

NO.	Signal	Description
1	52PD_Str	Start signal from 52PD
2	52PD_Op	Operation signal from 52PD

3.21.2 Operation Principle

3.21.2.1 CB Position Check

A check is performed to decide whether the circuit breaker or the individual circuit breaker pole is in open position. 52PD function receives the signals CBCM_Phx_Open(x=A,B,C) from the CB position supervision function. Circuit breaker pole x is considered in open position if the signal CBCM_Phx_Open is equal to 1. 52PD will not start if all the three circuit breaker poles are in the open position.

Additional residual and negative-sequence current criterions are used in the function to detect pole discrepancy conditions:

$$3I0 > 52\text{PD\_ResCur\_Op}$$

$$I2 > 52\text{PD\_NegCur\_Op}$$

$3I0$ is three times zero-sequence current

52PD_ResCur_Op is the setting of residual current threshold

$I2$ is the negative-sequence current.

52PD_NegCur_Op is the setting of negative-sequence current threshold.

At least one of the above criterions has to be met so 52PD function can issued the start signal if the setting 52PD_3I0/I2_Ena is set to 1. The *3I0* and *I2* criterions will be ignored if a CTS_Alm

signal is received.

3.21.2.2 Definite-Time Delay

52PD has a settable definite time delay which means the function will give out the operation signal when the setting time 52PD_Op_T expires after start.

3.21.3 Logic

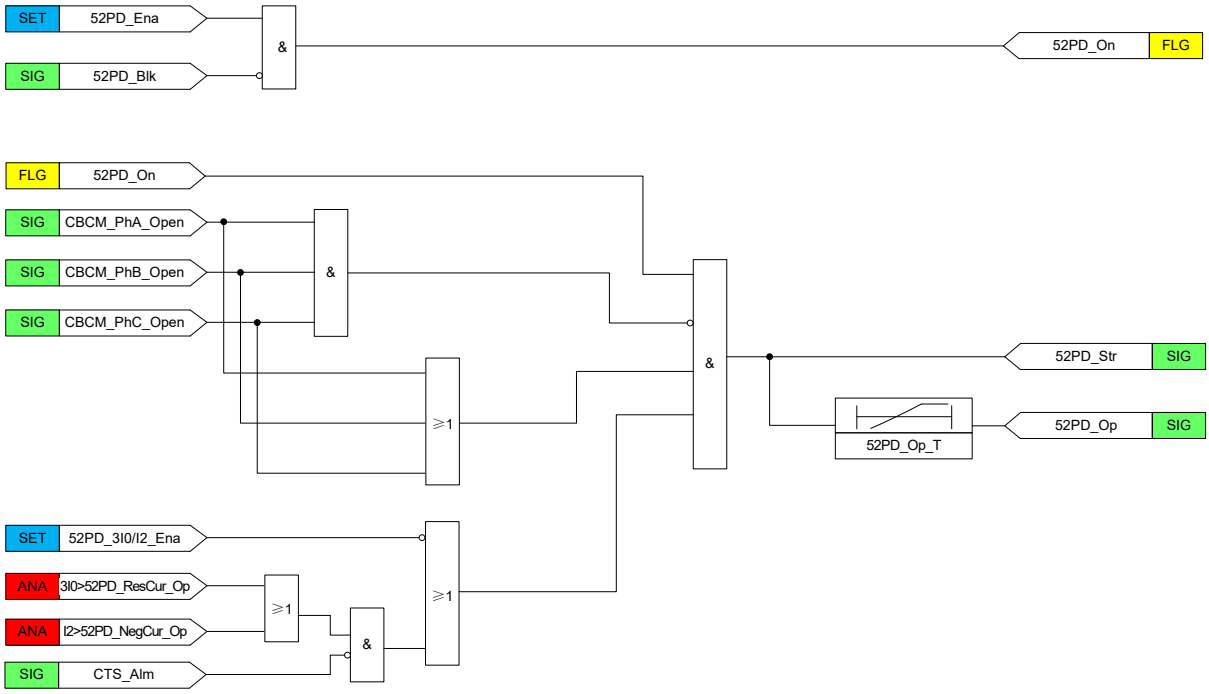


Figure 3.21.1 Logic Diagram of 32R

3.21.4 Settings

Table 3.21-3 52PD Settings

NO	Name	Range	Unit	Step	Default	Description
1	52PD_Ena	0 or 1	-	1	0	Enabling/disabling of pole discordance protection 0: disable 1: enable
2	52PD_3I0/I2_Ena	0 or 1	-	1	0	Enabling/disabling residual current criterion and negative-sequence current criterion for pole discordance protection 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
3	52PD_ResCur_Op	(0.05~30.00)×In	A	0.01	20	Current setting of zero-sequence current criterion for pole discordance protection
4	52PD_NegCur_Op	(0.05~30.00)×In	A	0.01	20	Current setting of negative-sequence current criterion for pole discordance protection
5	52PD_Op_T	0.000~100.000	s	0.001	1	Definite Time delay for pole discordance protection

3.22 Reverse Power Protection 32R

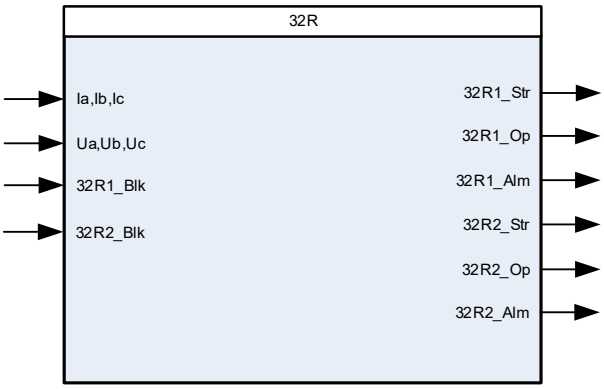
3.22.1 Overview

The main operating function of Reverse Power Protection (32R) is to continuously check the power flow of electric supply and if the power flow of electric supply isn't in define direction then its causes many malfunction like:

- Synchronous generator works as motor
- Interrupt the parallel operation of power grid and power plant turbines.

In order to make sure the system stability and prevent system from any kind of reverse power malfunction damages, reverse power protection 32R should be configured.

3.22.1.1 Function Block



3.22.1.2 Signals

Table 3.22-1 32R Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	32R1_Blk	Block signal of 32R, stage 1
4	32R2_Blk	Block signal of 32R, stage 2

Table 3.22-2 32R Output Signals

NO.	Signal	Description
1	32R1_Str	Start signal from 32R, stage 1
2	32R1_Op	Operation signal from 32R, stage 1
3	32R1_Alm	Alarm signal from 32R, stage 1
4	32R2_Str	Start signal from 32R, stage 2
5	32R2_Op	Operation signal from 32R, stage 2
6	32R2_Alm	Alarm signal from 32R, stage 2

3.22.2 Operation Principle

Reverse power protection provides two stages: each stage can be set as alarm purpose or tripping purpose via the setting 32R_Alm. When reverse power value of the generator detected is greater than reverse power protection setting 32Rx_Power_Op, reverse power protection can operate to alarm or trip with the setting time delay 32Rx_T_Tr or 32Rx_T_Alm.

Generator power is calculated by three-phase voltage and three-phase current of generator terminal. Positive sequence component of active power is calculated by fundamental wave of the voltage and current.

When the protection device is installed on the power plant side, reverse power is a negative value, and reverse power is a positive value when it is installed on the substation side.

The operation criterion is shown below:

$$32\text{R\_Dir\_Mod} == 2 \wedge \text{P} < -32\text{Rx\_Power\_Op}$$

Or

$$32\text{R\_Dir\_Mod} == 1 \wedge \text{P} > 32\text{Rx\_Power\_Op}$$

Where:

P1 is the positive sequence active power.

3.22.3 Logic

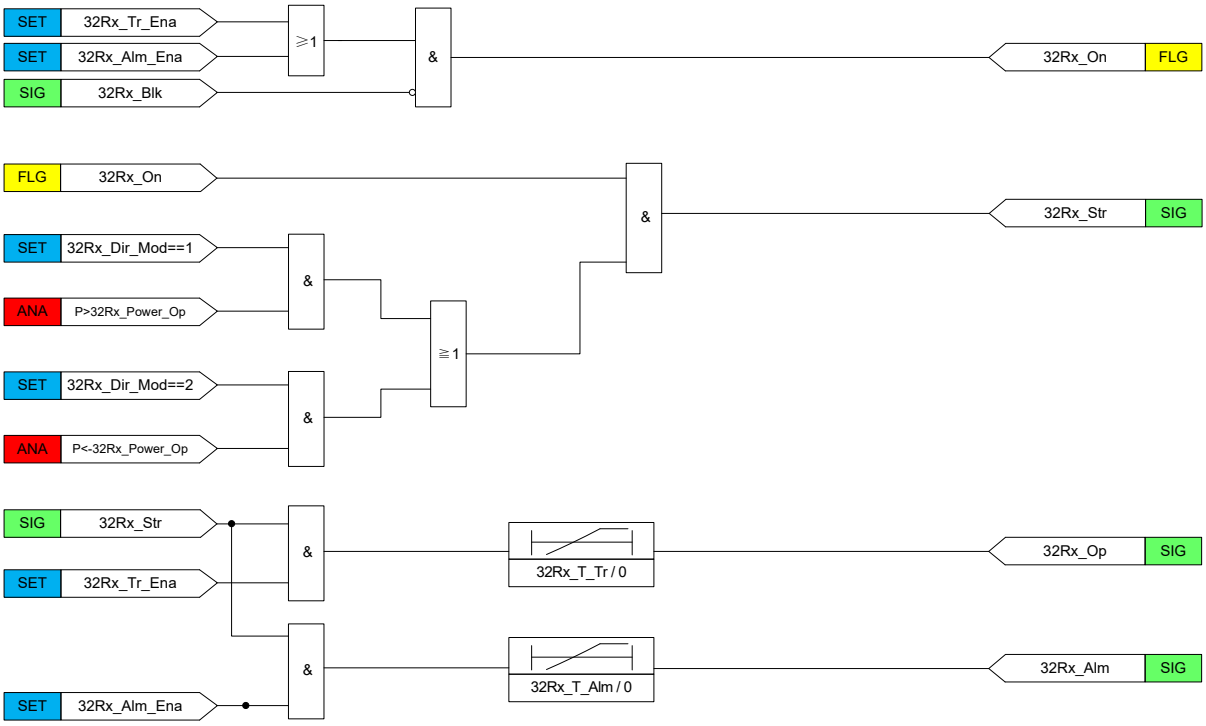


Figure 3.22.1 Logic Diagram of 32R

3.22.4 Settings

Table 3.22-3 32R Settings

NO	Name	Range	Unit	Step	Default	Description
1	32R1_Tr_Ena	0 or 1	-	1	0	Enabling/disabling stage 1 of reverse power protection for trip purpose 0: disable 1: enable
2	32R1_Alm_Ena	0 or 1	-	1	0	Enabling/disabling stage 1 of reverse power protection for alarm purpose 0: disable 1: enable
3	32R1_Dir_Mod	1: Forward 2: Reverse	-	1	1	Direction option for stage 1 of reverse power protection
4	32R1_Power_Op	0.10~900.00	W	0.01	20	Power setting of stage 1 of reverse power protection It should be greater 0.5 times the measured value of reverse power.
5	32R1_T_Tr	0.100~600.000	s	0.001	1	Definite Time delay for stage 1 of reverse power protection to operate

NO	Name	Range	Unit	Step	Default	Description
6	32R1_T_Alm	0.100~600.000	s	0.001	1	Definite Time delay for stage 1 of reverse power protection to issue the alarm signal
7	32R2_Tr_Ena	0 or 1	-	1	0	Enabling/disabling stage 2 of reverse power protection for trip purpose 0: disable 1: enable
8	32R2_Alm_Ena	0 or 1	-	1	0	Enabling/disabling stage 2 of reverse power protection for alarm purpose 0: disable 1: enable
9	32R2_Dir_Mod	1: Forward 2: Reverse	-	1	1	Direction option for stage 2 of reverse power protection
10	32R2_Power_Op	0.10~900.00	W	0.01	20	Power setting of stage 2 of reverse power protection It should be greater 0.5 times the measured value of reverse power.
11	32R2_T_Tr	0.100~600.000	s	0.001	1	Definite Time delay for stage 2 of reverse power protection to operate
12	32R2_T_Alm	0.100~600.000	s	0.001	1	Definite Time delay for stage 2 of reverse power protection to issue the alarm signal

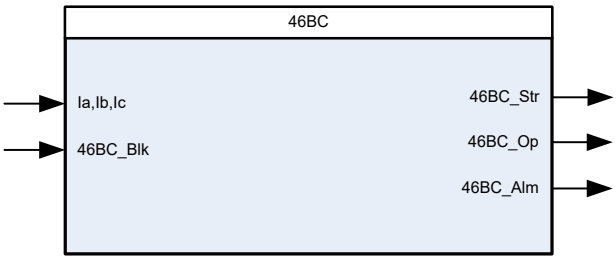
3.23 Broken Conductor Protection 46BC

3.23.1 Overview

The main function of broken conductor protection 46BC is to continuously monitor the transmission line conductor conductivity. When the broken conductor situation is happening in transmission line (single phase or two phase conductor broken) the conductivity of line are changed and it will change the ratio between negative sequence current and positive sequence current (I1/I2).

The operating criteria of Broken Conductor Protection 46BC is the ratio between negative and positive sequence current with definite time delay (DT). Under normal operating condition the ratio of negative and positive sequence current is under set define range and CT measuring circuit works normally. During abnormal condition the system detect CT fault and the ratio of negative and positive sequence is greater than set value and IED system detect conductor broken fault and Broken Conductor Protection 46BC will operate and isolate that line.

3.23.1.1 Function Block



3.23.1.2 Signals

Table 3.23-1 46BC Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	46BC_Blk	Blocking signal of 46BC

Table 3.23-2 46BC Output Signals

NO.	Signal	Description
1	46BC_Str	General start signal of 46BC
2	46BC_Op	Operation signal from 46BC
3	46BC_Alm	Alarm signal from 46BC

3.23.2 Protection Principle

3.23.2.1 Operation Mode

The function can be used for alarm purpose only. If the setting 46BC_Alm_Ena is set to 1. The function will give out the alarm signal instead of the operation signal if the operation conditions are met.

3.23.2.2 Unbalanced Broken Conductor Fault

Broken-conductor fault is difficult to detect since there is no increase of any phase current but negative-sequence current, so negative-sequence current can be used in the broken-conductor protection. However, under heavy load condition, negative-sequence current due to unbalanced load may be larger than the negative-sequence current caused by broken conductor fault under light load condition. Therefore, 46BC protection use the ratio of negative-sequence current and positive-sequence current to detect broken conductor fault.

In single-phase conductor broken fault:

$$\frac{I_2}{I_1} = \frac{Z_0}{Z_0 + Z_2}$$

Where:

I_2 is the negative-sequence current.

I_1 is the positive-sequence current.

Z_0 is zero-sequence impedance.

Z_2 is negative-sequence impedance.

Usually the zero-sequence impedance in the power system is larger than the positive-sequence impedance, so I_2/I_1>0.5.

In two-phase conductors broken fault, $I_2 = I_1$.

3.23.2.3 Overcurrent Element

I2/I1 ratio overcurrent element:

The *I2/I1* ratio overcurrent element will operate if the following criterions are met:

$$\frac{I_2}{I_1} > 46\text{BC\_Cur\_Op\_I2/I1}$$

Where:

46BC_Cur_Op_I2/I1 is the threshold value for *I2/I1.*

Phase overcurrent element:

The phase overcurrent element will operate if the following criterions are met:

$$I_{ph} > 46\text{BC\_Cur\_Op\_Min}$$

Where:

I_{ph} is the amplitude of input current vector in phase A, phase B or phase C.

46BC_Cur_Op_Min is the current threshold setting.

3.23.2.4 Definite-time Delay Element

46BC has a settable definite time delay. If the current ratio and any phase current stay above the set value for a time period corresponding to the function's set time delay and no other blocking signals received, the operation or alarm signal is issued.

The definite-time delay can be changed via the setting 46BC_Op_T.

3.23.3 Logic

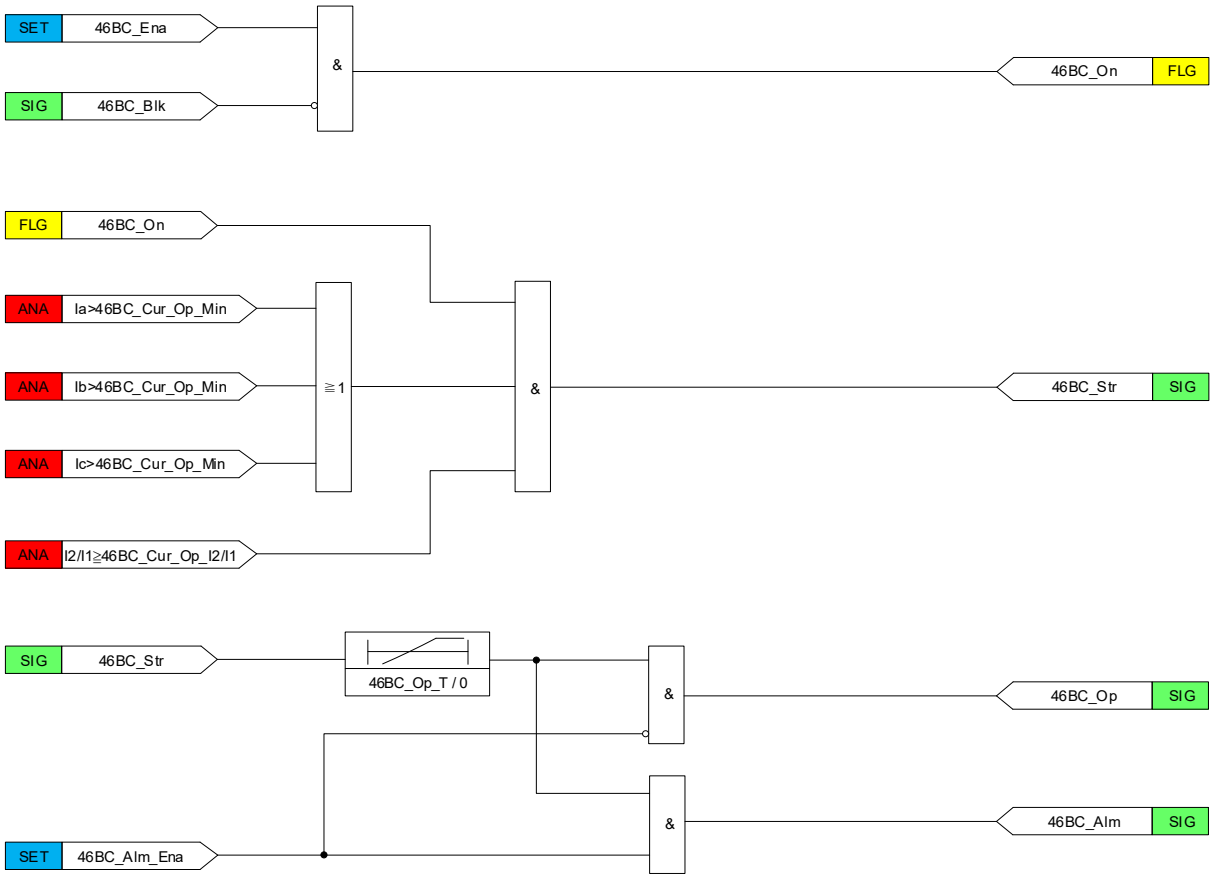


Figure 3.23.1 Logic Diagram of 46BC

3.23.4 Settings

Table 3.23-3 46BC Settings

NO	Name	Range	Unit	Step	Default	Description
1	46BC_Ena	0 or 1	-	1	0	Enabling/disabling of broken conductor protection 0: disable 1: enable
2	46BC_Alm_Ena	0 or 1	-	1	0	Enabling/disabling of broken conductor protection for alarm purpose 0: disable 1: enable
3	46BC_Cur_Op_Min	(0.05~30.00)×In	A	0.01	20	Minimum current for broken conductor protection to operate

NO	Name	Range	Unit	Step	Default	Description
4	46BC_Cur_Op_I2/I1	0.20~1.00	-	0.01	0.6	Threshold ratio between I2 and I1 for broken conductor protection to operate
5	46BC_Op_T	0.000~600.000	s	0.001	1	Time delay of broken conductor protection

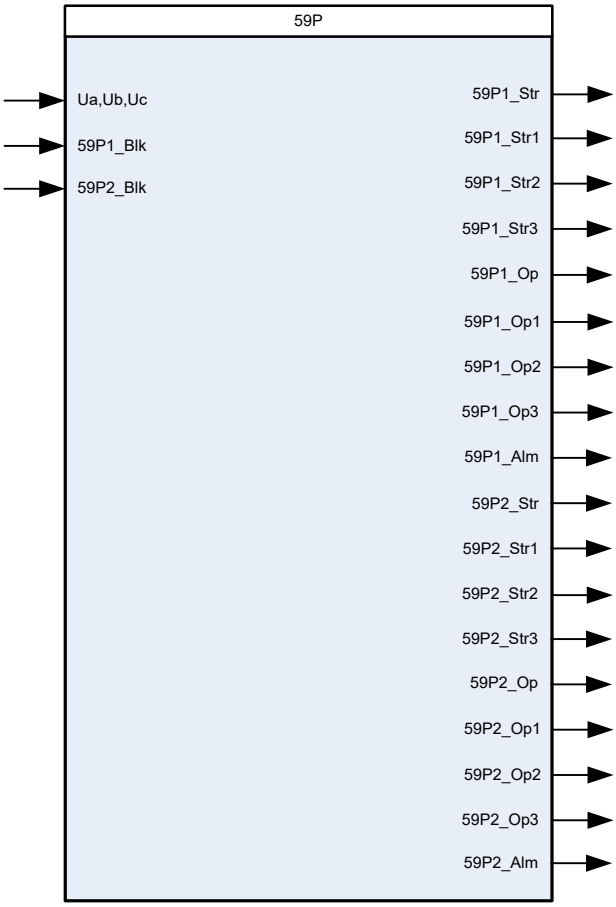
3.24 Three Phase Overvoltage Protection 59P

3.24.1 Overview

Three phase overvoltage protection 59P prevents voltage from rising and causing damage to electrical equipment. 59P protection can be used for tripping purpose as well as to alarm purpose. 59P protection has the following characteristics:

- Both of the two stages in 59P have independent logic, voltage threshold, and settable time delays.
- All stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.
- “1 out of 3” or “3 out of 3” operating mode can be selected via the setting.
- Both phase-to-ground and phase-to-phase voltage can be used in the overvoltage relay.

3.24.1.1 Function Block



3.24.1.2 Signals

Table 3.24-1 59P Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	59P1_Blk	Block signal of 59P stage1
3	59P2_Blk	Block signal of 59P stage2

Table 3.24-2 59P Output Signals

NO.	Signal	Description
1	59P1_Str	Common start signal from stage1
2	59P1_Str1	Start signal from stage1 phase A or AB
3	59P1_Str2	Start signal from stage1 phase B or BC
4	59P1_Str3	Start signal from stage1 phase C or CA
5	59P1_Op	Operation signal from stage1
6	59P1_Op1	Operation signal from stage1 phase A or AB
7	59P1_Op2	Operation signal from stage1 phase B or BC
8	59P1_Op3	Operation signal from stage1 phase C or CA

NO.	Signal	Description
9	59P1_Alm	Alarm signal from stage1
10	59P2_Str	Common start signal from stage2
11	59P2_Str1	Start signal from stage2 phase A or AB
12	59P2_Str2	Start signal from stage2 phase B or BC
13	59P2_Str3	Start signal from stage2 phase C or CA
14	59P2_Op	Operation signal from stage2
15	59P2_Op1	Operation signal from stage2 phase A or AB
16	59P2_Op2	Operation signal from stage2 phase B or BC
17	59P2_Op3	Operation signal from stage2 phase C or CA
18	59P2_Alm	Alarm signal from stage2

3.24.2 Protection Principle

3.24.2.1 Operation Mode

The Pickup mode parameter defines whether the protection stage picks up if all 3 measuring elements detect the overvoltage condition (3 out of 3) or if only 1 measuring element detects the overvoltage condition (1 out of 3). When 59P_SP/TP is set to “1”, “1-out-of-3” logic is selected as operation criterion, and when set as “0”, “3-out-of-3” logic is selected.

All stages can be selected for alarm purpose if the setting 59Px_Alm is set to 1. in the alarm mode, no operation signals will be released by 59P.

3.24.2.2 Overvoltage Element

Users can select phase voltage or phase-to-phase voltage for the protection calculation. If setting 59P_Up/Upp is set to “1”, phase-to-phase voltage criterion is selected, else phase voltage criterion is selected.

When phase voltage or phase-to-phase voltage is greater than any enabled stage voltage setting, the stage protection picks up and operates after the time delay, which will drop off instantaneously when fault voltage disappears.

Phase voltage criterion for each stage is:

$$U_{\emptyset} > 59\text{Px\_Vol\_Op}$$

or

$$(U_a > 59\text{Px\_Vol\_Op})\ \&\ (U_b > 59\text{Px\_Vol\_Op})\ \&\ (U_c > 59\text{Px\_Vol\_Op})$$

Where:

$U_{\emptyset}$ is the measured phase voltage.

59Px_Vol_Op is the voltage setting of stage x (x=1, 2) of overvoltage protection.

Phase-to-phase voltage criterion for each stage is:

$$U_{\emptyset\emptyset} > 59\text{Px\_Vol\_Op}$$

or

$$(U_{ab} > 59\text{Px\_Vol\_Op}) \,\&\, (U_{bc} > 59\text{Px\_Vol\_Op}) \,\&\, (U_{ca} > 59\text{Px\_Vol\_Op})$$

Where:

$U_{\emptyset\emptyset}$ is the measured phase-to-phase voltage.

59Px_Vol_Op is the voltage setting of stage x (x=1, 2) of overvoltage protection.

3.24.2.3 Definite-Time Delay

59P has a settable definite time delay for each stage. If the comparing voltage remains above the set value for a time period corresponding to the stage's set time delay and no other blocking signals received, the operation signal of that stage is issued.

The definite time delay can be changed via the setting 59Px_Op_T.

3.24.2.4 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

The user can select the operating characteristic from various inverse-time characteristic curves by setting 59Px_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 59Px_T_Min, then the operating time of the protection changes to the value of setting 59Px_T_Min automatically.

3.24.2.5 Enable and Blocking of the Function

It is possible to block two stages of overvoltage protection 59P by input signals:

59P1_Blk: blocks all start and trip outputs related to stage 1

59P2_Blk: blocks all start and trip outputs related to stage 2

Notice that 59P will not start if the fault detector (FD) is not pickup.

3.24.3 Logic

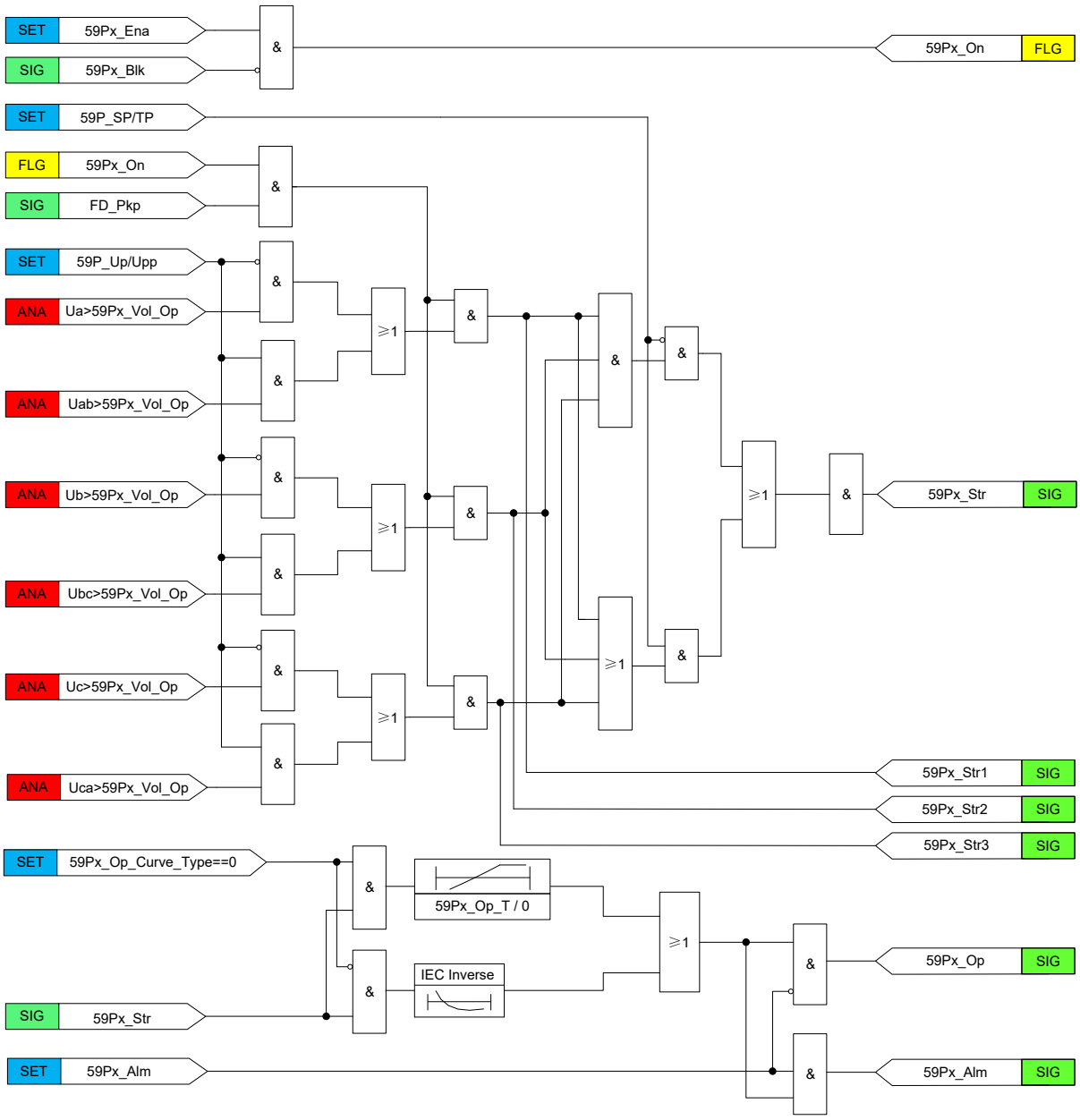


Figure 3.24.1 Logic Diagram of 59P

3.24.4 Settings

Table 3.24-3 59P Settings

NO	Name	Range	Unit	Step	Default	Description
1	59P_Up/Upp	0 or 1	-	1	0	Option of phase-to-phase voltage or phase voltage 0: phase voltage 1: phase-to-phase voltage

NO	Name	Range	Unit	Step	Default	Description
2	59P_SP/TP	0 or 1	-	1	0	Option of 1-out-of-3 mode or 3-out-of-3 mode 0: 3-out-of-3 mode 1: 1-out-of-3 mode
3	59Px_Ena	0 or 1	-	1	0	Enabling/disabling stage x of overvoltage protection (x=1, 2) 0: disable 1: enable
4	59Px_Alm	0 or 1	-	1	0	Enabling/disabling stage x of overvoltage protection for alarm purpose (x=1, 2) 0: disable 1: enable
5	59Px_Vol_Op	30.00~200.00	V	0.01	70	Voltage setting for stage x of overvoltage protection (x=1, 2)
6	59Px_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of overvoltage protection (x=1, 2)
7	59Px_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time overvoltage protection (x=1, 2)
8	59Px_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time overvoltage protection (x=1, 2)
9	59Px_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic overvoltage protection (x=1, 2)
10	59Px_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic overvoltage protection (x=1, 2)
11	59Px_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic overvoltage protection (x=1, 2)
12	59Px_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

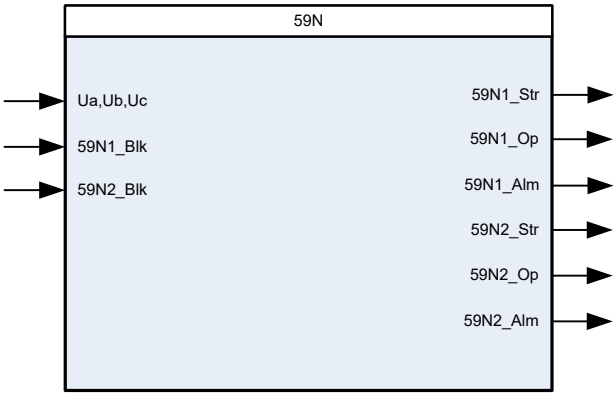
3.25 Residual Overvoltage Protection 59N

3.25.1 Overview

The Overvoltage protection with residual voltage 59N can detects ground faults in isolated or arc-suppression-coil-grounded systems. 59N protection has the following characteristics:

- Both of the two stages in 59N have independent logic, voltage threshold, and settable time delays.
- All stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.

3.25.1.1 Function Block



3.25.1.2 Signals

Table 3.25-1 59N Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	59N1_Blk	Block signal of 59N stage1
3	59N2_Blk	Block signal of 59N stage2

Table 3.25-2 59N Output Signals

NO.	Signal	Description
1	59N1_Str	Common start signal from stage1
2	59N1_Op	Operation signal from stage1
3	59N1_Alm	Alarm signal from stage1
4	59N2_Str	Common start signal from stage2
5	59N2_Op	Operation signal from stage2
6	59N2_Alm	Alarm signal from stage2

3.25.2 Protection Principle

3.25.2.1 Operation Mode

All stages can be selected for alarm purpose if the setting 59Nx_Alm is set to 1. In the alarm mode, no operation signals will be released by 59N.

3.25.2.2 Overvoltage Element

When residual voltage is greater than any enabled stage voltage setting, the stage protection picks up and operates after the time delay, which will drop off instantaneously when fault voltage disappears.

Residual voltage criterion for each stage is:

$$3U_0 > 59\text{Nx\_ResVol\_Op}$$

Where:

$3U_0$ is the calculated residual voltage.

59Nx_ResVol_Op is the voltage setting of stage x (x=1, 2) of residual overvoltage protection.

3.25.2.3 Definite-Time Delay

59N has a settable definite time delay for each stage. If the comparing residual voltage remains above the set value for a time period corresponding to the stage's set time delay and no other blocking signals received, the operation signal of that stage is issued.

The definite time delay can be changed via the setting 59Nx_Op_T.

3.25.2.4 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

The user can select the operating characteristic from various inverse-time characteristic curves by setting 59Nx_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 59Nx_T_Min, then the operating time of the protection changes to the value of setting 59Nx_T_Min automatically.

3.25.2.5 Enable and Blocking of the Function

It is possible to block two stages of residual overvoltage protection 59N by input signals:

59N1_Blk: blocks all start and trip outputs related to stage 1.

59N2_Blk: blocks all start and trip outputs related to stage 2.

Notice that 59N will not start if the fault detector (FD) is not pickup.

3.25.3 Logic

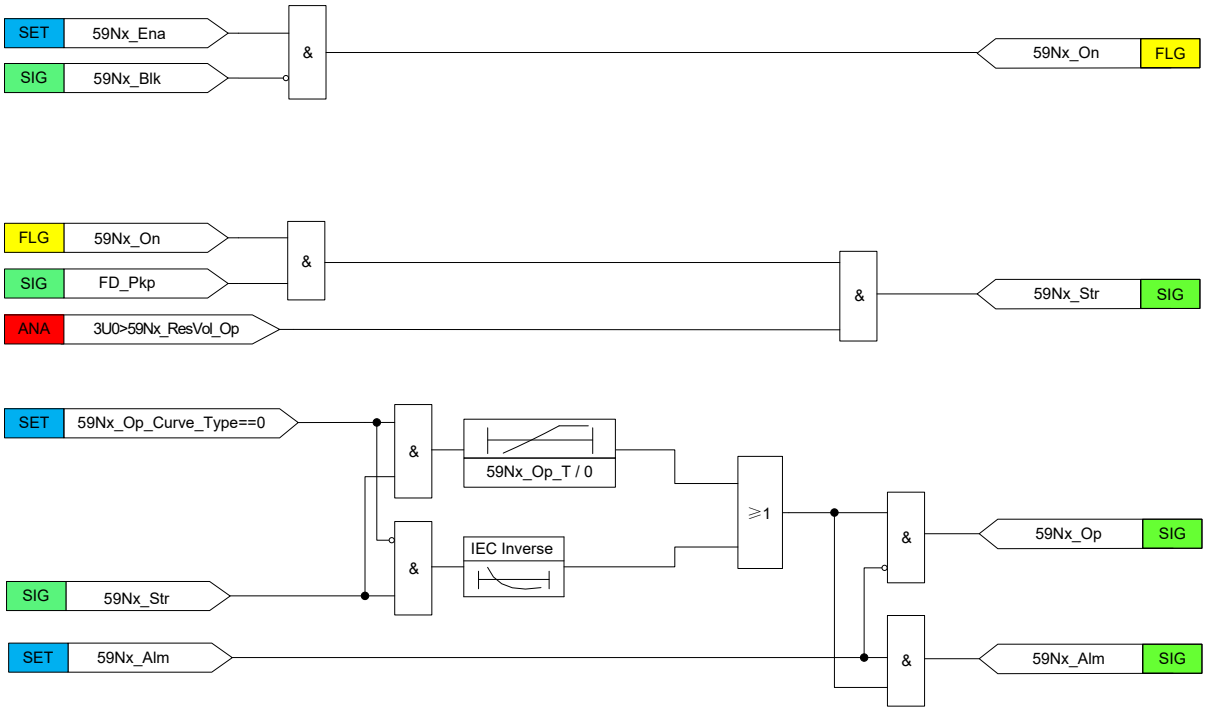


Figure 3.25.1 Logic Diagram of 59N

3.25.4 Settings

Table 3.25-3 59N Settings

NO	Name	Range	Unit	Stage	Default	Description
1	59Nx_Ena	0 or 1	-	1	0	Enabling/disabling stage x of residual overvoltage protection (x=1, 2) 0: disable 1: enable
2	59Nx_Alm	0 or 1	-	1	0	Enabling/disabling stage x of residual overvoltage protection for alarm purpose (x=1, 2) 0: disable 1: enable
3	59Nx_ResVol_Op	0.00~120.00	V	0.01	70	Voltage setting for stage x of residual overvoltage protection (x=1, 2)

NO	Name	Range	Unit	Stage	Default	Description
4	59Nx_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of residual overvoltage protection (x=1, 2)
5	59Nx_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time residual overvoltage protection (x=1, 2)
6	59Nx_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time residual overvoltage protection (x=1, 2)
7	59Nx_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic residual overvoltage protection (x=1, 2)
8	59Nx_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic residual overvoltage protection (x=1, 2)
9	59Nx_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic residual overvoltage protection (x=1, 2)
10	59Nx_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.26 Three Phase Undervoltage Protection 27P

3.26.1 Overview

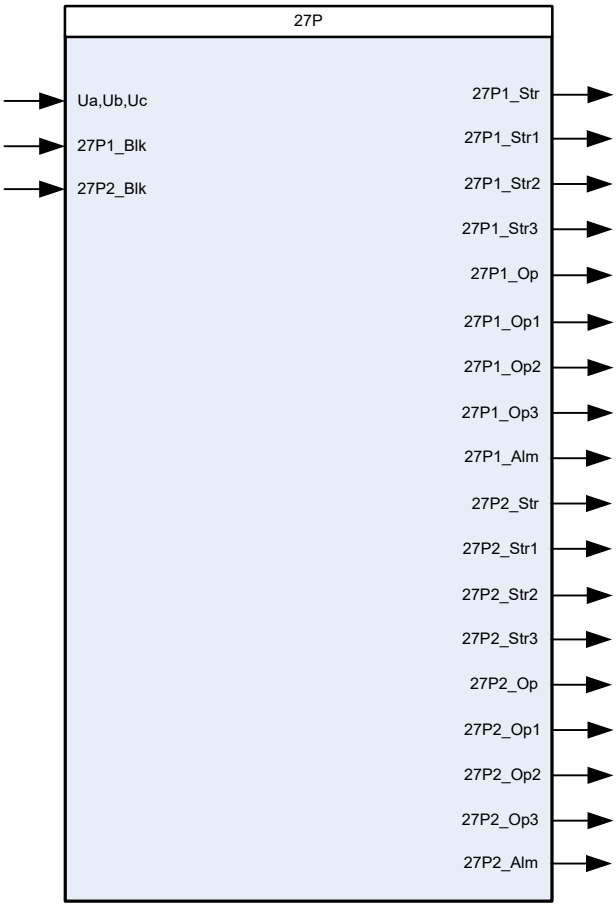
Low voltage may occur when faults or anomalies occur in the power system. Undervoltage protection 27P can be used to trip circuit breaker for system recovery or backup protection in addition to the main protection. 27P protection has the following characteristics:

- Both of the two stages in 27P have independent logic, voltage threshold, and settable time

delays.

- All stages can be set to operating with definite-time or inverse-time delay. The inverse-time characteristic can be chosen from four IEC standard inverse-time characteristics and a user-defined inverse-time curve.
- “1 out of 3” or “3 out of 3” operating mode can be selected via the setting.
- Both phase-to-ground and phase-to-phase voltage can be used in the undervoltage relay.

3.26.1.1 Function Block



3.26.1.2 Signals

Table 3.26-1 27P Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	27P1_Blk	Block signal of 27P stage1
4	27P2_Blk	Block signal of 27P stage2

Table 3.26-2 27P Output Signals

NO.	Signal	Description
1	27P1_Str	Common start signal from stage1
2	27P1_Str1	Start signal from stage1 phase A or AB
3	27P1_Str2	Start signal from stage1 phase B or BC
4	27P1_Str3	Start signal from stage1 phase C or CA
5	27P1_Op	Operation signal from stage1
6	27P1_Op1	Operation signal from stage1 phase A or AB
7	27P1_Op2	Operation signal from stage1 phase B or BC
8	27P1_Op3	Operation signal from stage1 phase C or CA
9	27P1_Alm	Alarm signal from stage1
10	27P2_Str	Common start signal from stage2
11	27P2_Str1	Start signal from stage2 phase A or AB
12	27P2_Str2	Start signal from stage2 phase B or BC
13	27P2_Str3	Start signal from stage2 phase C or CA
14	27P2_Op	Operation signal from stage2
15	27P2_Op1	Operation signal from stage2 phase A or AB
16	27P2_Op2	Operation signal from stage2 phase B or BC
17	27P2_Op3	Operation signal from stage2 phase C or CA
18	27P2_Alm	Alarm signal from stage2

3.26.2 Protection Principle

3.26.2.1 Operation Mode

“1-out-of-3” or “3-out-of-3” logic can be selected for protection criterion. If the setting 27P_SP/TP is set to “1”, every stage of function 27P will start if any of the three phase-to-ground or phase-to-phase criterions are met, and when set to “0”, every stage of function 27P will start if all of the three phase-to-ground or phase-to-phase criterions are met.

All stages can be selected for alarm purpose. If the setting 27Px_Alm is set to 1, stage x of function 27P will only give out an alarm signal instead of operation signal when the time delay expires after the start.

3.26.2.2 Undervoltage Element

User can select phase voltage or phase-to-phase voltage for the protection calculation. If setting 27P_Up/Upp is set to “1”, phase-to-phase voltage criterion is selected, else phase voltage criterion is selected.

When phase voltage or phase-to-phase voltage is less than any enabled stage voltage setting, the stage protection picks up and operates after time delay, which will drop off instantaneously when fault voltage disappears.

Phase voltage criterion for each stage is:

$$U_{\emptyset} < 27\text{Px\_Vol\_Op}$$

or

$$(U_a < 27\text{Px\_Vol\_Op}) \,\&\, (U_b < 27\text{Px\_Vol\_Op}) \,\&\, (U_c < 27\text{Px\_Vol\_Op})$$

Where:

$U_{\emptyset}$ is the measured phase voltage.

27Px_Vol_Op is the voltage setting of stage x (x=1, 2) of undervoltage protection.

Phase-to-phase voltage criterion for each stage is:

$$U_{\emptyset\emptyset} < 27\text{Px\_Vol\_Op}$$

or

$$(U_{ab} < 27\text{Px\_Vol\_Op}) \,\&\, (U_{bc} < 27\text{Px\_Vol\_Op}) \,\&\, (U_{ca} < 27\text{Px\_Vol\_Op})$$

Where:

$U_{\emptyset\emptyset}$ is the measured phase-to-phase voltage.

27Px_Vol_Op is the voltage setting of stage x (x=1, 2) of undervoltage protection.

3.26.2.3 Definite-Time Delay

27P has a settable definite time delay for each stage. If the comparing voltage remains under the set value for a time period corresponding to the set time delay, the operation signal of that stage is issued.

The definite time delay can be change via the setting 27Px_Op_T.

3.26.2.4 Inverse-Time Delay Characteristic

All stages can be selected as definite-time or inverse-time characteristic.

The timer model is determined by **IDMT curves for over quantity protection and under quantity protection**

The user can select the operating characteristic from various inverse-time characteristic curves by setting 27Px_Op_Curve_Type, and parameters of available characteristics for selection are listed in the **table 3.35-1**.

When inverse-time characteristic is selected, if calculated operating time is less than setting 27Px_T_Min, then the operating time of the protection changes to the value of setting 27Px_T_Min automatically.

3.26.2.5 Enable and Blocking of the Function

27P will be blocked when voltage abnormal condition occurs in the initialization of the device when powered on. For example, if a phase current is greater than 0.05In or circuit breaker in that phase is in closed position, undervoltage protection will be in service with a time delay of 100ms as long

as the phase voltage is greater than 0.1Un. Otherwise a signal 27P_U_abnormal will give out by the function and all stages of 27P are blocked. The signal 27P_U_abnormal will not return once pickup.

In order to prevent undervoltage protection from undesired operation, after the device powered on, 27P can also be blocked by VT circuit failure, current flow criteria and certain FD(for example superimposed current element and residual current element) pickup via the following settings:

- If the setting 27Px_VTS_Blk is set to “1”, undervoltage protection will be blocked if VT circuit fails.
- If the setting 27Px_NoCur_Blk is set to “1”, undervoltage protection will be blocked if current condition (>0.05In) is not met.
- If the setting 27Px_FD_Blk is set to “1”, undervoltage protection will be blocked if FD element reflecting current does not operate.

If any phase of circuit breaker is open (binary input of normal close contact of breaker is energized) and the corresponding phase current is smaller than 0.06In, undervoltage protection will be blocked.

It is possible to block Two stage undervoltage protection 27P completely via input signals where:

27P1_Blk: blocks all start and trip outputs related to stage 1.

27P2_Blk: blocks all start and trip outputs related to stage 2.

3.26.3 Logic

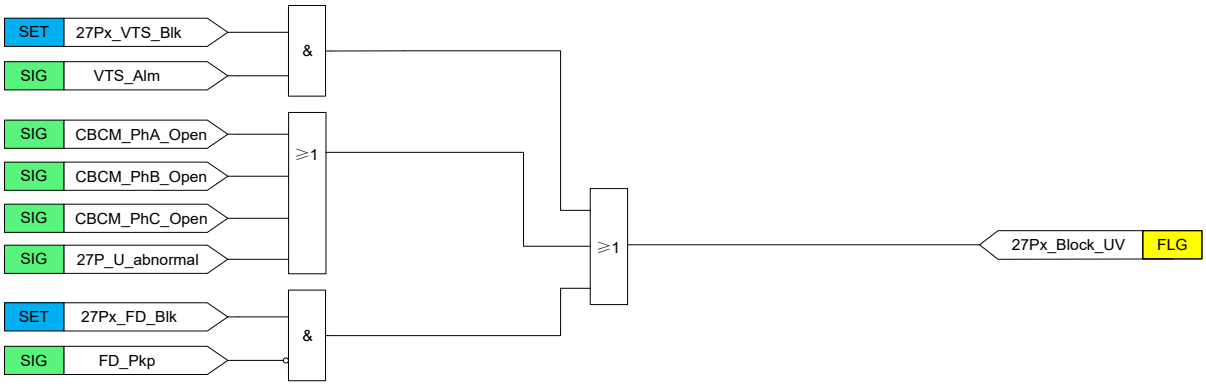


Figure 3.26.1 Logic diagram of Block 27P

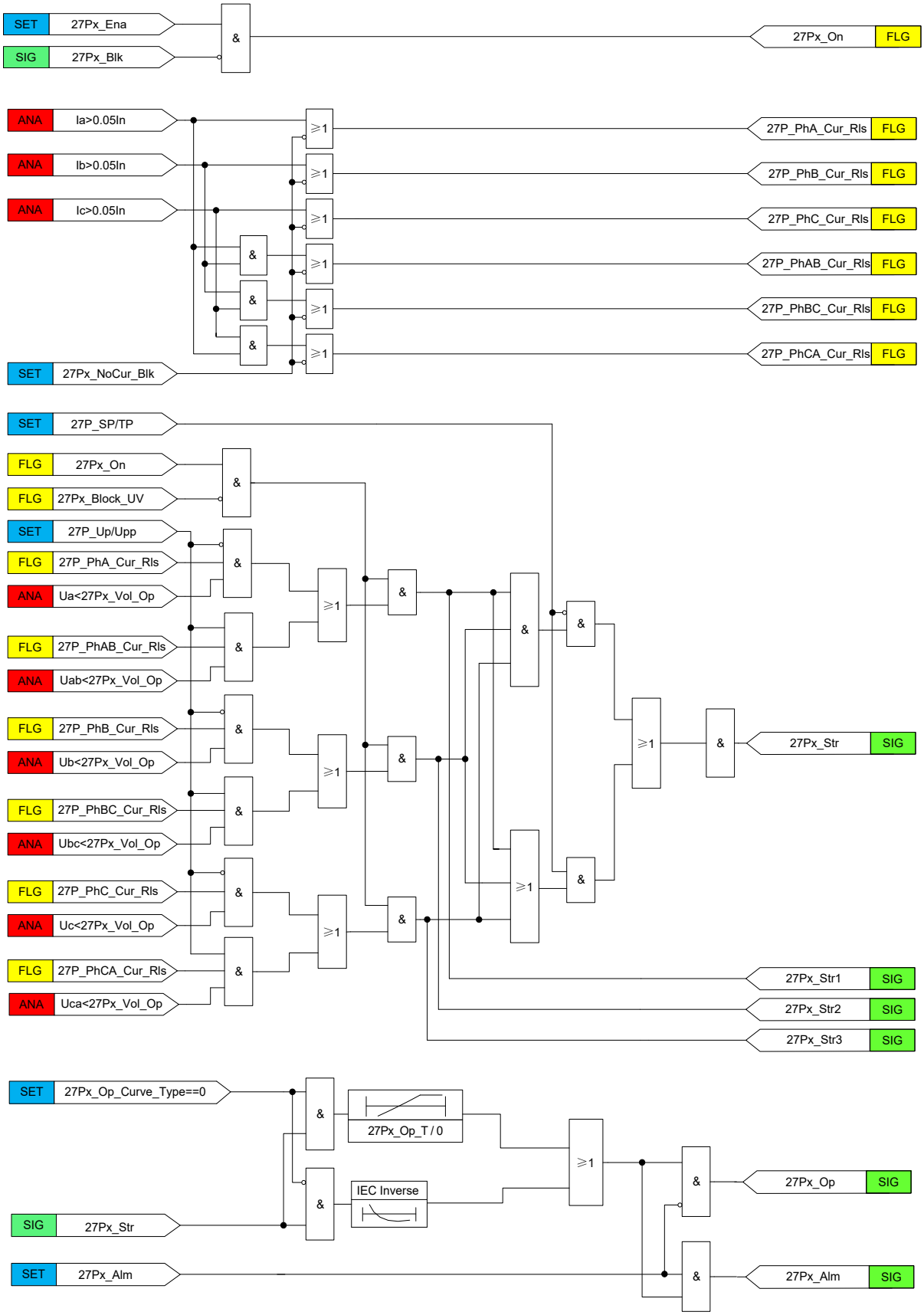


Figure 3.26.2 Logic diagram of 27P

3.26.4 Settings

Table 3.26-3 27P Settings

NO	Name	Range	Unit	Step	Default	Description
1	27P_Up/Upp	0 or 1	-	1	0	Option of phase-to-phase voltage or phase voltage 0: phase voltage 1: phase-to-phase voltage
2	27P_SP/TP	0 or 1	-	1	0	Option of 1-out-of-3 mode or 3-out-of-3 mode 0: 3-out-of-3 mode 1: 1-out-of-3 mode
3	27Px_Ena	0 or 1	-	1	0	Enabling/disabling stage x of undervoltage protection (x=1, 2) 0: disable 1: enable
4	27Px_Alm	0 or 1	-	1	0	Enabling/disabling stage x of undervoltage protection for alarm purpose (x=1, 2) 0: disable 1: enable
5	27Px_VTS_Blk	0 or 1	-	1	0	Enabling/disabling stage x of undervoltage protection controlled by VT circuit failure (x=1, 2) 0: disable 1: enable
6	27Px_NoCur_Blk	0 or 1	-	1	0	Enabling/disabling stage x of undervoltage protection controlled by current condition (x=1, 2) 0: disable 1: enable
7	27Px_FD_Blk	0 or 1	-	1	0	Enabling/disabling stage x of undervoltage protection controlled by FD element reflecting current (x=1, 2) 0: disable 1: enable
8	27Px_Vol_Op	0.00~120.00	V	0.01	50	Voltage setting for stage x of undervoltage protection (x=1, 2)

NO	Name	Range	Unit	Step	Default	Description
9	27Px_Op_T	0.000~100.000	s	0.001	10	Definite Time delay for stage x of undervoltage protection (x=1, 2)
10	27Px_T_Mult	0.010~200.000	-	0.001	10	Time multiplier setting for stage x of inverse-time undervoltage protection (x=1, 2)
11	27Px_T_Min	0.000~60.000	s	0.001	10	Minimum operating time for stage x of inverse-time undervoltage protection (x=1, 2)
12	27Px_Curve_Alpha	0.010~5.000	-	0.001	1	α for stage x of customized inverse-time characteristic undervoltage protection (x=1, 2)
13	27Px_Curve_C	0.000~20.000	-	0.001	0	C for stage x of customized inverse-time characteristic undervoltage protection (x=1, 2)
14	27Px_Curve_K	0.005~200.000	-	0.001	13.5	K for stage x of customized inverse-time characteristic undervoltage protection (x=1, 2)
15	27Px_Op_Curve_Type	1~17	-	1	0	The operation curve type setting (x=1, 2): including Definite time, ANSI and IEC typical curve and user programmable curve. The detail is defined in **Table 3.35- 1 Inverse-time curve parameters**

3.27 Overfrequency Protection 81O

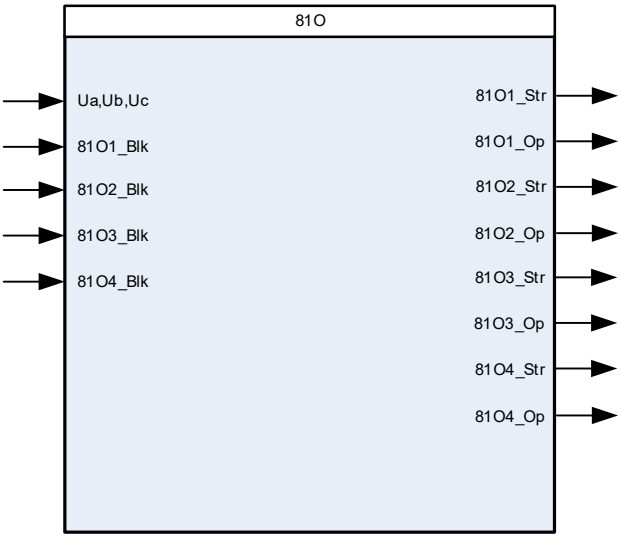
3.27.1 Overview

Unbalanced active power between power plant and the load may cause frequency deviation. Overfrequency may be caused by load shedding, power system disconnection or shunt faults in the power network. Overfrequency implies a risk of self-excitation of machines which are connected to long lines without load. Overfrequency protection 81O can provide a reliable detection of over frequencies and disconnect generating units when the frequency is critical. 81O function has the following characteristics:

- Each of the four stages in 81O has independent logic, frequency threshold, and settable time delays.

- All four stages can be blocked if the VT circuit fails.
- 81O will not operate if the frequency is abnormal or the phase to phase voltage is low.

3.27.1.1 Function Block



3.27.1.2 Signals

Table 3.27-1 81O Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	81O1_Blk	Block signal of 81O stage1
3	81O2_Blk	Block signal of 81O stage2
4	81O3_Blk	Block signal of 81O stage3
5	81O4_Blk	Block signal of 81O stage4

Table 3.27-2 81O Output Signals

NO.	Signal	Description
1	81O1_Str	Common start signal from stage1
2	81O1_Op	Operation signal from stage1
3	81O2_Str	Common start signal from stage2
4	81O2_Op	Operation signal from stage2
5	81O3_Str	Common start signal from stage3
6	81O3_Op	Operation signal from stage3
7	81O4_Str	Common start signal from stage4
8	81O4_Op	Operation signal from stage4

3.27.2 Protection Principle

3.27.2.1 Pickup and Overfrequency Element

The fundamental frequency of the positive sequence voltage is measured continuously, and compared with the setting value, 81Ox_Fr_Op. The frequency measurement depends on the voltage, in fact the function measures the time interval *t* between two zero-crossing point of voltage in the same direction and use 1/t as current frequency value. Frequency criterion for each stage of 81O is:

$$f > 81Ox\_Fr\_Op$$

3.27.2.2 Definite-Time Delay

81O has a settable definite time delay. If the frequency remains above the setting value for a time period corresponding to the set time delay, the corresponding operation signal is issued.

The definite time delay can be changed via the setting 81Ox_Op_T.

3.27.2.3 Enable and Blocking of the Function

It is possible to block both the start and operation signals from 81Ox via input blocking signal 81Ox_Blk.

In order to prevent overfrequency protection from undesired operation, the function will be blocked in the following cases too:

- To avoid an unwanted trip due to uncertain frequency measurement if VT circuit failure occurs, all stages of 81O can be blocked if a VTS_Alm signal is received.
- Frequency abnormality condition. When the measuring frequency f is off the limit for example f<(Fn-20) or f>(Fn+20), where Fn=50 or 60Hz, overfrequency protection will be blocked.
- If the phase to phase voltage magnitude is below the setting value 81O_Vol_Blk, overfrequency protection will be blocked.

3.27.3 Logic

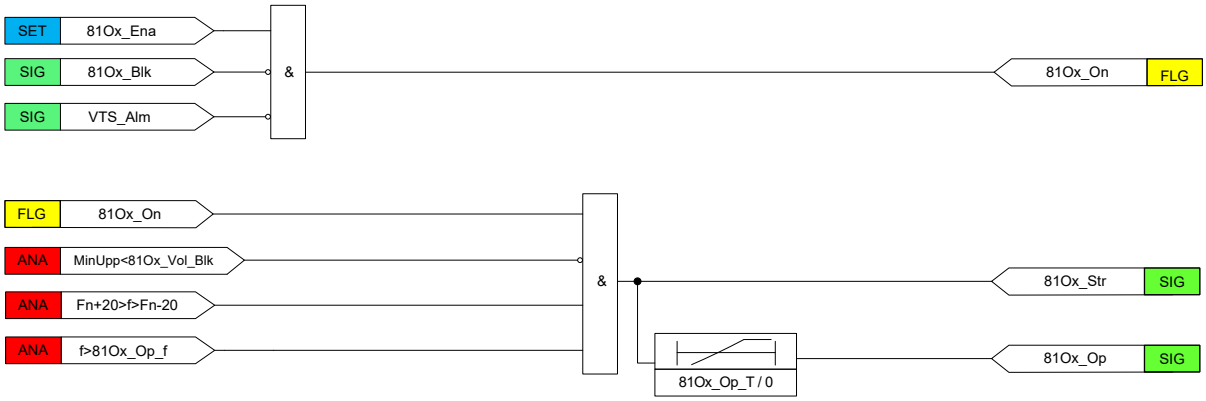


Figure 3.27.1 Logic Diagram of 81O

3.27.4 Settings

Table 3.27-3 81O Settings

NO	Name	Range	Unit	Step	Default	Description
1	81O1_Ena	0 or 1	-	1	0	Enabling/disabling stage 1 of overfrequency protection 0: disable 1: enable
2	81O1_Fr_Op	50.00~70.00(Fn=50) 60.00~80.00(Fn=60)	Hz	0.01	60.1	Frequency setting for stage 1 of overfrequency protection
3	81O1_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 1 of overfrequency protection
4	81O1_Vol_Blk	18.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 1
5	81O2_Ena	0 or 1	-	1	0	Enabling/disabling stage 2 of overfrequency protection 0: disable 1: enable
6	81O2_Fr_Op	50.00~70.00(Fn=50) 60.00~80.00(Fn=60)	Hz	0.01	60.2	Frequency setting for stage 2 of overfrequency protection
7	81O2_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 2 of overfrequency protection
8	81O2_Vol_Blk	18.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 2
9	81O3_Ena	0 or 1	-	1	0	Enabling/disabling stage 3 of overfrequency protection 0: disable 1: enable
10	81O3_Fr_Op	50.00~70.00(Fn=50) 60.00~80.00(Fn=60)	Hz	0.01	60.3	Frequency setting for stage 3 of overfrequency protection
11	81O3_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 3 of overfrequency protection
12	81O3_Vol_Blk	18.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 3
13	81O4_Ena	0 or 1			0	Enabling/disabling stage 4 of overfrequency protection 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
14	81O4_Fr_Op	50.00~70.00(Fn=50) 60.00~80.00(Fn=60)	Hz	0.01	60.4	Frequency setting for stage 4 of overfrequency protection
15	81O4_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 4 of overfrequency protection
16	81O4_Vol_Blk	18.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 4

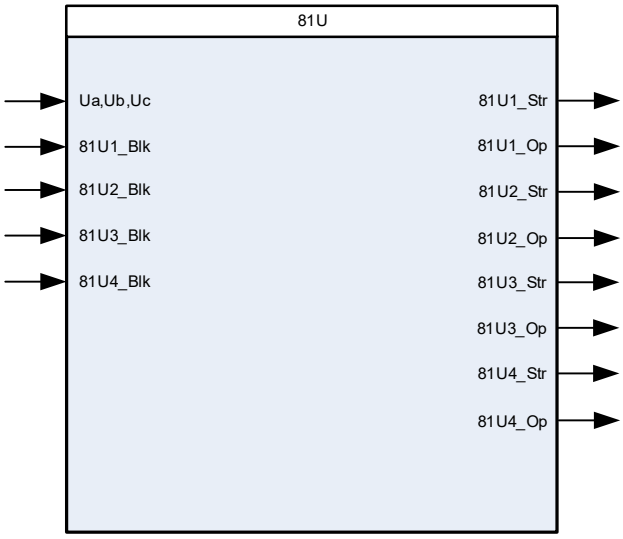
3.28 UnderFrequency Protection 81U

3.28.1 Overview

Underfrequency in power systems is caused by an increase of the active power in the load or by a decrease of the generated active power. Other incidents like power system disconnection, generator failure may also cause underfrequency. Underfrequency protection function 81U can be used to detect underfrequencies in the power system, shed load and decouple power systems. 81U function has the following characteristics:

- Each of the four stages in 81U has independent logic, frequency threshold, and settable time delays.
- All four stages of 81U can be blocked if the VT circuit fails.
- 81U will not operate if the frequency is abnormal.

3.28.1.1 Function Block



3.28.1.2 Signals

Table 3.28-1 81U Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input

NO.	Signal	Description
2	81U1_Blk	Block signal of 81U stage1
3	81U2_Blk	Block signal of 81U stage2
4	81U3_Blk	Block signal of 81U stage3
5	81U4_Blk	Block signal of 81U stage4

Table 3.28-2 81U Output Signals

NO.	Signal	Description
1	81U1_Str	Common start signal from stage1
2	81U1_Op	Operation signal from stage1
3	81U2_Str	Common start signal from stage2
4	81U2_Op	Operation signal from stage2
5	81U3_Str	Common start signal from stage3
6	81U3_Op	Operation signal from stage3
7	81U4_Str	Common start signal from stage4
8	81U4_Op	Operation signal from stage4

3.28.2 Protection Principle

Underfrequency Protection 81U has four stages (stage 1 to stage 4). All stages of 81U consist of independent operation logic, pickup frequency, and time delay settings.

3.28.2.1 Pickup and Underfrequency Element

If the frequency remains below the set value 81Ux_Fr_Op for a time period corresponding to the setting time delay 81Ux_Op_T, the corresponding operation signal is issued. Frequency criterion for each stage is:

$$f < 81Ux\_Fr\_Op$$

It is possible to block overfrequency protection 81U via input signals 81Ux_Blk which blocks the start and operation signals of 81Ux, stage x.

3.28.2.2 Definite-Time Delay

81U has a settable definite time delay. If the frequency remains under the set value for a time period corresponding to the set time delay and no other blocking signals received, the corresponding operation signal is issued.

The definite time delay can be changed via the setting 81Ux_Op_T.

3.28.2.3 Enable and Blocking of the Function

In order to prevent underfrequency protection from undesired operation, underfrequency protection will be blocked in the following cases.

- To avoid an unwanted trip due to uncertain frequency measurement if VT circuit failure occurs, all stages of 81U can be blocked if a VTS_Alm signal is received.

- Frequency abnormality condition. When the measuring frequency f is off the limit for example f<(Fn-20) or f>(Fn+20), where Fn=50 or 60Hz, overfrequency protection will be blocked.
- If the phase to phase voltage magnitude is below the setting value 81U_Vol_Blk, overfrequency protection will be blocked.

3.28.3 Logic

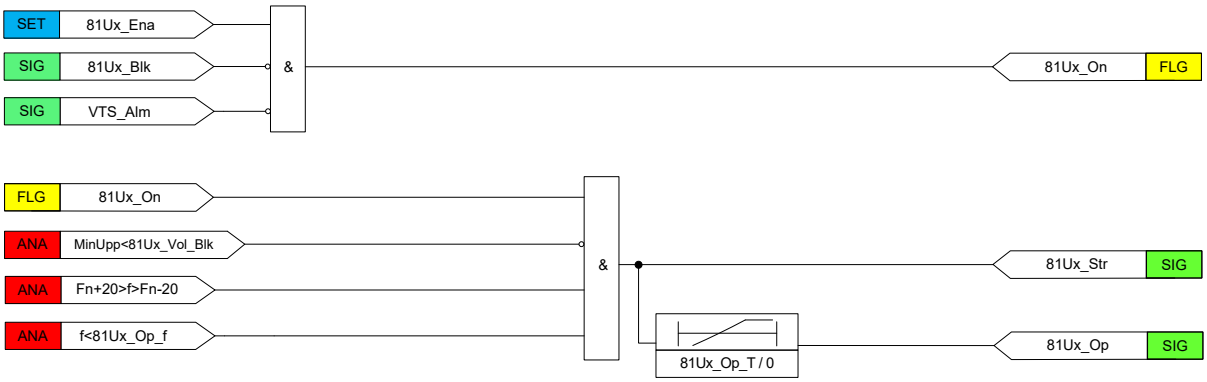


Figure 3.28.1 Logic Diagram of 81U

3.28.4 Settings

Table 3.28-3 81U Settings

NO	Name	Range	Unit	Step	Default	Description
1	81U1_Ena	0 or 1	-	1	0	Enabling/disabling stage 1 of underfrequency protection 0: disable 1: enable
2	81U1_Fr_Op	30.00~50.00(Fn=50) 40.00~60.00(Fn=60)	Hz	0.01	59.9	Frequency setting for stage 1 of underfrequency protection
3	81U1_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 1 of underfrequency protection
4	81U1_Vol_Blk	0.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 1
5	81U2_Ena	0 or 1	-	1	0	Enabling/disabling stage 2 of underfrequency protection 0: disable 1: enable
6	81U2_Fr_Op	30.00~50.00(Fn=50) 40.00~60.00(Fn=60)	Hz	0.01	59.8	Frequency setting for stage 2 of underfrequency protection
7	81U2_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 2 of underfrequency protection

NO	Name	Range	Unit	Step	Default	Description
8	81U2_Vol_Blk	0.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 2
9	81U3_Ena	0 or 1	-	1	0	Enabling/disabling stage 3 of underfrequency protection 0: disable 1: enable
10	81U3_Fr_Op	30.00~50.00(Fn=50) 40.00~60.00(Fn=60)	Hz	0.01	59.7	Frequency setting for stage 3 of underfrequency protection
11	81U3_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 3 of underfrequency protection
12	81U3_Vol_Blk	0.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 3
13	81U4_Ena	0 or 1	-	1	0	Enabling/disabling stage 4 of underfrequency protection 0: disable 1: enable
14	81U4_Fr_Op	30.00~50.00(Fn=50) 40.00~60.00(Fn=60)	Hz	0.01	59.6	Frequency setting for stage 4 of underfrequency protection
15	81U4_Op_T	0.040~200.000	s	0.001	10	Time delay for stage 4 of underfrequency protection
16	81U4_Vol_Blk	0.00~100.00	V	0.01	30	Undervoltage blocking setting value for stage 4

3.29 Frequency Gradient Protection 81R

3.29.1 Overview

This function 81R provides one-stage frequency gradient protection with independent definite time delay characteristic.

81R is applicable in all the situations where the change of the fundamental power system voltage frequency should be detected reliably. 81R can be used for both increasing and decreasing of the frequencies.

This function can provide trip signal suitable for load shedding, generator shedding, generator boosting and gas turbine startup. The frequency gradient is often used in combination with a low frequency signal, especially in smaller power systems where the loss of a fairly large generator requires quick remedial actions to secure the power system's integrity.

The calculation of the frequency and frequency rate are based on the phase to phase voltage sampled values.

3.29.1.1 Function Block

3.29.1.2 Signals

Table 3.29-1 81R Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	81R_Blk	Block signal of 81R

Table 3.29-2 81R Output Signals

NO.	Signal	Description
1	81R_Str	Start signal from 81R
2	81R_Op	Operation signal from 81R

3.29.2 Protection Principle

3.29.2.1 Pickup Element

The changing rate of the frequency of the positive sequence voltage is calculated from phase-to-phase or phase-to-earth voltages and compared with the setting 81R_Dfdt_Str. If the measured frequency changing rate is higher than the setting 81R_Dfdt_Str and no blocking signal is received, the operate timer and 81R_Str signal are activated:

$$df/dt > 81R\_Dfdt\_Str$$

Notice that the function compares the absolute value of the changing rate of frequency with the setting 81R_Dfdt_Str. And when the setting 81R_FrUp_Ena is set to 1, the measured frequency must be above the rated frequency for the function to operate which means it can only detect a positive change in frequency. Similarly, the function can and only detect negetive change in frequency if the setting 81R_FrUp_Ena is set to 0.

3.29.2.2 Definite-Time Delay

81R has a settable definite operation and reset time delay. If the changing rate of frequency remains above the setting value for the setting time delay 81R_Op_T, the operation signal will be issued.

If the frequency gradient condition disappears before the function operates, the operation resets after a setting time delay 81R_Reset_T.

3.29.2.3 Enable and Blocking of the Function

It is possible to block both the start and operation signals from 81R via input blocking signal 81R_Blk.

In order to prevent frequency gradient protection from undesired operation, the function will be blocked in the following cases too:

- To avoid unwanted trip due to uncertain frequency measurement if VT circuit failure occurs, 81R can be blocked if VTS_Alm signal is received.
- Frequency abnormality condition. When the measured frequency f is off the limit for example f<(Fn-20) or f>(Fn+20), where Fn=50 or 60Hz, frequency gradient protection will be blocked.
- If the phase to phase voltage magnitude is below the setting value 81R_Vol_Blk, the function will be blocked.

3.29.3 Logic

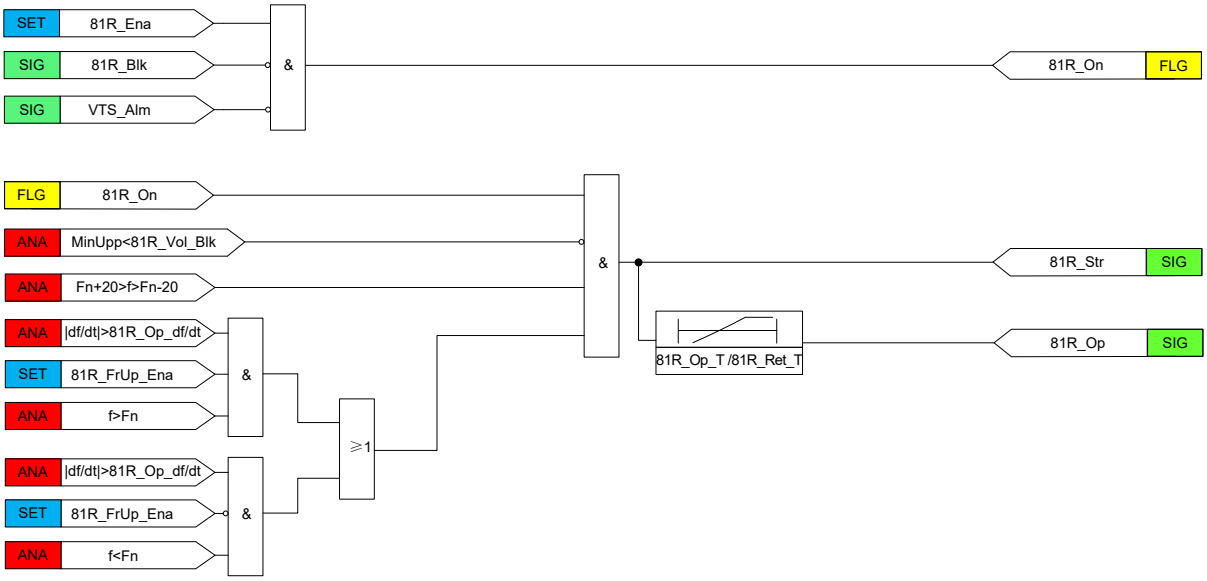


Figure 3.29.1 Logic Diagram of 81

3.29.4 Settings

Table 3.29-3 81R Settings

NO	Name	Range	Unit	Step	Default	Description
1	81R_Ena	0 or 1	-	1	0	Enabling/disabling of frequency gradient protection 0: disable 1: enable
2	81R_FrUp_Ena	0 or 1	-	1	0	Negative/positive change in frequency:

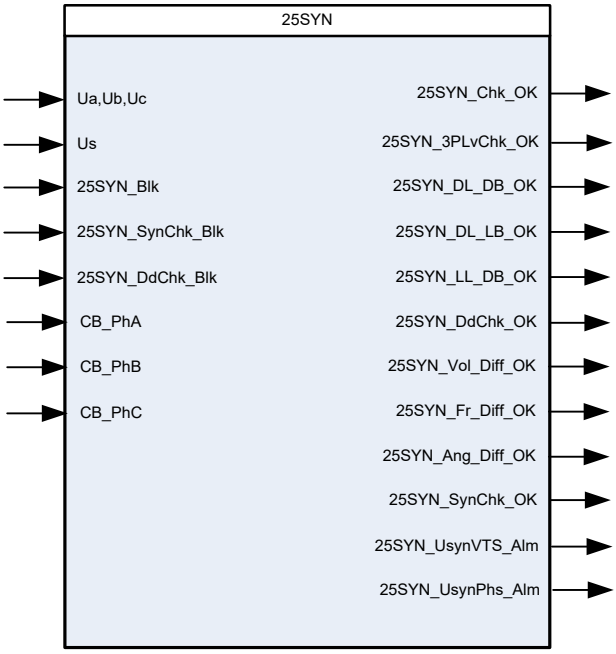
NO	Name	Range	Unit	Step	Default	Description
						0: negative 1: positive
3	81R_Dfdt_Str	0.5~10.00	Hz/s	0.01	0.5	Frequency gradient start value
4	81R_Op_T	0.120~100.000	s	0.001	1	Operate time delay
5	81R_Reset_T	0.000~100.000	s	0.001	0.2	Time delay for reset
6	81R_Vol_Blk	18.00~100.00	V	0.01	30	Block signal of the function

3.30 Synchrocheck 25SYN

3.30.1 Overview

The synchronization checking function 25SYN ensures that the grid can be merged at the right time and improve the stability of the auto-recloser. 25SYN checks whether the activation is permissible without a risk to the stability of the system when interconnecting 2 parts of an electrical power system. Typical applications are the synchronization of a line and a bus bar.

3.30.1.1 Function Block



3.30.1.2 Signals

Table 3.30-1 25SYN Input Signals

NO.	Signal	Description
1	Ua,Ub,Uc	Three-phase voltage input
2	Us	Synchronism voltage input
3	25SYN_Blk	Block signal of synchrocheck function for AR
4	25SYN_SynChk_Blk	Block signal of synchronism check for AR

NO.	Signal	Description
5	25SYN_DdChk_Blk	Block signal of dead charge check for AR
6	CB_PhA	Normally closed contact of A-phase of circuit breaker
7	CB_PhB	Normally closed contact of B-phase of circuit breaker
8	CB_PhC	Normally closed contact of C-phase of circuit breaker

Table 3.30-2 25SYN Output Signals

NO.	Signal	Description
1	25SYN_Chk_OK	Synchronizing OK output
2	25SYN_3PLvChk_OK	Live three-phase check condition of AR is met
3	25SYN_DL_DB_OK	Dead line and dead bus condition is met
4	25SYN_DL_LB_OK	Dead line and live bus condition is met
5	25SYN_LL_DB_OK	Live line and dead bus condition is met
6	25SYN_DdChk_OK	Dead charge check is OK
7	25SYN_Vol_Diff_OK	To indicate that voltage difference condition for synchronism check of AR is met, voltage difference between reference voltage and synchronism voltage is smaller than 25SYN_Vol_Diff.
8	25SYN_Fr_Diff_OK	To indicate that frequency difference condition for synchronism check of AR is met, frequency difference between reference voltage and synchronism voltage is smaller than 25SYN_Fr_Diff.
9	25SYN_Ang_Diff_OK	To indicate that phase angle difference condition for synchronism check of AR is met, phase angle difference between reference voltage and synchronism voltage is smaller than 25SYN_Ang_Diff.
10	25SYN_SynChk_OK	Synchronism is OK
11	25SYN_UsynVTS_Alm	Synchronism circuit failure alarm signal
12	25SYN_UsynPhs_Alm	Synchronism phase error alarm signal

3.30.2 Operation Principle

The synchronism check function is mainly to measure the electrical quantities between both sides of the circuit breaker and compares them with the corresponding settings. The output is only given if all measured quantities are simultaneously within their set limits.

3.30.2.1 Synchronization Voltage Selection

3.30.2.2 Dead Charge Check Logic

The bus/line dead criterion is:

$$U < 25\mathrm{SYN\_Vol\_Dd}$$

Where:

U is the voltage $\dot{U}_{syn}$ or $\dot{U}_{ref}$.

25SYN_Vol_Dd is the setting of Voltage threshold of dead check.

the bus/line live criterion is:

$$U > 25\text{SYN\_Vol\_Lv}$$

Where:

U is the voltage $\dot{U}_{syn}$ or $\dot{U}_{ref}$.

25SYN_Vol_Lv is the setting of voltage threshold of live check.

3.30.2.3 Synchronism Check Logic

The voltage difference criterion is:

$$\left|\dot{U}_{syn} - \dot{U}_{ref}\right| \leq 25\text{SYN\_Vol\_Diff}$$

The phase difference criterion is:

$$\left|arg\frac{\dot{U}_{syn}}{\dot{U}_{ref}}\right| \leq 25\text{SYN\_Ang\_Diff}$$

The frequency difference criterion is:

$$\left|\mathrm{f}(\dot{U}_{syn}) - \mathrm{f}(\dot{U}_{ref})\right| \leq 25\text{SYN\_Fr\_Diff}$$

Where:

25SYN_Vol_Diff is the setting of voltage difference limit.

25SYN_Ang_Diff is the setting of phase difference limit.

25SYN_Fr_Diff is the setting of frequency difference limit.

3.30.3 Logic

The dead charge check conditions have five types:

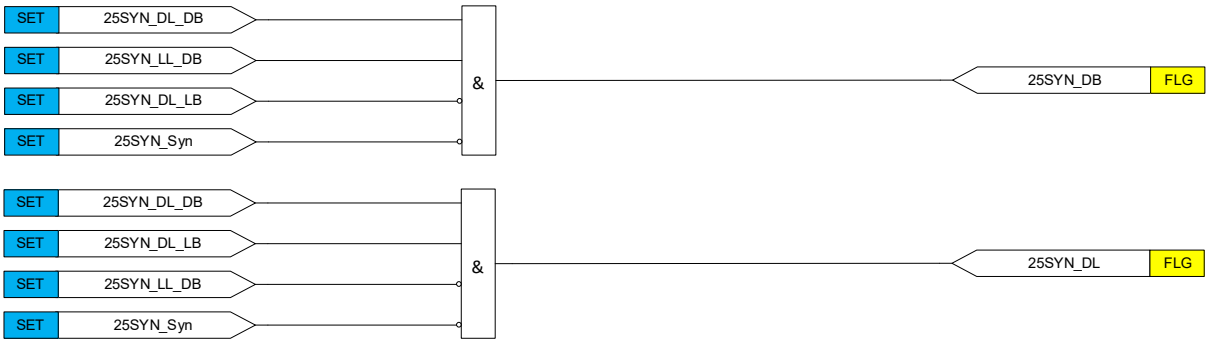
1) When logic setting 25SYN_DL_DB is set as “1”, the dead charge check mode is dead-line and dead-bus check;

2) When logic setting 25SYN_DL_LB is set as “1”, the dead charge check mode is dead-line and live-bus check;

3) When logic setting 25SYN_LL_DB is set as “1”, the dead charge check mode is live-line and dead-bus check;

4) When logic setting 25SYN_DL_DB and 25SYN_LL_DB is set as “1”, 25SYN_DL_LB and 25SYN_Syn is set as “0”, the dead charge check mode is dead-bus check;

5) When logic setting 25SYN_DL_DB and 25SYN_DL_LB is set as “1”, 25SYN_LL_DB and 25SYN_Syn is set as “0”, the dead charge check mode is dead-line check;



The device can calculate the measured bus voltage and line voltage at both sides of the circuit breaker and compare them with the settings. When the voltage is higher than 25SYN_Vol_Lv, the bus/line is regarded as live. When the voltage is lower than 25SYN_Vol_Dd, the bus/line is regarded as dead.

When the logic setting VTS_LineVT is set to “0”, voltage select bus VT for protection calculation, line VT for synchronism voltage. The dead charge check logic is shown in Figure 3.30.1.

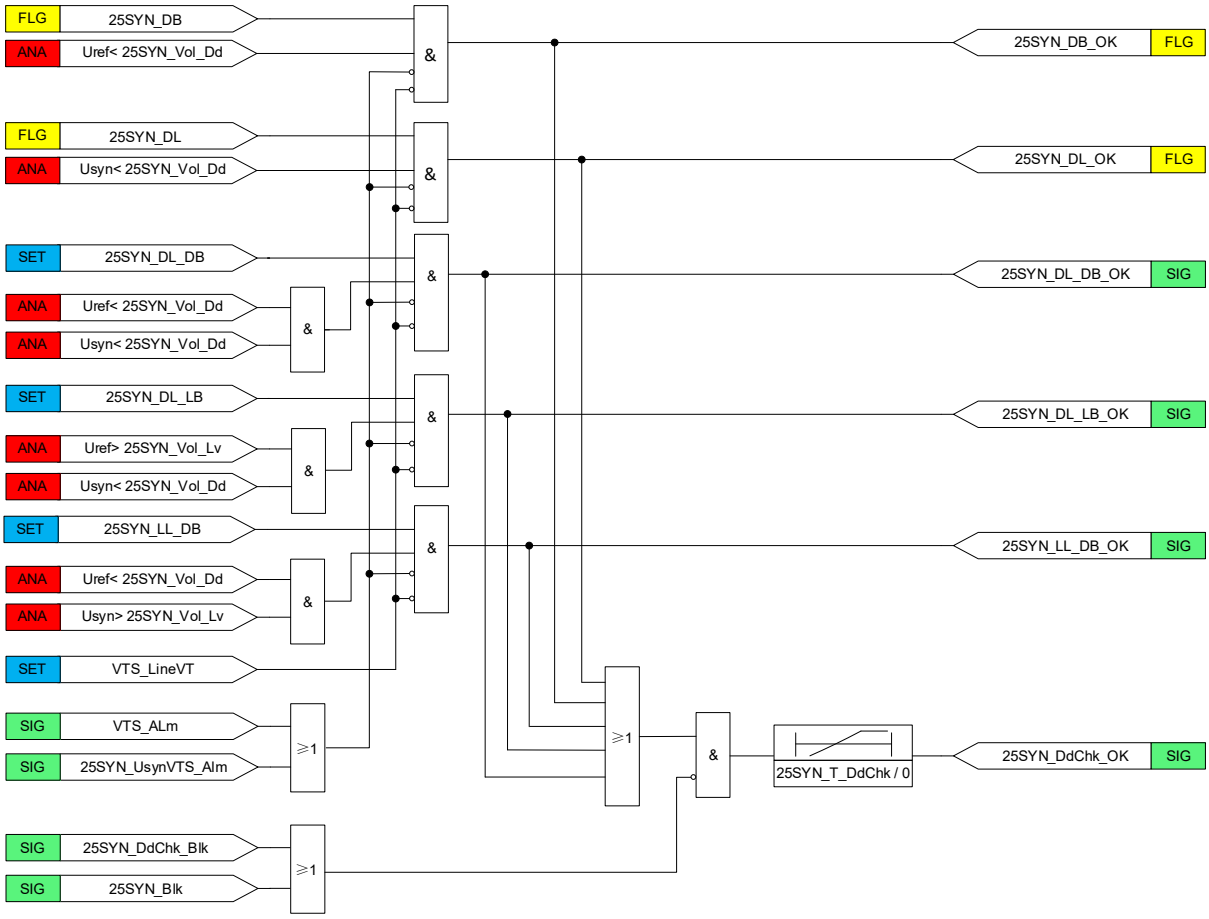


Figure 3.30.1 Logic Diagram of Dead charge check logic（the logic setting VTS_LineVT is set to “0”）

When the logic setting VTS_LineVT is set to “1”, voltage select line VT for protection calculation, bus VT for synchronism voltage. The dead charge check logic is shown in Figure 3.30.2.

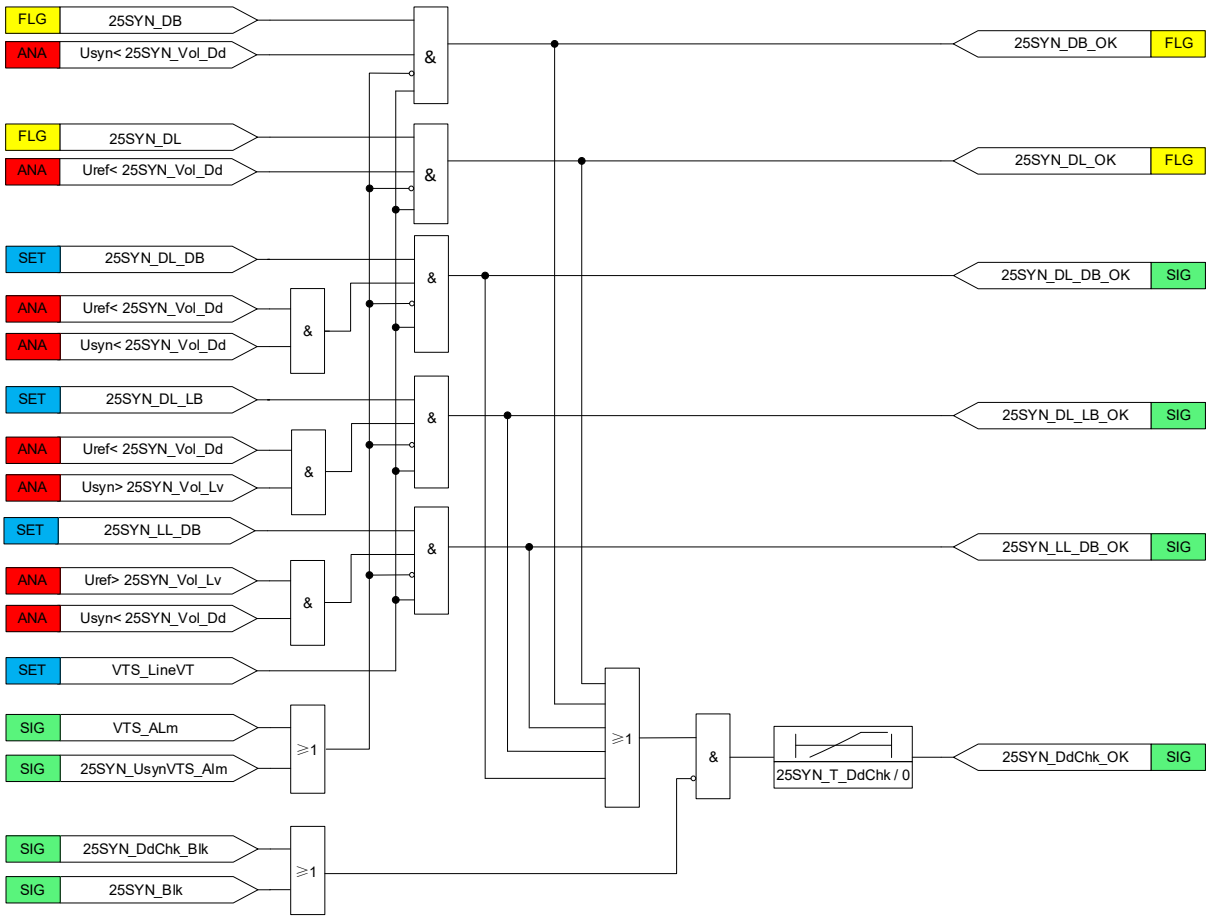
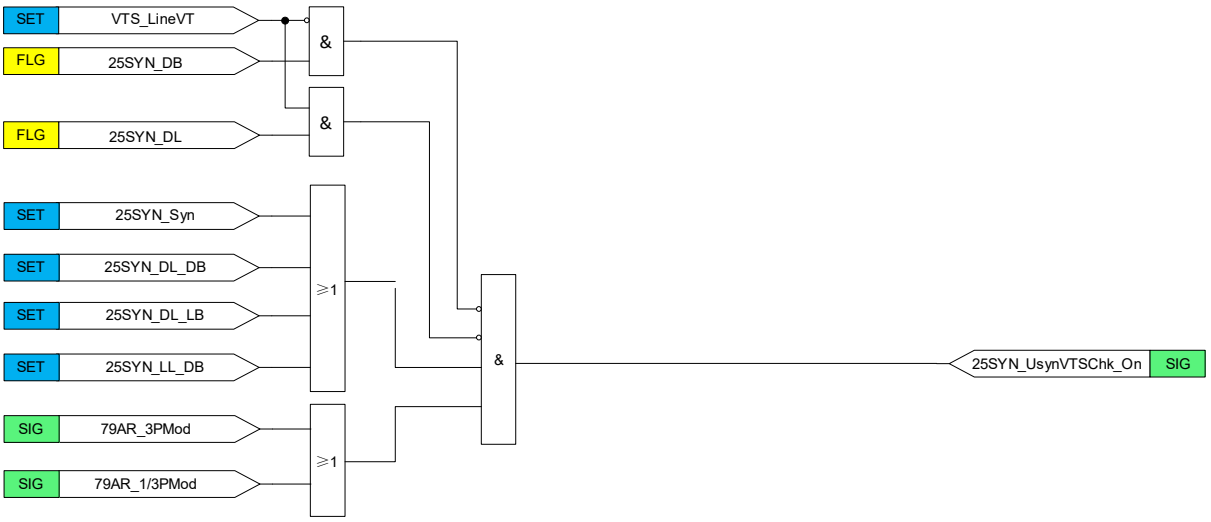


Figure 3.30.2 Logic Diagram of Dead charge check logic (the logic setting VTS_LineVT is set to "1")

If synchronism voltage is used for auto-reclosing with synchronism or dead line or busbar check, the VT circuit of synchronism voltage is monitored.



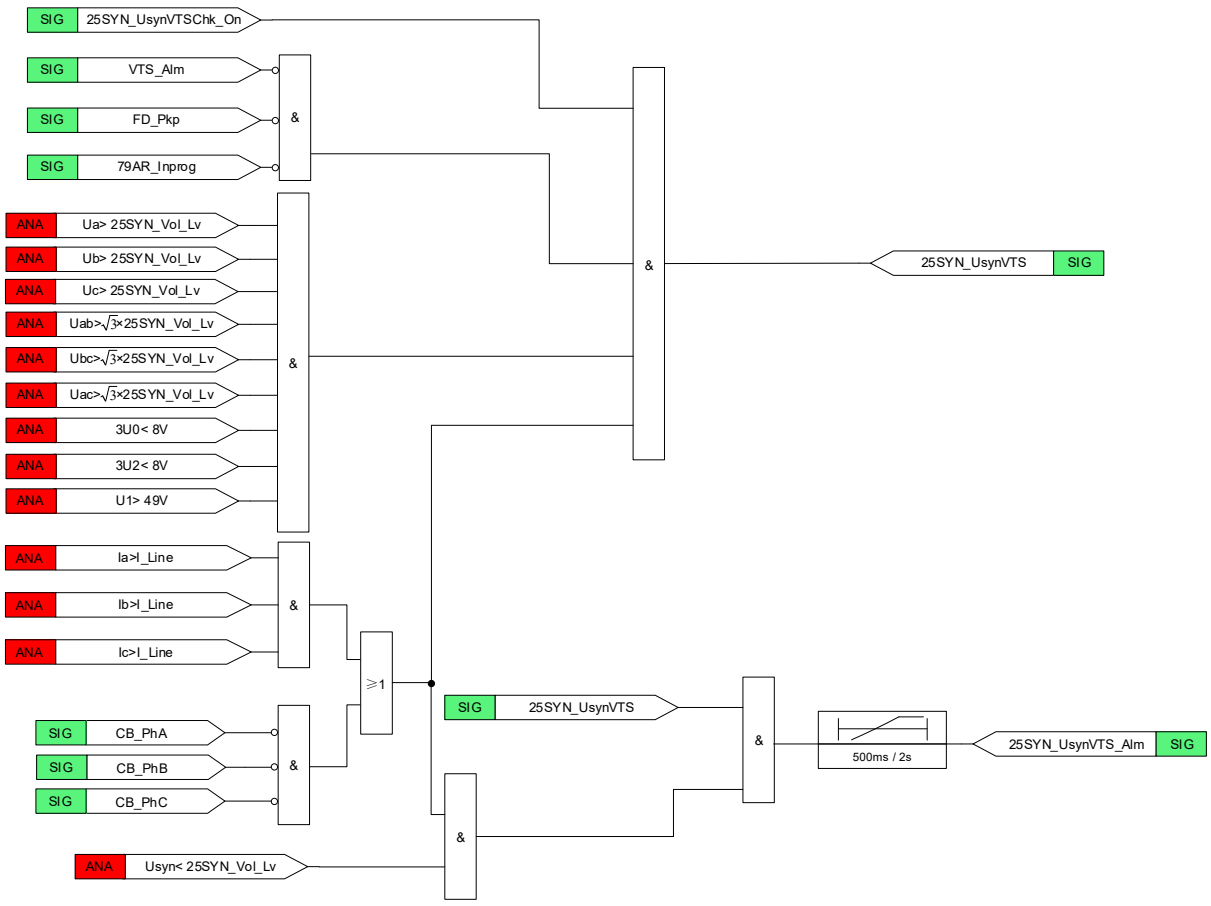


Figure 3.30.3 Logic Diagram of Synchronism voltage circuit failure supervision

The frequency difference, voltage difference, and phase difference of voltages from both sides of the circuit breaker are calculated in the device, they are used as input conditions of the synchronism check. When the synchronism check function is enabled and the voltages of both ends meet the requirements of the voltage difference, phase difference, and frequency difference, and there is no synchronism check blocking signal, and the measured bus voltage and line voltage for synchro-check should not exceed the overvoltage threshold 25SYN_OV or lag the undervoltage threshold 25SYN_UV, it is regarded that the synchronism check conditions are met.

Synchronism check logic is usually used for 3-pole AR, and 1-pole AR usually adopts no check logic. However, the circuit breaker at local end can not reclosed unless the circuit breaker at remote end is reclosed successfully. In order to meet this requirement, live three-phase check can be used for 1-pole AR, determined by the setting 25SYN_3PLvChk, ensure that three-phase voltages is restored to normal at local end after the circuit breaker at remote end is reclosed.

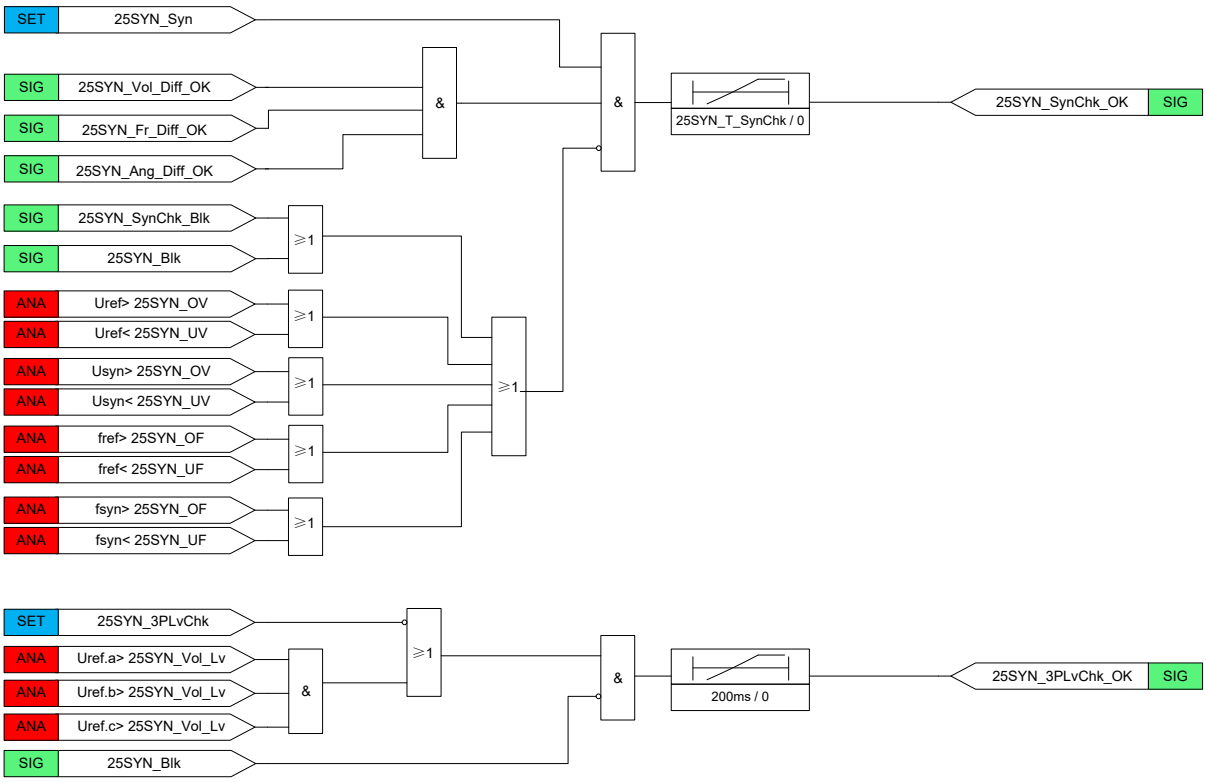


Figure 3.30.4 Logic Diagram of Synchronism check

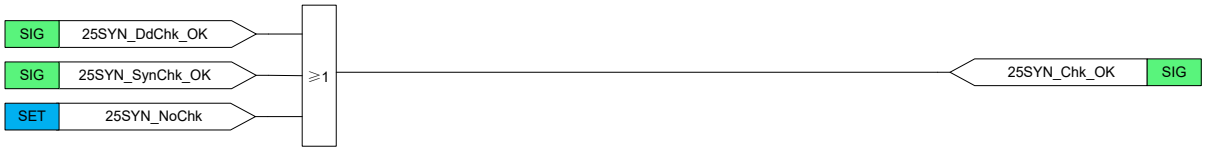


Figure 3.30.5 Logic diagram of Synchronism Output

3.30.4 Settings

Table 3.30-3 25SYN Settings

NO	Name	Range	Unit	Step	Default	Description
1	25SYN_NoChk	0 or 1	-	1	0	Enabling/disabling 79AR without any check 0: disable 1: enable
2	25SYN_DL_DB	0 or 1	-	1	0	Enabling/disabling dead line and dead bus (DLDB) check 0: disable 1: enable
3	25SYN_DL_LB	0 or 1	-	1	0	Enabling/disabling dead line and live bus (DLLB) check 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
4	25SYN_LL_DB	0 or 1	-	1	0	Enabling/disabling live line and dead bus (LLDB) check 0: disable 1: enable
5	25SYN_Syn	0 or 1	-	1	0	Enabling/disabling synchronism check 0: disable 1: enable
6	25SYN_3PLvChk	0 or 1	-	1	0	Enabling/disabling live three-phase check of line 0: disable 1: enable
7	25SYN_OV	55.7~110.00	V	0.01	110	Threshold of over voltage for synchronism blocking
8	25SYN_UV	0.01~66.4	V	0.01	40	Threshold of under voltage for synchronism blocking
9	25SYN_OF	0~65	Hz	0.01	65	Threshold of over frequency for synchronism blocking
10	25SYN_UF	0~65	Hz	0.01	45	Threshold of under frequency for synchronism blocking
11	25SYN_Vol_Dd	0.01~110.00	V	0.01	30	Voltage threshold of dead check
12	25SYN_Vol_Lv	0.01~110.00	V	0.01	40	Voltage threshold of live check
13	25SYN_Ang_Diff	0~ 89	deg	0.01	30	Phase difference limit of synchronism check for 79AR
14	25SYN_Vol_Diff	0.01~110.00	V	0.01	10	Voltage difference limit of synchronism check for 79AR
15	25SYN_Fr_Diff	0.00~5.00	Hz	0.01	0.5	Frequency difference limit of synchronism check for 79AR
16	25SYN_T_DdChk	0.010~20.000	s	0.001	1	Time delay to confirm dead check condition
17	25SYN_T_SynChk	0.010~20.000	s	0.001	1	Time delay to confirm synchronism check condition
18	25SYN_SynPhs	0~5		1	0	0:Ua: A-phase voltage 1:Ub: B-phase voltage 2:Uc: C-phase voltage 3:Uab: AB-phase voltage 4:Ubc: BC-phase voltage 5:Uca: CA-phase voltage

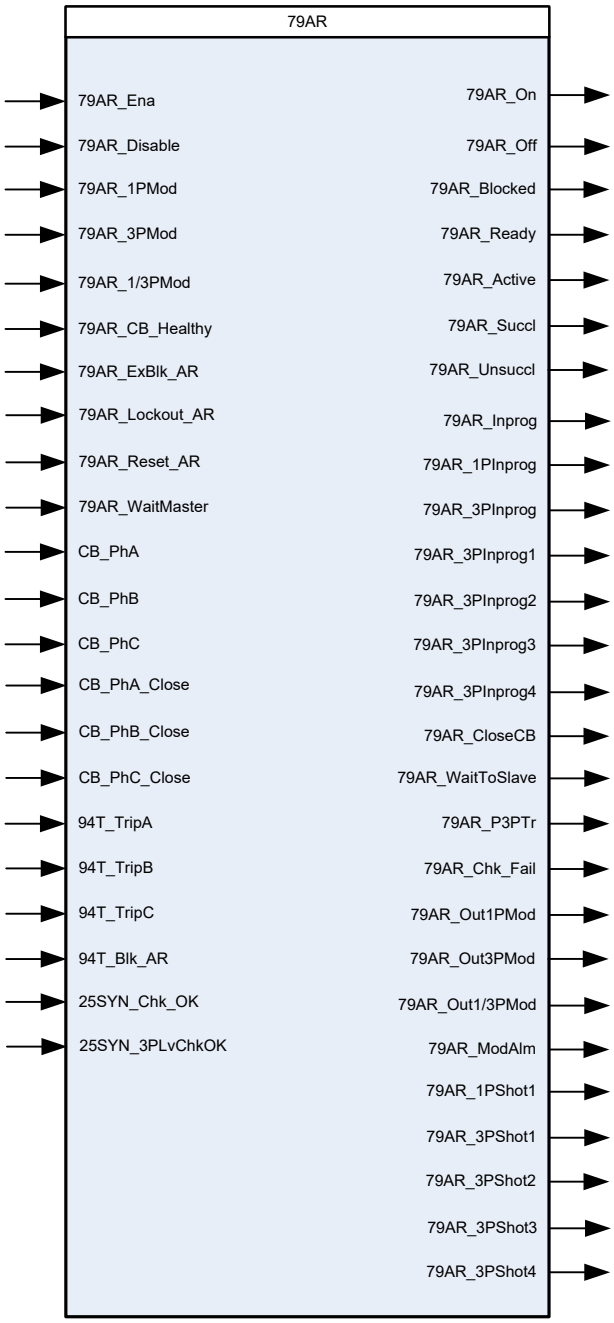
3.31 Automatic Reclosure 79AR

3.31.1 Overview

To maintain the integrity of the overall electrical transmission system, the device is installed on the transmission system to isolate faulted segments during system disturbances. Faults caused by lightning, wind, or tree branches could be transient in nature and may disappear once the circuit is de-energized. According to statistics, 80%~90% of the faults on overhead lines are the transient faults. Auto-reclosing systems are installed to restore the faulted section of the transmission system once the fault is extinguished (providing it is a transient fault). For certain transmission systems, auto-recloser is used to improve system stability by restoring critical transmission paths as soon as possible.

When the auto-reclosing command is issued, the reclaim timer starts. If the circuit breaker does not trip again, the auto-recloser resets at the end of the reclaim time. If another protection operates during the reclaim time delay, this relay either proceeds to the next shot in the programmed auto-reclosing cycle, or it lockouts if all programmed reclose attempts have been made. The reclaim time should be set long enough to allow this relay to operate when the circuit breaker is automatically closed onto a fault.

3.31.1.1 Function Block



3.31.1.2 Signals

Table 3.31-1 79AR Input Signals

NO.	Signal	Description
1	79AR_Ena	Binary input for enabling AR. If the logic setting 79AR_ExtCtrl =1, enabling AR will be controlled by the external input
2	79AR_Disable	Binary input for disabling AR. If the logic setting 79AR_ExtCtrl =1, disabling AR will be controlled by the external input

NO.	Signal	Description
3	79AR_1PMod	Input signal to set 1-pole 79AR mode
4	79AR_3PMod	Input signal to set 3-pole 79AR mode
5	79AR_1/3PMod	Input signal to set 1/3-pole 79AR mode
6	79AR_CB_Healthy	Binary input of circuit breaker in healthy condition
7	79AR_ExBlk_AR	Binary input signal to block auto-recloser
8	79AR_Lockout_AR	Binary input signal to lockout auto-recloser, if AR is lockout, it needs to be reset automatically or manually
9	79AR_Reset_AR	Binary input signal to reset auto-recloser. If the logic setting 79AR_AutoRst=0, the lockout AR only can be reset by this input.
10	79AR_WaitMaster	Input signal of waiting for reclosing permissive signal from master AR (when reclosing multiple circuit breakers)
11	CB_PhA	Normally closed contact of A-phase of circuit breaker
12	CB_PhB	Normally closed contact of B-phase of circuit breaker
13	CB_PhC	Normally closed contact of C-phase of circuit breaker
14	CB_PhA_Close	Normally opened contact of A-phase of circuit breaker
15	CB_PhB_Close	Normally opened contact of B-phase of circuit breaker
16	CB_PhC_Close	Normally opened contact of C-phase of circuit breaker
17	94T_TripA	Tripping A-phase circuit breaker
18	94T_TripB	Tripping B-phase circuit breaker
19	94T_TripC	Tripping C-phase circuit breaker
20	94T_Blk_AR	Block signal of auto-recloser from line trip
21	25SYN_Chk_OK	Synchronizing OK signal from 25SYN
22	25SYN_3PLvChkOK	Live three-phase check condition of AR is met from 25SYN

Table 3.31-2 79AR Output Signals

NO.	Signal	Description
1	79AR_On	Automatic reclosure is enabled
2	79AR_Off	Automatic reclosure is disabled
3	79AR_Blocked	Automatic reclosure is blocked
4	79AR_Ready	Automatic reclosure is ready for reclosing cycle
5	79AR_Active	Automatic reclosing is active
6	79AR_Succl	Automatic reclosing is successful
7	79AR_Unsuccl	Automatic reclosing is unsuccessful
8	79AR_Inprog	Automatic reclosing cycle is in progress
9	79AR_1PInprog	1-pole AR is in progress for shot 1
10	79AR_3PInprog	3-pole AR is in progress

NO.	Signal	Description
11	79AR_3PInprog1	3-pole AR is in progress for shot 1
12	79AR_3PInprog2	3-pole AR is in progress for shot 2
13	79AR_3PInprog3	3-pole AR is in progress for shot 3
14	79AR_3PInprog4	3-pole AR is in progress for shot 4
15	79AR_CloseCB	Close command for circuit breaker
16	79AR_WaitToSlave	Waiting signal of AR which will be sent to slave (when reclosing multiple circuit breakers)
17	79AR_P3PTr	Three-phase trip is prepared
18	79AR_Chk_Fail	Re-closing condition checking fail signal
19	79AR_Out1PMod	Output of 1-pole AR mode
20	79AR_Out3PMod	Output of 3-pole AR mode
21	79AR_Out1/3PMod	Output of 1/3-pole AR mode
22	79AR_ModAlm	Alarm signal from AR mod set error
23	79AR_1PShot1	The first 1-pole reclosing attempts
24	79AR_3PShot1	The first 3-pole reclosing attempts
25	79AR_3PShot2	The second 3-pole reclosing attempts
26	79AR_3PShot3	The third 3-pole reclosing attempts
27	79AR_3PShot4	The fourth 3-pole reclosing attempts

3.31.2 Operation Principle

This auto-reclosing logic can be used with either integrated device or external device. When the auto-recloser is used with integrated device, the internal protection logic can initiate AR, moreover, a tripping contact from external device can be connected to the device via opto-coupler input to initiate integrated AR function.

When external auto-recloser is used, the device can output some configurable output to initiate external AR, such as, contact of initiating AR, phase-segregated tripping contact, single-phase tripping contact, three-phase tripping contact and contact of blocking AR. According to requirement, these contacts can be selectively connected to external auto-recloser device to initiate AR.

For phase-segregated circuit breaker, AR mode can be 1-pole AR for single-phase fault and 3-pole AR for multi-phase fault, or always 3-pole AR for any kinds of fault according to system requirement. For persistent fault or multi-shot AR number preset value is reached, the device will send final tripping command. The device will provide appropriate tripping command based on faulty phase selection if adopting 1-pole AR.

3.31.2.1 AR OFF AND ON

AR function can be enabled by internal logic settings of AR mode or external signal via binary inputs in addition to internal logic setting 79AR_Ena. When logic setting 79AR_ExtCtrl is set as “1”, AR enable are determined by external signal via binary inputs and logic settings. When logic setting 79AR_ExtCtrl set as “0”, AR enable are determined only by logic settings. When AR is enabled, the

device will output contact 79AR_On, otherwise the device outputs the signal 79AR_Off.

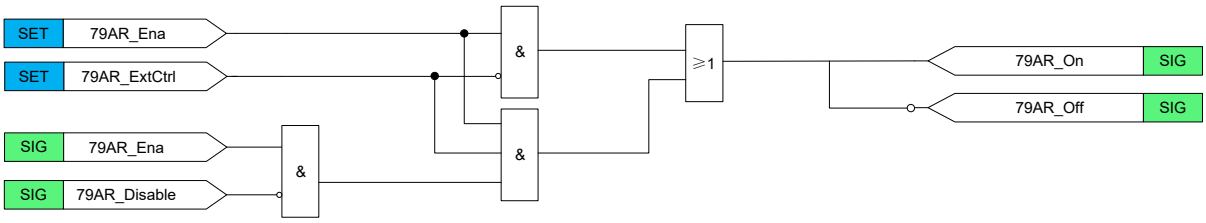


Figure 3.31.1 AR On

3.31.2.2 AR Mode selection

For the first reclosing of multi-shot AR, AR mode can be 1-pole AR or 3-pole AR, however, the selection is valid only to the first reclosing, after that it can only be 3-pole AR.

When logic setting 79AR_SetOption is set as “0”, AR mode is determined by logic settings. When logic setting 79AR_SetOption is set as “1”, AR mode is determined by external signal via input signals. The selected mode is reported as a Boolean on the 79AR_Out1PMod,79AR_Out3PMod and 79AR_Out1/3PMod output.

If there are more than one mode for 1-pole AR, 3-pole AR,1/3-pole AR, and AR is enabled, the device will output contact 79AR_ModAlm. When the AR is disabled or the 79AR_ModAlm is activated, the 79AR_Out1PMod,79AR_Out3PMod and 79AR_Out1/3PMod output contact are inactivated.

3.31.2.3 AR Ready

An auto-recloser must be ready to operate before performing reclosing. The output signal 79AR_Ready means that the auto-recloser can perform at least one time of reclosing function, i.e., breaker open-close-open. When the device is energized or after the settings are modified, 79AR cannot be ready unless the following conditions are met:

1. 79AR function is enabled.

2. The circuit breaker is ready, such as, normal storage energy and no low pressure signal.

3. The duration of the circuit breaker in closed position before fault occurrence is not less than the setting 79AR_T_CBclosed.

4. There is no block signal of auto-reclosing.

The input signal 79AR_CB_Healthy must be energized before auto-recloser gets ready. Because most circuit breakers can finish one complete process: open-closed-open, it is necessary that circuit breaker has enough energy before reclosing. When the time delay of AR is exhausted, AR will be blocked if the input signal 79AR_CB_Healthy is still not energized within time delay 79AR_T_CBhealthy.

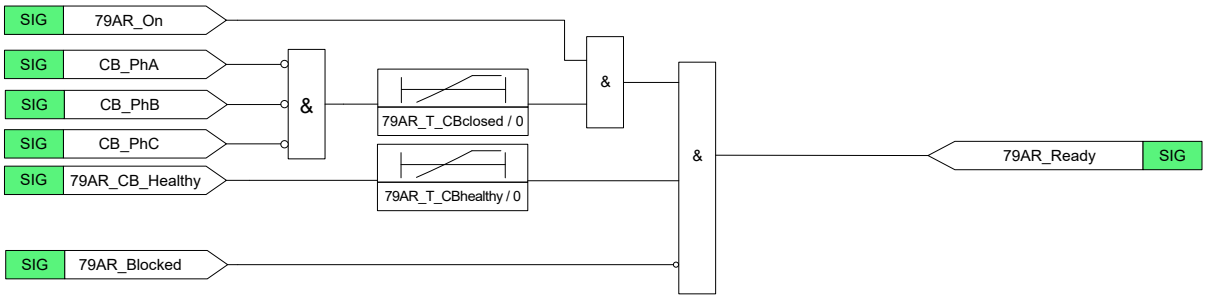


Figure 3.31.2 AR Ready

When auto-recloser is blocked (the blocked logic is show in section 3.31.2.7), auto-recloser will be discharged immediately and next auto-reclosing will be disabled.

When AR is enabled, the device will output the signal 79AR_P3PTr if AR is not ready, or AR mode is set as 3-Pole AR, or another fault occurs after the circuit breaker is open. 79AR_P3PTr output is usually connected to the trip function 94T to force the coming trip to be three-phase.

3.31.2.4 AR Initiation

When 79AR is initiated, the device will output a signal 79AR_Active until AR drop off (Reset Reclaim).

1.AR initiated by tripping signal of line protection

79AR can be initiated by tripping signal of line protection, and the tripping signal may be from internal trip signal or external trip signal.

When selecting 1-pole or 1/3-pole, line single-phase fault will trigger 1-pole 79AR. When 79AR is ready to reclosing and the single-phase tripping command is received, this single-phase tripping command will be kept in the device, and 1-pole 79AR will be initiated after the single-phase tripping command drops off. The single-phase tripping command kept in the device will be cleared after the completion of auto-reclosing sequence.

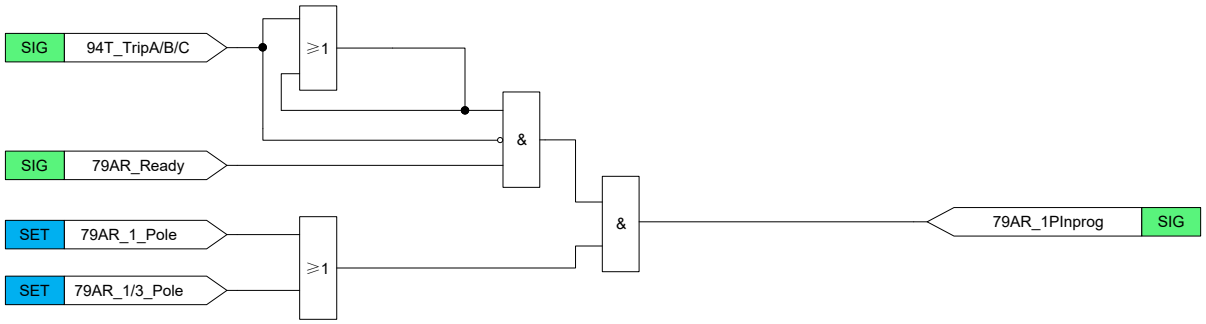


Figure 3.31.3 1-pole AR Initiated by Line Tripping Signal

When selecting 3-pole or 1/3-pole, three-phase tripping will trigger 3-pole 79AR. When 79AR is ready to reclosing and the three-phase tripping command is received, this three-phase tripping command will be kept in the device, and 3-pole 79AR will be initiated after the three-phase tripping command drops off. The three-phase tripping command kept in the device will be cleared after the completion of auto-reclosing sequence.

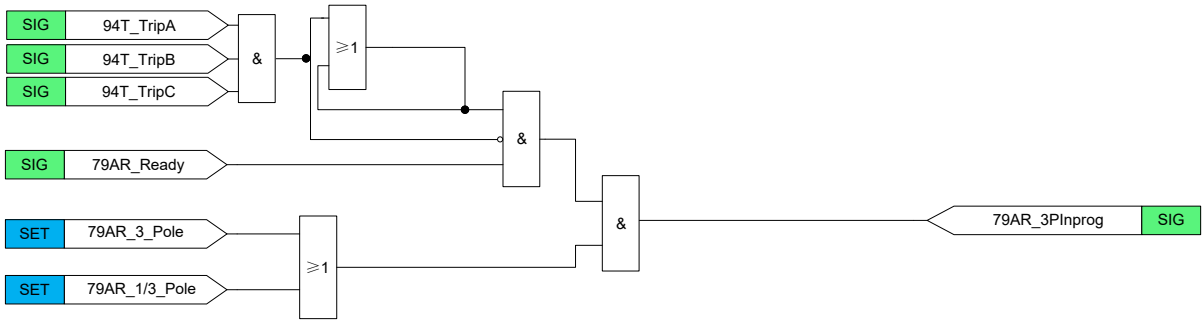


Figure 3.31.4 3-pole AR Initiated by Line Tripping Signal

2.AR initiated by CB State

A logic setting 79AR_CB_Str is available for selection that 79AR is initiated by CB state. Under normal conditions, when 79AR is ready to reclosing, 79AR will be initiated if circuit breaker is open and corresponding phase current is nil.

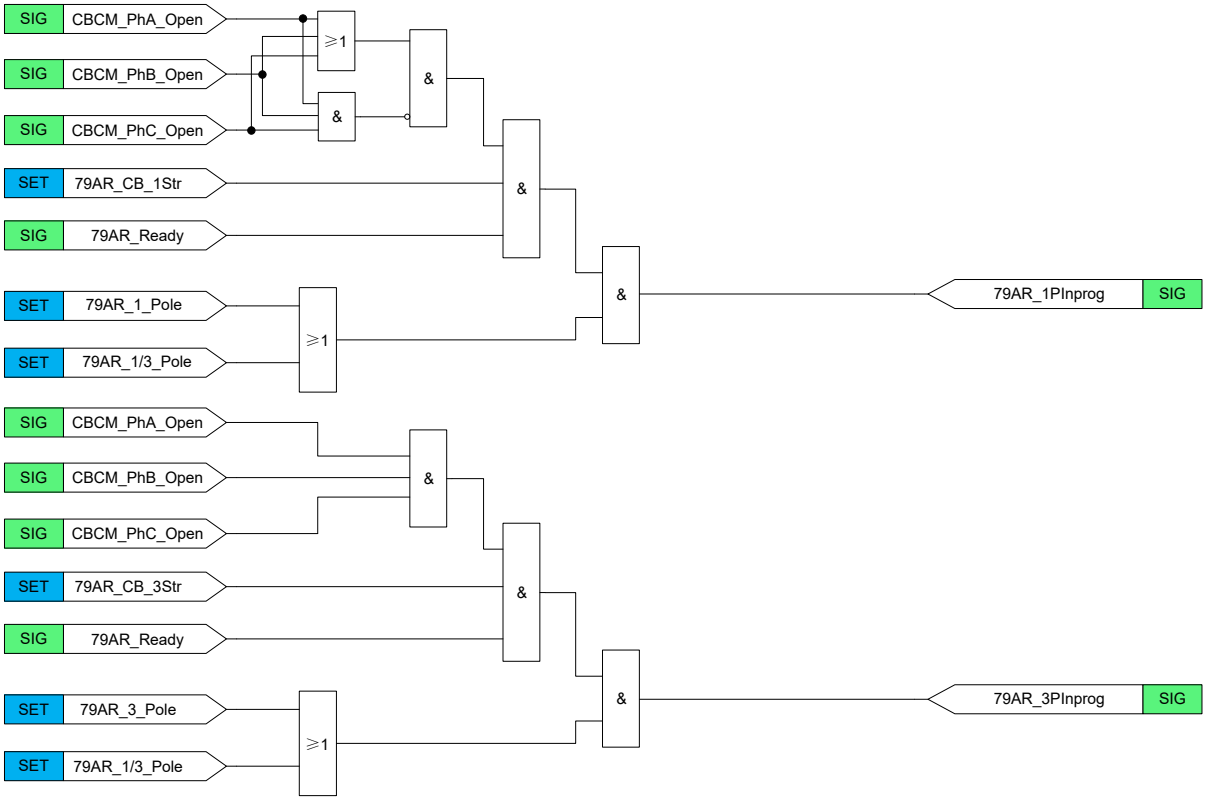


Figure 3.31.5 79AR Initiated by CB State

3.31.2.5 AR Reclosing

After AR is initiated, the AR is in progress. For 1-pole AR, in order to prevent pole discrepancy protection from maloperation under pole discrepancy conditions, the contact of “79AR_1PInprog” can be used to block pole discrepancy protection.

When the dead time delay of AR expires after AR is initiated, as for 1-pole AR, when the setting 25SYN_3PLvChk is set as “0”, the result of synchronism check will not be judged, and reclosing command will be output directly. When the setting 25SYN_3PLvChk is set as “1”, the reclosing is

not permissible unless live three-phase check is met. As far as the 3-pole AR, if the synchronism check is enabled, the release of reclosing command shall be subject to the result of synchronism check. After the dead time delay of AR expires, if the synchronism check is still unsuccessful within the time delay 79AR_T_WaitSyn, the signal of synchronism check failure 79AR_Chk_Fail will be output and the AR will be blocked. If 3-pole AR with no-check is enabled, the condition of synchronism check success 25SYN_Chk_OK will always be established. And the signal of synchronism check success 25SYN_Chk_OK from the synchronism check logic can be applied by auto-reclosing function inside the device or external auto-recloser device.

Reclosing pulse length may be set through the setting 79AR_T_Pluse.

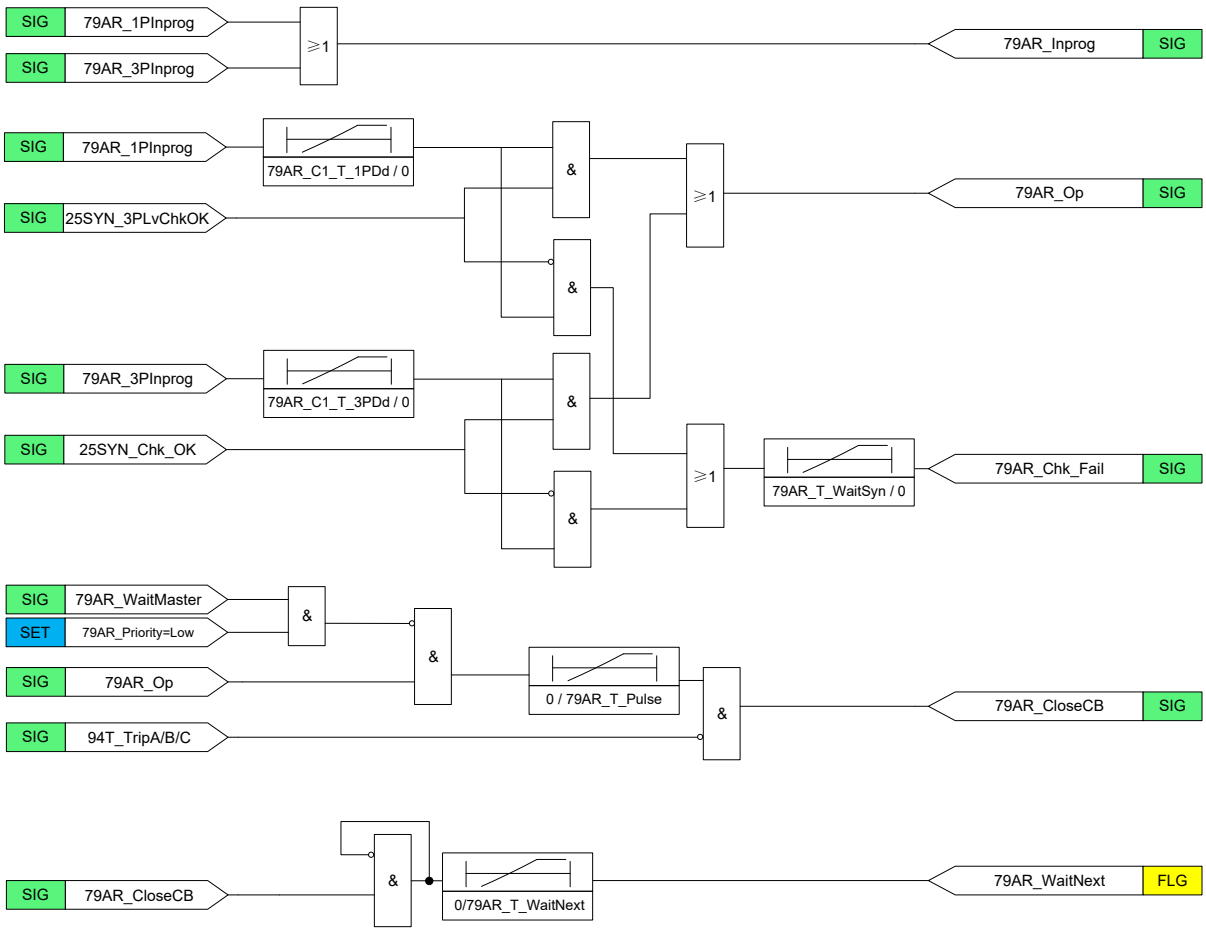


Figure 3.31.6 79AR Pulse and Reset

If a circuit breaker close command is given successfully at the end of the dead time, a reclaim time starts. If the circuit breaker does not trip again within reclaim time, the auto recloser indicates a successful reclosing and resets into "ready" status. If the protection trips again during the reclaim time, the sequence advances to the next shot. If all reclosing attempts have been made and the circuit breaker does not remain closed, the auto recloser indicates an unsuccessful reclosing. Each time a breaker close command is given, a shot counter is incremented by one.

The auto recloser is set as master or slave in multi-breaker arrangements with sequential reclosing with the setting 79AR_Priority. While the master is in progress, it issues the “79AR_WaitToSlave” output. After an unsuccessful reclosing the 79AR_WaitToSlave output is also maintained. The

output signal “79AR_WaitToSlave” is usually configured to the signal “79AR_WaitMaster” of slave AR. Slave AR is permissible to reclosing only if master AR is reclosed successfully.

A setting 79AR_T_WaitForMaster sets a maximum wait time for the “79AR_WaitMaster” input to reset. If the wait time expires, the reclosing cycle of the slave is blocked.

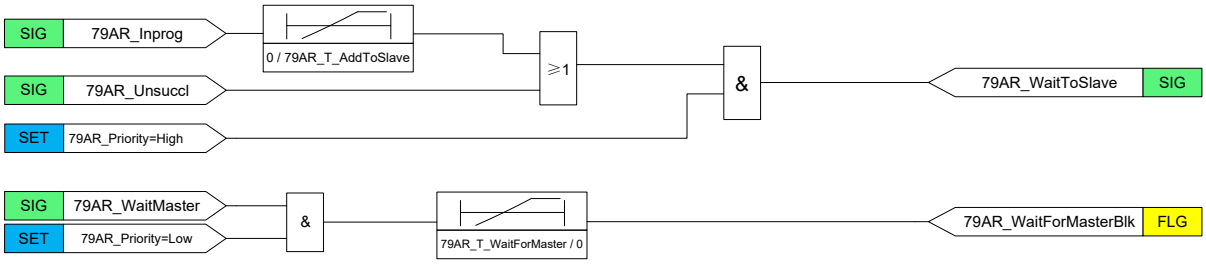


Figure 3.31.7 79AR Wait to slave signal

3.31.2.6 Reclosing Success and Unsuccess

For transient fault, the fault will be cleared after the device operates to trip. After the reclosing command is issued, AR will drop off after time delay 79AR_T_WaitNext, and can carry out next reclosing. When the reclosing is unsuccessful or the reclosing condition is not met after AR initiated, the reclosing will be considered as unsuccessful, including the following cases.

1) For one-shot AR, if the tripping command is received again within reclaim time after the reclosing pulse is issued, the reclosing shall be considered as unsuccessful.

2) For multi-shot AR, if the reclosing times are equal to the setting value of AR number and the tripping command is received again after the last reclosing pulse is issued, the reclosing shall be considered as unsuccessful.

3) A new shot is initiated during the 79AR_T_WaitNext after AR reclose.

4) The logic setting 79AR_UnsucCBChk is available to judge whether the reclosing is successful by CB state, when it is set as “1”. If CB is still in open position with a time delay 79AR_T_Unsuc after the reclosing pulse is issued, the reclosing shall be considered as unsuccessful. For this case, the device will issue a signal 79AR_Unsuccl to indicate that the reclosing is unsuccessful. AR will be blocked if the reclosing shall be considered as unsuccessful.

After unsuccessful AR is confirmed, if 79AR_UnsucBlk=1, AR will be lockout and AR ready will reset when AR is failure, so AR can be ready only after releasing lockout reset and the ready conditions are met again. If 79AR_UnsucBlk=0, AR ready will reset but not lockout when AR is failure, so AR will be ready after the ready conditions are met.

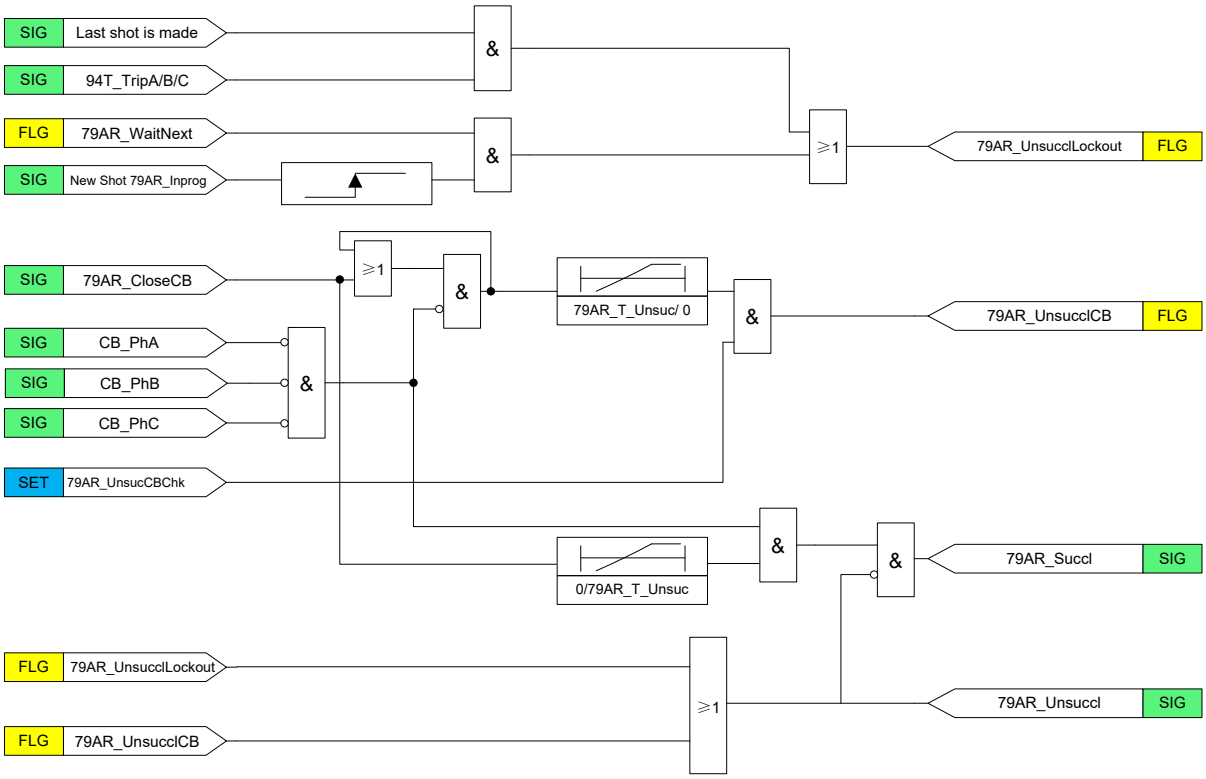


Figure 3.31.8 79AR Success and Unsuccess

3.31.2.7 AR Block and lockout

Beside the above unsuccessful conditions, there are some other lockout conditions.

1) The input signal 79AR_Lockout_AR=1;

2) The flag 79AR_UnsucclCB = 1 and the setting 79AR_UnsucBlk = 1.

3) After the dead time is escaped, the automatic sequence initiation is not allowed because of a synchronization failure when the time setting 79AR_T_WaitSyn expires.

4) The protection trip signal has been active longer than the time set 79AR_T_TrFail

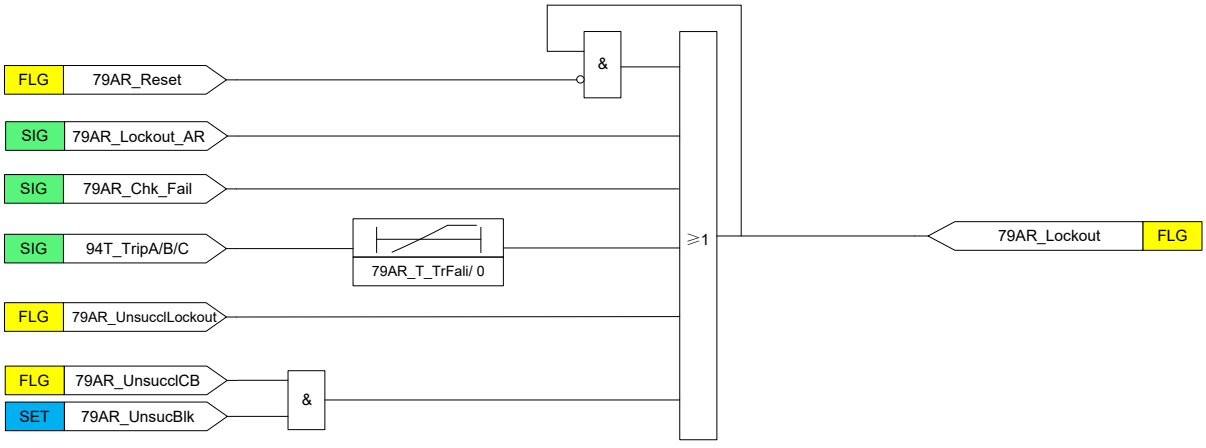


Figure 3.31.9 79AR Lockout conditions

When BI 79AR_BlockAR=1, or AR is in lockout, the 79AR_Blocked BO is active.

The 79AR_Blocked BO including the following cases.

1) The input signal 79AR_ExBlk_AR=1;

2) The internal blocking condition of AR is met (The input signal 94T_Blk_AR is fulfilled.), auto-recloser will be discharged immediately and next auto-reclosing will be disabled.

3) When one-shot and 1-pole AR is enabled, auto-recloser will be blocked immediately if there are binary inputs of multi-phase CB position is energized.

4) AR is in lockout

5) If the wait time expires 79AR_T_WaitForMaster for the “79AR_WaitMaster” input to reset, the reclosing cycle of the slave is blocked.

6) When a fault occurs under pole disagreement condition, blocking AR can be enabled or disabled. The time delay 79AR_T_SecFault is used to discriminate another fault which begins after 1-pole AR initiated. AR will be blocked if another fault happens after this time delay if the logic setting 79AR_PDBlk is set as “1”, and 3-pole AR will be initiated if 79AR_PDBlk is set as “0”.

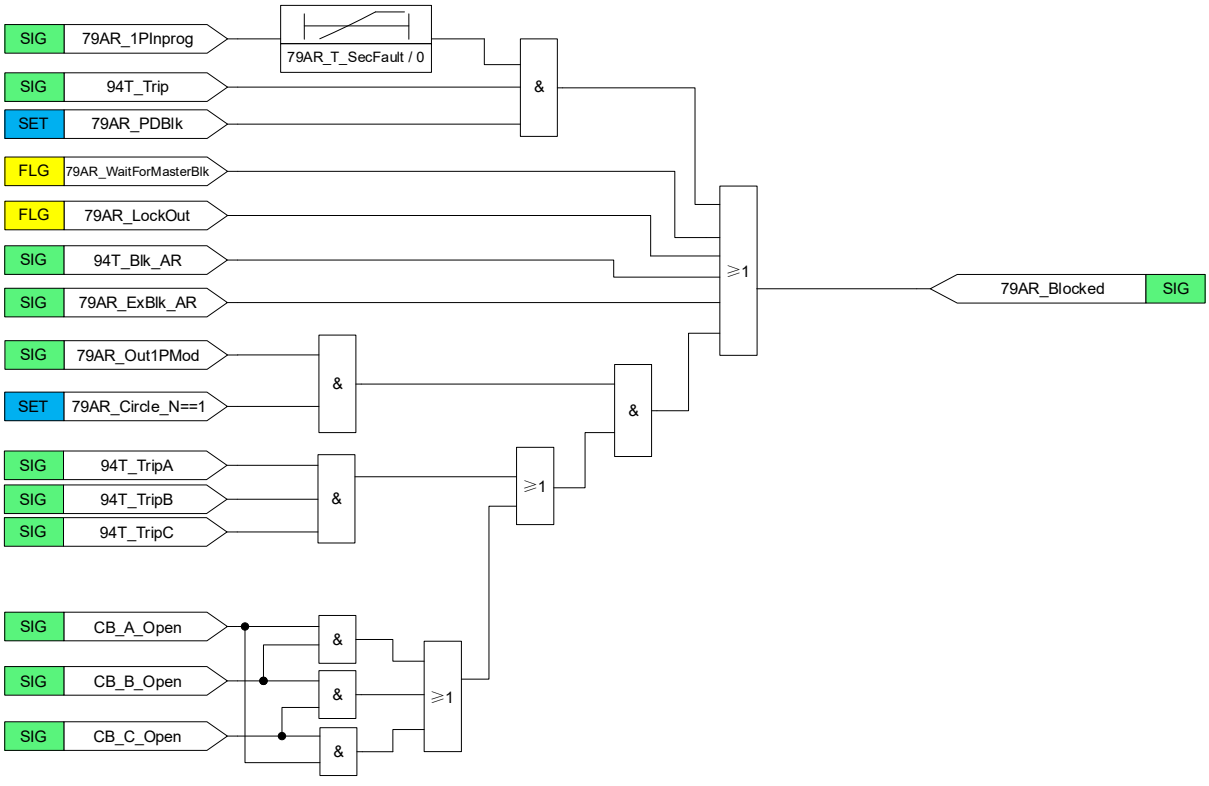


Figure 3.31.10 AR Blocked conditions

3.31.2.8 Reset AR lockout

When the AR function is in lockout status, it means that new sequences cannot be initialized, because AR is insensitive to initiation commands. It can be released from the lockout state if all blocked signals disappear (such as 79AR_Lockout_AR BI=0) in the following ways:

• The function is reset through by 79AR_Reset_AR BI manually or locally control.

• If the setting 79AR_AutoRst=1, the lockout is automatically reset after the reclaim time.

Note: If the setting 79AR_AutoRst=0, the lockout can be reset only by 79AR_Reset_AR BI.

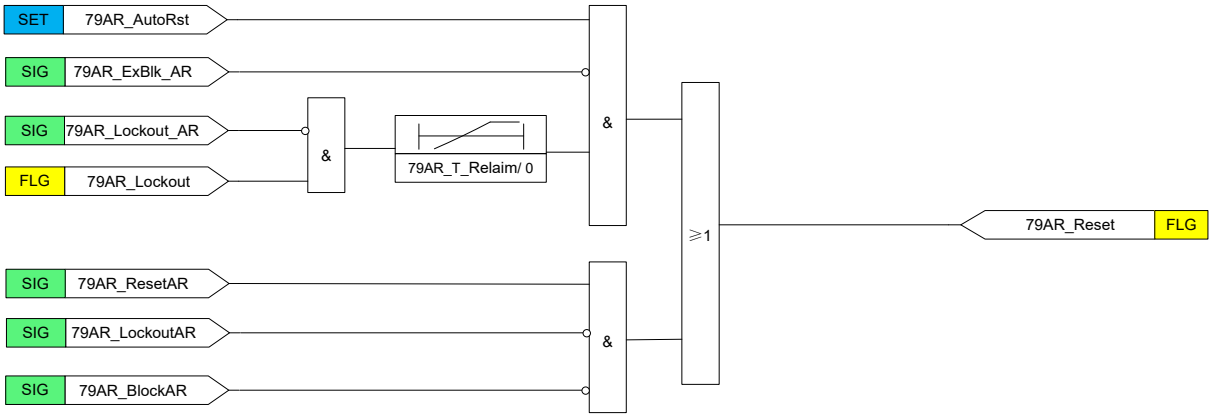


Figure 3.31.11 Reset AR Lockout

3.31.2.9 Reclosing shots count

The recloser shall be provided with counters to count the number of each reclosing attempts, each counter will plus 1 when the reclosing attempt is sent and it can be cleared by submenu [Clr BOCnt], the number will be display in device MENU [Monitor] -> [BO Count].

3.31.3 Settings

Table 3.31-3 79AR Settings

NO	Name	Range	Unit	Step	Default	Description
1	79AR_Ena	0 or 1	-	1	0	Enabling/disabling auto-reclosing 0: disable 1: enable
2	79AR_ExtCtrl	0 or 1	-	1	0	Enabling/disabling AR by external input signal besides logic setting 79AR_Ena 0: only logic setting 1: logic setting and external input signal

NO	Name	Range	Unit	Step	Default	Description
3	79AR_SetOption	0 or 1	-	1	0	Control option of AR mode 0: select AR mode by internal logic settings 1: select AR mode by external input signals
4	79AR_Priority	0: Non 1: High 2: Low	-	1	0	Option of AR priority None: single-breaker arrangement High: master AR of multi-breaker arrangement Low: slave AR of multi-breaker arrangement
5	79AR_1_Pole	0 or 1	-	1	0	Enabling/disabling 1-pole 79AR mode 0: disable 1: enable
6	79AR_3_Pole	0 or 1	-	1	0	Enabling/disabling 3-pole 79AR mode 0: disable 1: enable
7	79AR_1/3_Pole	0 or 1	-	1	0	Enabling/disabling 1/3-pole 79AR mode 0: disable 1: enable
8	79AR_CB_1Str	0 or 1	-	1	0	Enabling/disabling 79AR be initiated by open state of circuit breaker (single phase) 0: disable 1: enable
9	79AR_CB_3Str	0 or 1	-	1	0	Enabling/disabling 79AR be initiated by open state of circuit breaker (three phase) 0: disable 1: enable
10	79AR_UnsucCBChk	0 or 1	-	1	0	Enabling/disabling confirm whether AR is successful by checking CB position 0: disable 1: enable

NO	Name	Range	Unit	Step	Default	Description
11	79AR_UnsucBlk	0 or 1	-	1	0	Enabling/disabling block AR at unsuccessful reclosing 0: disable 1: enable
12	79AR_PDBlk	0 or 1	-	1	1	Enabling/disabling auto-reclosing blocked when a fault occurs under pole disagreement condition 0: disable 1: enable
13	79AR_AutoRst	0 ~1	-	1	1	Enabling/disabling auto reset the blocked status 0: disable 1: enable
14	79AR_Circle_N	1~4	-	1	1	Maximum number of reclosing attempts
15	79AR_T_CBclosed	0.000~600.000	s	0.001	10	Time delay of circuit breaker in closed position before reclosing
16	79AR_T_CBhealthy	0.000~600.000	s	0.001	10	Time delay to wait for CB healthy
17	79AR_T_TrFail	0.000~600.000	s	0.01	0.2	Time delay of excessive trip signal to Lockout AR
18	79AR_C1_T_1PDd	0.000~600.000	s	0.001	10	Dead time of first shot 1-pole reclosing
19	79AR_C1_T_3PDd	0.000~600.000	s	0.001	10	Dead time of first shot 3-pole reclosing
20	79AR_C2_T_3PDd	0.000~600.000	s	0.001	10	Dead time of second shot 3-pole reclosing
21	79AR_C3_T_3PDd	0.000~600.000	s	0.001	10	Dead time of third shot 3-pole reclosing
22	79AR_C4_T_3PDd	0.000~600.000	s	0.001	10	Dead time of fourth shot 3-pole reclosing
23	79AR_T_WaitSyn	0.000~600.000	s	0.001	10	Maximum wait time for synchronism check
24	79AR_T_Pluse	0.000~5.000	s	0.001	0.2	Pulse width of 79AR closing signal

NO	Name	Range	Unit	Step	Default	Description
25	79AR_T_WaitNext	0.000~600.000	s	0.001	0.4	Wait time of Next 79AR
26	79AR_T_Reclaim	0.000~600.000	s	0.001	10	Reclaim time of 79AR
27	79AR_T_Unsuc	0.000~600.000	s	0.001	0.2	Maximum wait time for circuit breaker closing before indicating unsuccessful
28	79AR_T_WaitForMaster	0.000~600.000	s	0.001	3	Maximum wait time for release from master AR
29	79AR_T_AddToSlave	0.000~600.000	s	0.001	0.2	Additional time delay for the slave AR
30	79AR_T_SecFault	0.000~600.000	s	0.001	0.2	Time delay of discriminating another fault, and begin to times after 1-pole AR initiated, 3-pole AR will be initiated if another fault happens during this time delay. AR will be blocked if another fault happens after that.

3.32 Faulty Phase Selection FPS

3.32.1 Overview

Faulty phase selection is used to discriminate faulty phase for all kinds of fault type. If protection element operates, faulty phase selection is succeeded and the device output tripping command. Faulty phase selection is adaptive to both earthed system and unearthed system. For the unearthed system, earthed protection elements should be disabled, such as phase-to-ground distance protection, earth fault protection, and only phase-to-phase protection elements are enabled, such as phase-to-phase distance protection, phase overcurrent protection.

When current differential protection is enabled, operation phase is the selected faulty phase if current differential protection operates.

Detecting the superimposed operating voltage

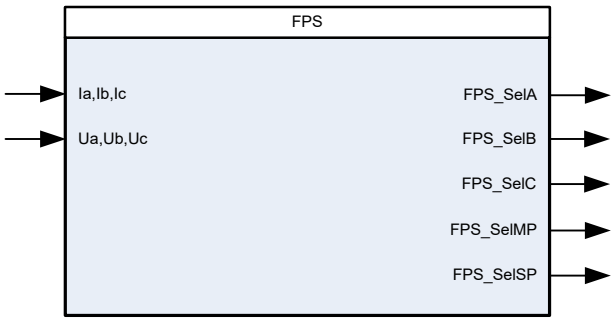
Detecting the phase difference between I0 and I2A

When phase overcurrent element operates, pickup phase due to overcurrent is judged as a faulty phase.

When phase overvoltage element operates, pickup phase due to overvoltage is judged as a faulty phase.

When phase undervoltage element operates, pickup phase due to undervoltage is judged as a faulty phase.

3.32.1.1 Function Block



3.32.1.2 Signals

Table 3.32-1 FPS Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input

Table 3.32-2 FPS Output Signals

NO.	Signal	Description
1	FPS_SelA	Faulty phase selection result of phase A
2	FPS_SelB	Faulty phase selection result of phase B
3	FPS_SelC	Faulty phase selection result of phase C
4	FPS_SelMP	Faulty phase selection result of multi-phase
5	FPS_SelSP	Faulty phase selection result of single phase

3.32.2 Operation Principle

3.32.2.1 Differential Current Element

Because current differential protection is simple and reliable, its priority of faulty phase selection is high. When current differential protection is enabled, operation phase is the selected faulty phase if current differential protection operates.

3.32.2.2 Superimposed Operating Voltage Element

Variation of phase operating voltage

Phase A: $\Delta UOPA$

Phase B: $\Delta UOPB$

Phase C: $\Delta UOPC$

Variation of phase-to-phase operating voltage

Phase AB: $\Delta UOPAB$

Phase BC: $\Delta UOPBC$

Phase CA: $\Delta UOPCA$

$\Delta UO\Phi MAX = \mathrm{Max}(\Delta UOPA, \Delta UOPB, \Delta UOPC)$

$\Delta UO\Phi\Phi MAX = \mathrm{Max}(\Delta UOPAB, \Delta UOPBC, \Delta UOPCA)$

If $\Delta UO\Phi MAX$ is several times higher than the variation of operating voltages of other two phases, the single-phase fault is ensured, otherwise, the multi-phase fault is ensured.

3.32.2.3 I0 and I2A Selection Element

The phase selection algorithm uses the angle relation between I0 and I2A of the device. There are three faulty phase selection regions.

Depended on the phase relation between I0 and I2A, the faulty phase can be determined.

1. -60º<Arg(I0/I2A)<60º, region A is selected, possible faulty phase is phase A or phase BC.
2. 60º<Arg(I0/I2A)<180º, region B is selected, possible faulty phase is phase B or phase CA.
3. 180º<Arg(I0/I2A)<300º, region C is selected, possible faulty phase is phase C or phase AB.

For single-phase earth fault, I0 and I2 of faulty phase are in-phase and its distance element operates.

For phase-to-phase earth fault, I0 and I2 of non-faulty phase are in-phase but its distance element does not operate.

3.32.2.4 Phase Current or Phase Voltage Element

When phase overcurrent element or phase voltage element pick up, the corresponding phase which is overcurrent, overvoltage or undervoltage will be judged as a faulty phase.

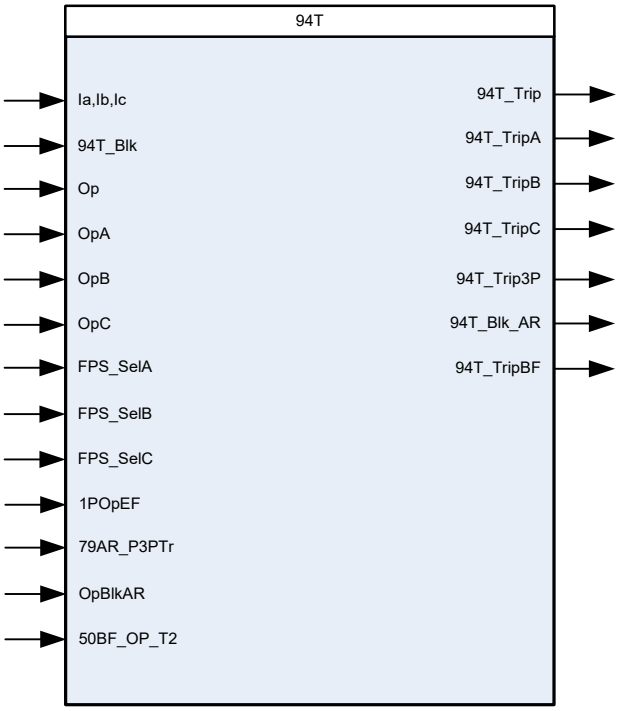
3.33 Trip Logic 94T

3.33.1 Overview

94T provides a pulse with settable time period to ensure a trip pulse of sufficient length, as well as block signals for correct co-operation with 79AR.

The function gathers signals from FPS and all the operation signal of all the protection functions then converts the signals to appropriate tripping pulse. The device can implement phase-segregated tripping or three-phase tripping.

3.33.1.1 Function Block



3.33.1.2 Signals

Table 3.33-1 94T Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	94T_Blk	Blocking signal of 94T
3	Op	Operation signal to trip all phases
4	OpA	Operation signal to trip phase A
5	OpB	Operation signal to trip phase B
6	OpC	Operation signal to trip phase C
7	FPS_SelA	FPS selected phase A as the faulty phase
8	FPS_SelB	FPS selected phase B as the faulty phase
9	FPS_SelC	FPS selected phase C as the faulty phase
10	1POpEF	Input for phase selective earth fault trip
11	79AR_P3PTr	Input signal of permitting three-phase tripping. When this signal is valid, three-phase tripping will be adopted for any kind of faults.
12	OpBlkAR	Operation signal to block auto-recloser
13	50BF_OP_T2	Adjacent three-phase circuit breaker tripping signal from 50BF

Table 3.33-2 94T Output Signals

NO.	Signal	Description
1	94T_Trip	Tripping any phase circuit breaker
2	94T_TripA	Tripping A-phase circuit breaker
3	94T_TripB	Tripping B-phase circuit breaker
4	94T_TripC	Tripping C-phase circuit breaker
5	94T_Trip3P	Tripping three-phase circuit breaker
6	94T_Blk_AR	Blocking auto-recloser
7	94T_TripBF	Tripping breaker failure

3.33.2 Operation Principle

The duration of tripping pulse can be adjusted by the setting 94T_T_Pulse. The pulse length should be long enough to secure the opening of the circuit breaker. When the time delay is expired, for phase-segregated tripping, the tripping signal will drop off immediately if the fault current of corresponding phase is less than I_Line, otherwise, the tripping signal will be always kept until the faulty current of corresponding phase is less than I_Line. For three-phase tripping, the tripping signal will drop off immediately if three-phase currents are all less than I_Line, otherwise, the tripping signal will be always kept until three-phase currents are all less than I_Line.

There is a single input (Op) through which all trip output signals from the protection functions within the IED or from external protection functions via one or more of the IEDs' binary inputs are routed. It has a single three-phase trip output (94T_Trip3P) to connect to one or more of the IEDs' binary outputs, as well as to other functions within the IED requiring this signal.

94T has separate inputs (OpA, OpB, OpC) which are used for single-phase tripping from the functions which offer phase segregated operation outputs.

The inputs 1POpEF enable single- phase tripping for those functions which do not have their own phase selection capability (i.e. which have just a single operation output). An example of such a protection function is the residual overcurrent protection. External phase selection for this operation signal shall be provided via inputs FPS_SelA , FPS_SelB and FPS_SelC.

A timer 94T_T_PSFail, secures a three-phase trip command for 1POpEF operation signal in the absence of the external phase selection signals.

94T has three trip outputs 94T_TripA, 94T_TripB and 94T_TripC, every phase can connect to one or more of the binary outputs. These three output signals shall be used as trip signals for individual circuit breaker poles. These signals are important for cooperation with the 79AR function. And a setting 94T_Trp3P_Ena is provided which will force all tripping to be three-phase.

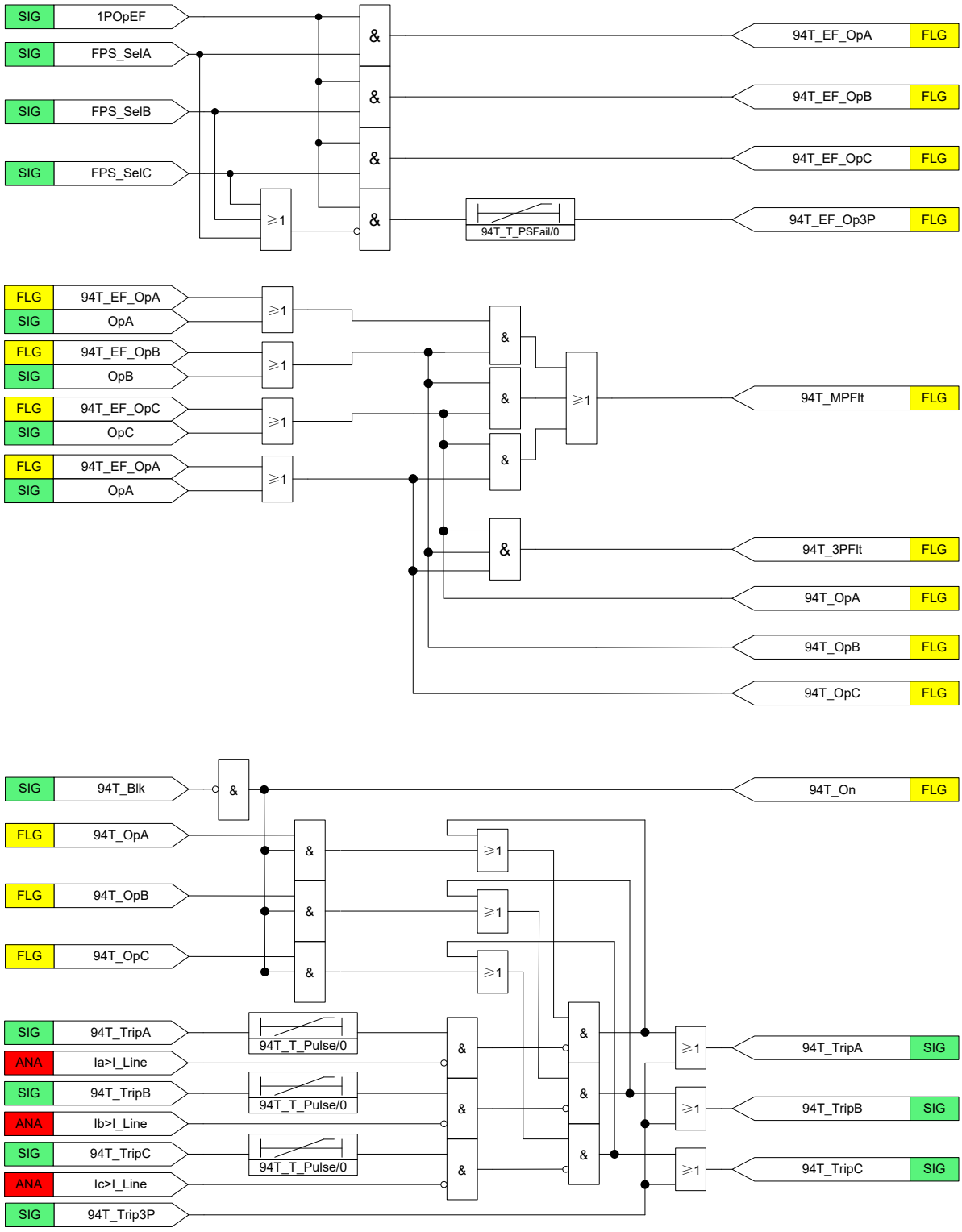
94T is equipped with logic which secures correct operation for evolving faults as well as for reclosing on to persistent faults. A binary input 79AR_P3PTr is provided which will force all tripping to be three-phase. This input is required in order to cooperate with the 79AR function.

94T_Blk_AR output is usually connected to the 79AR function to block the auto recloser. If the general trip is used the auto recloser must be blocked, via the OpBlkAR input, from all back-up

tripping. The breaker failure function must always be connected to block the auto recloser. If the device operates for multi-phase fault and logic setting 94T_MPF_Blk_AR_Ena is set as “1”, or the device operates for three-phase fault and logic setting 94T_3PF_Blk_AR_Ena is set as “1”, the device will output contact 94T_Blk_AR. The 94T_Blk_AR will drop off with a time delay of 2s after the above conditions disappears.

There is a single input (50BF_OP_T2) through breaker failure protection. It has a single trip output (94T_TripBF) to connect to one or more of the IEDs' binary outputs. This output signal shall be used as trip signals for adjacent circuit breakers in case of a tripping failure of the circuit breaker.

3.33.3 Logic


SIG
1POpEF
SIG
FPS_SelA
SIG
FPS_SelB
SIG
FPS_SelC
&
&
&
&
≥1
94T_T_PSFail/0
94T_EF_OpA
FLG
94T_EF_OpB
FLG
94T_EF_OpC
FLG
94T_EF_Op3P
FLG
FLG
94T_EF_OpA
SIG
OpA
FLG
94T_EF_OpB
SIG
OpB
FLG
94T_EF_OpC
SIG
OpC
FLG
94T_EF_OpA
SIG
OpA
≥1
≥1
≥1
≥1
&
&
&
&
≥1
94T_MPFlt
FLG
94T_3PFlt
FLG
94T_OpA
FLG
94T_OpB
FLG
94T_OpC
FLG
SIG
94T_Blk
&
94T_On
FLG
FLG
94T_OpA
FLG
94T_OpB
FLG
94T_OpC
&
&
&
≥1
≥1
≥1
SIG
94T_TripA
ANA
Ia>I_Line
SIG
94T_TripB
ANA
Ib>I_Line
SIG
94T_TripC
ANA
Ic>I_Line
SIG
94T_Trip3P
94T_T_Pulse/0
94T_T_Pulse/0
94T_T_Pulse/0
&
&
&
&
&
&
≥1
≥1
≥1
94T_TripA
SIG
94T_TripB
SIG
94T_TripC
SIG

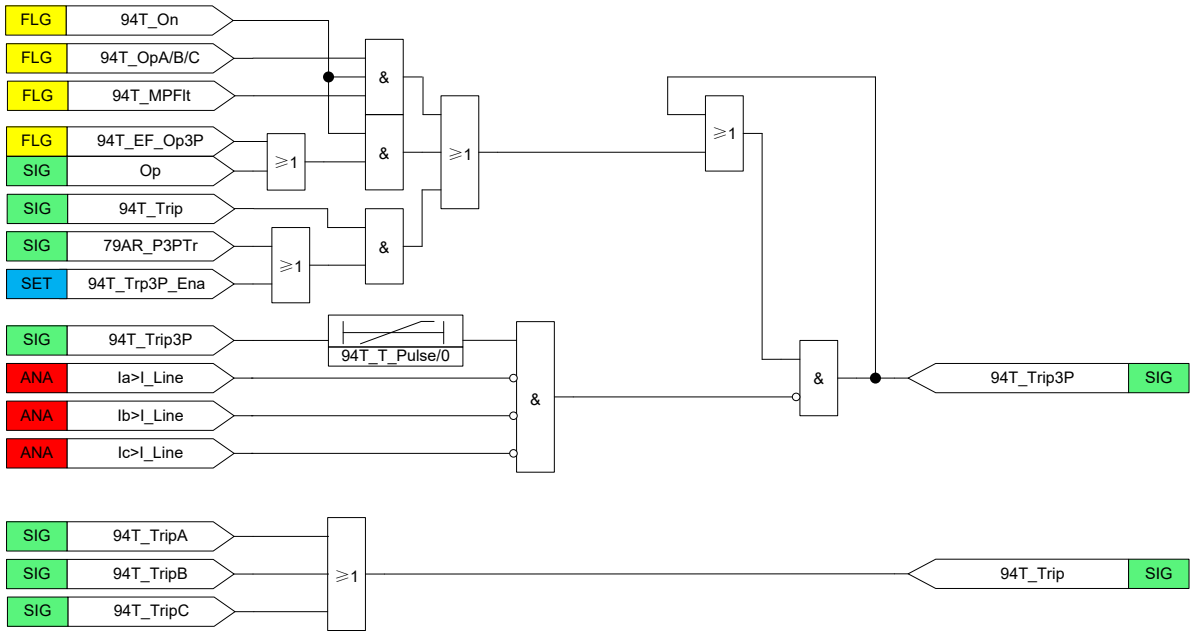


Figure 3.33.1 Logic Diagram of 94T

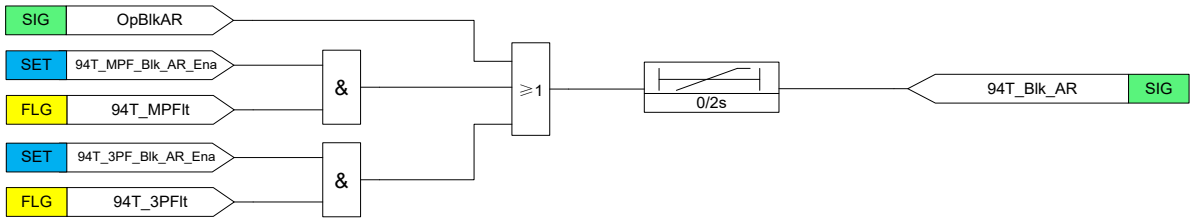


Figure 3.33.2 Logic Diagram of Blocking AR

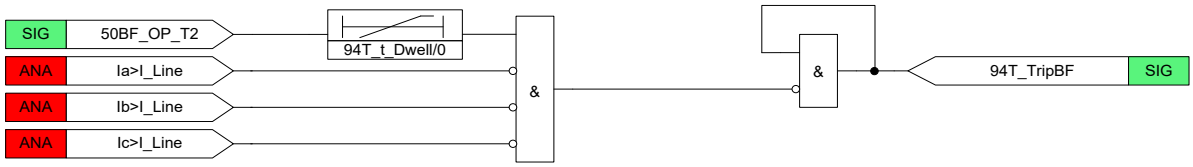


Figure 3.33.3 Logic Diagram of Tripping breaker failure

3.33.4 Settings

Table 3.33-3 94T Settings

NO	Name	Range	Unit	Step	Default	Description
1	94T_MPF_Blk_AR_Ena	0 or 1	-	1	0	Enabling/disabling auto-reclosing blocked when multi-phase fault happens 0: disable 1: enable

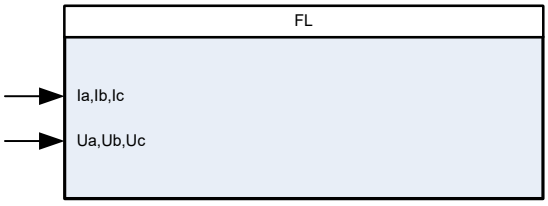
NO	Name	Range	Unit	Step	Default	Description
2	94T_3PF_Blk_AR_Ena	0 or 1	-	1	0	Enabling/disabling auto-reclosing blocked when three-phase fault happens 0: disable 1: enable
3	94T_Trp3P_Ena	0 or 1	-	1	0	Enabling/disabling three-phase tripping mode for any fault conditions 0: disable 1: enable
4	94T_T_Pulse	0.000~10.000	s	0.001	0.04	The duration of tripping pulse, empirical value is 0.04 The tripping contact shall drop off under conditions of no current or protection tripping element drop-off.
5	94T_T_PSFail	0.000~0.500	s	0.001	0.2	Secure 3-pole trip when phase selection failed

3.34 Fault Locator FL

3.34.1 Overview

The main objective of line protection and monitoring terminals is fast, selective and reliable operation for faults on a protected line section. Besides this, information on the distance to fault is very important for those involved in operation and maintenance. Reliable information on the fault location greatly decreases the downtime of the protected lines and increases the total availability of a power system.

3.34.1.1 Function Block



3.34.1.2 Signals

Table 3.34-1 FL Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input

3.34.2 Operation Principle

The fault location is an essential function to various line protection devices, after selecting faulty phase, it measures and indicates the distance to the fault with high accuracy. Thus, the fault can be quickly located for repairs. The calculation algorithm considers the effect of load currents, double-end infeed and additional fault resistance. Both double-end fault location and single-end fault location are available in line differential relay. The calculation equation is:

$$\text{Dist} = \frac{\text{Zcal}}{\text{Z1L}} * \text{Length}$$

Where:

Dist: The distance of fault location according to the Zcal (km).

Zcal: The impedance value calculated from the location of protection device to fault point.

Z1L: Positive-sequence impedance of the whole line, set by the setting Z1L.

Length: Total length of the whole line (km), set by the setting LineLength.

3.35 General function block

3.35.1 IDMT curves for over quantity protection and under quantity protection

The inverse-time modes of over quantity protection, the operation time depends on the momentary value of the quantity (such as 67P, 67N, 67I2, 51PVT, 51NVT,59P,59N): the higher the quantity, the faster the operation time.
The time duration of over quantity protection can be calculated according to the formula:

$$t = \left(\frac{K}{(\frac{G}{G_p})^{\alpha} - 1} + C \right) \times T_P$$

The inverse-time modes of under quantity protection, the operation time depends on the momentary value of the quantity (such as 27P): the lower the quantity, the faster the operation time.
The time duration of under quantity protection can be calculated according to the formula:

$$t = \left(\frac{K}{1 - (\frac{G}{G_p})^{\alpha}} + C \right) \times T_P$$

Where:

G_P : The Start setting value of the characterizing quantity.

T_P : Time multiplier setting.

α : A constant setting.

K: A constant setting.

C: A constant setting.

G: The measured value.

The user can select the operating characteristic from various inverse-time characteristic curves by setting Curve_Type, and parameters of available characteristics for selection are shown in the following table.

Table 3.35- 1 Inverse-time curve parameters

Curve Value	Curve Type	Curve Characteristic	K	α	C
1	ANSIE	ANSI Extremely Inverse	28.2	2	0.1217
2	ANSIV	ANSI Very Inverse	19.61	2	0.491
3	ANSIN	ANSI Normal Inverse	0.0086	0.02	0.0185
4	ANSIM	ANSI Moderately Inverse	0.0515	0.02	0.114
5	ANSIDefTime	ANSI Definite Time	×	×	×
6	ANSILTE	ANSI Long Time Extremely Inverse	64.07	2	0.25
7	ANSILTV	ANSI Long Time Very Inverse	28.55	2	0.712
8	ANSILT	ANSI Long Time Inverse	0.086	0.02	0.185
9	IECN	IEC Normal Inverse	0.14	0.02	0
10	IECV	IEC Very Inverse	13.5	1	0
11	IEC	IEC Inverse	0.14	0.02	0
12	IECE	IEC Extremely Inverse	80	2	0
13	IECST	IEC Short Time Inverse	0.05	0.04	0
14	IECLT	IEC Long Time Inverse	120	1	0
15	IECDefTime	IEC Definite Time	×	×	×
16	Resv	Reserve	×	×	×
17	UserDefine	User Programmable	-	-	-

If the Curve_Type= **ANSIDefTime** or **IECDefTime** or **Resv** , the operate time is Definite Time mode and the time duration can be calculated according to the formula:

$$t = C \times T_P$$

If the Curve_Type= **UserDefine**, the operate time is user Programmable. The timer model is determined by the parameter K, α, C, T_P setting value.

4 Supervision Functions

4.1 Overview

Though the protection system is in non-operating state under normal conditions, it is waiting for a power system fault to occur at any time and must operate for the fault without fail.

When the equipment is in energizing process, the equipment needs to be checked to ensure there are no errors. Therefore, the automatic supervision function, which checks the health of the protection system during startup and normal operation procedure, plays an important role.

The numerical relay based on the microprocessor operations has the capability for implementing this automatic supervision function of the protection system.

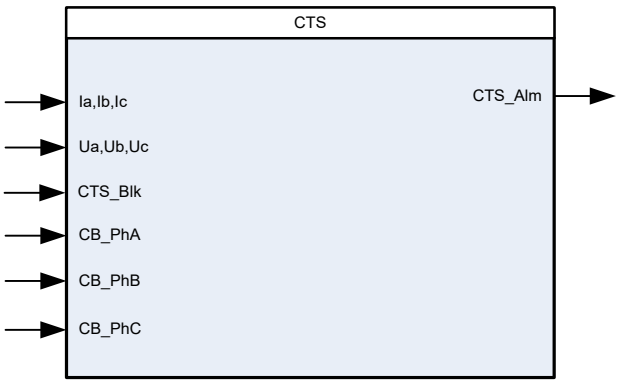
In case a fatal fault is detected during automatic supervision, the equipment will be blocked out. It means that this relay is out of service. Therefore you must re-energize the relay or even replace a module to make this relay back into service.

4.2 CT Circuit Supervision CTS

4.2.1 Overview

The purpose of the CT circuit supervision is to detect any abnormality on CT secondary circuit.

4.2.1.1 Function Block



4.2.1.2 Signals

Table 4.2-1 CTS Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	CTS_Blk	Blocking signal of CTS
4	CB_PhA	Normally closed contact of A-phase of circuit breaker
5	CB_PhB	Normally closed contact of B-phase of circuit breaker

NO.	Signal	Description
6	CB_PhC	Normally closed contact of C-phase of circuit breaker

Table 4.2-2 CTS Output Signals

NO.	Signal	Description
1	CTS_Alm	CT circuit fail alarm signal

4.2.2 Operation Principle

Under normal conditions, CT secondary signal is continuously supervised by detecting the zero-sequence current and voltage.

If zero-sequence current is larger than the minimum of 10%In and FD_ResCur_Str whereas zero-sequence voltage is less than 2V, and only one phase current is less than I_Line, an error in CT circuit is considered, the concerned protection functions are blocked and an alarm is issued with a time delay of 12s and drop off with a time delay of 12s after CT circuit is restored to normal condition.

4.2.3 Logic

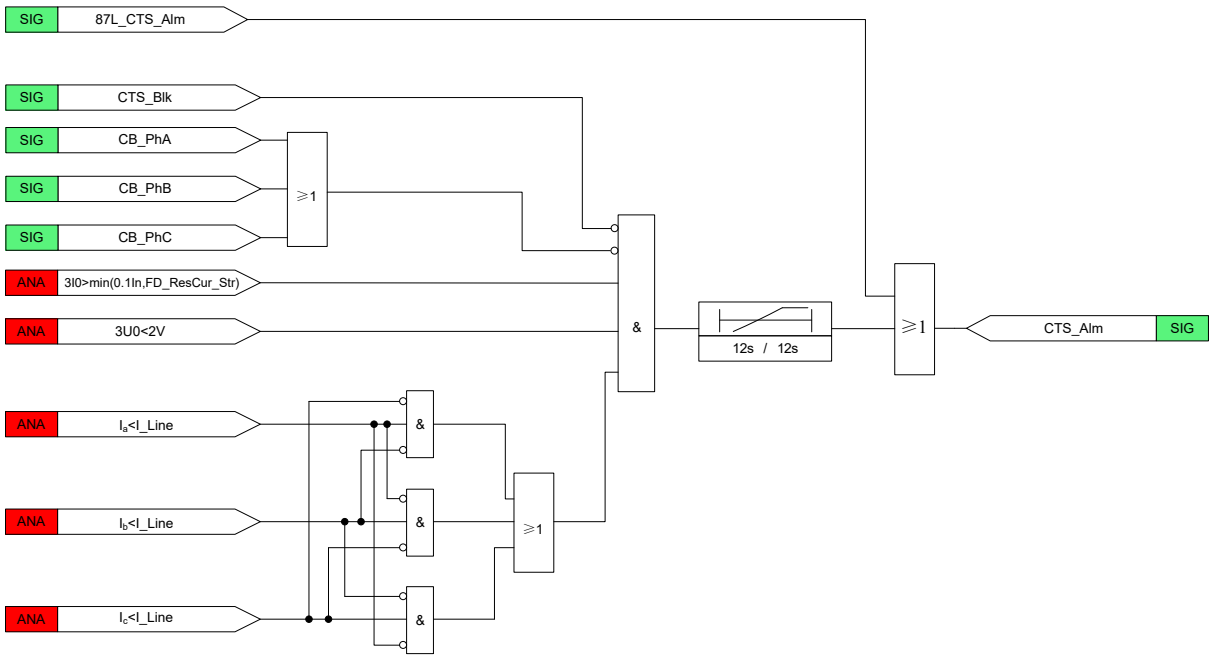


Figure 4.2.1 Logic Diagram of CTS

4.3 VT Circuit Supervision VTS

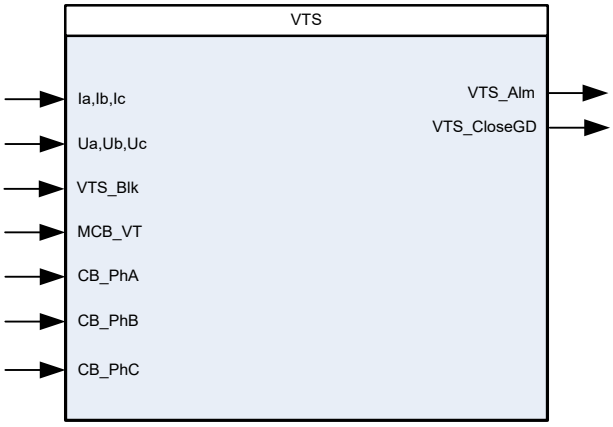
4.3.1 Overview

Some protection functions, such as distance protection, under-voltage protection and so on, will be influenced by VT circuit failure, these protection functions should be disabled when VT circuit fails. Therefore, it is necessary to supervise whether the VT circuit is normal.

VT circuit failure can be caused by many reasons, such as fuse blown due to short-circuit fault, poor contact of VT circuit, VT maintenance and so on. The device can detect them and issue an

alarm signal to block relevant protection functions.

4.3.1.1 Function Block



4.3.1.2 Signals

Table 4.3-1 VTS Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	Ua,Ub,Uc	Three-phase voltage input
3	VTS_Blk	Blocking signal of VTS
4	MCB_VT	Binary input for VT MCB auxiliary contact
5	CB_PhA	Normally closed contact of A-phase of circuit breaker
6	CB_PhB	Normally closed contact of B-phase of circuit breaker
7	CB_PhC	Normally closed contact of C-phase of circuit breaker

Table 4.3-2 VTS Output Signals

NO.	Signal	Description
1	VTS_Alm	VT circuit failure alarm signal
2	VTS_CloseGD	Permit closed ground disconnector signal

4.3.2 Operation Principle

4.3.2.1 Unbalanced VT Circuit Failure

A 3-phase measuring-voltage failure is detected if the following criteria are fulfilled simultaneously. If the criteria is fulfilled and no other blocking signals, VTS will output the alarm signal. When the voltage returns, the alarm signal drops out.

Operation criteria:

$$3U0 > VTS\_3U0$$

Where:

$3U0$: zero-sequence voltage

VTS_3U0 is the zero-sequence voltage setting of VT circuit supervision.

When the logic setting VTS_LineVT is set to “1”, voltage select line VT for protection calculation, there is another condition that needs to be met: three-phase of circuit breaker is closed or any phase current is more than I_Line.

4.3.2.2 Three-phase VT Circuit Failure

Operation criteria:

$$U1 < VTS\_U1$$

Where:

$U1$: positive -sequence voltage

VTS_U1 is the positive-sequence voltage setting of VT circuit supervision.

If the setting VTS_LineVT is set to 1, three phase VT circuit failure detection is only available if all the three phase circuit breaker is in closed position.

4.3.2.3 MCB auxiliary contact

VT (secondary circuit) MCB auxiliary contact as a binary input can be connected to the binary input circuit of the device. If MCB is open (i.e. [MCB_VT] is energized), the device will consider the VT circuit is not in a good condition and issues an alarm without a time delay. If the auxiliary contact is not connected to the device, VT circuit supervision will be issued with time delay as mentioned in previous paragraph.

4.3.2.4 Operation Time Delay

When the above abnormality is detected on VT circuit, an alarm will comes up with the time delay VTS_T_DPU and drop off with the time delay VTS_T_DDO after VT circuit restored to normal.

When VT is not connected to the device, the alarm will be not issued if the logic setting VTS_Out_VT is set to “1”. However, the alarm is still issued if the binary input [MCB_VT] is energized, no matter that the logic setting VTS_Out_VT is set as “1” or “0”.

4.3.2.5 Blocking of the Function

The alarm signal of VT circuit failure should not be issued when the following cases happen:

- Line VT is used as protection VT and the protected line is out of service.
- The fault detector element operates.
- Only current protection functions are enabled and VT is not connected to the device.

4.3.2.6 Permit closed gourd disconnector

VT (secondary circuit) MCB auxiliary contact as a binary input can be connected to the binary input circuit of the device.

When MCB is closed (i.e. [MCB_VT] is inactivated), the VT circuit is in a good condition, but if the voltage is about zero, it is safe to close the ground disconnector.

When three phase voltage is less than VTS_UV_CloseGD setting, and MCB is closed (i.e. [MCB_VT] is inactivated), the device will send VTS_CloseGD signals with a time delay of 500ms.

4.3.3 Logic

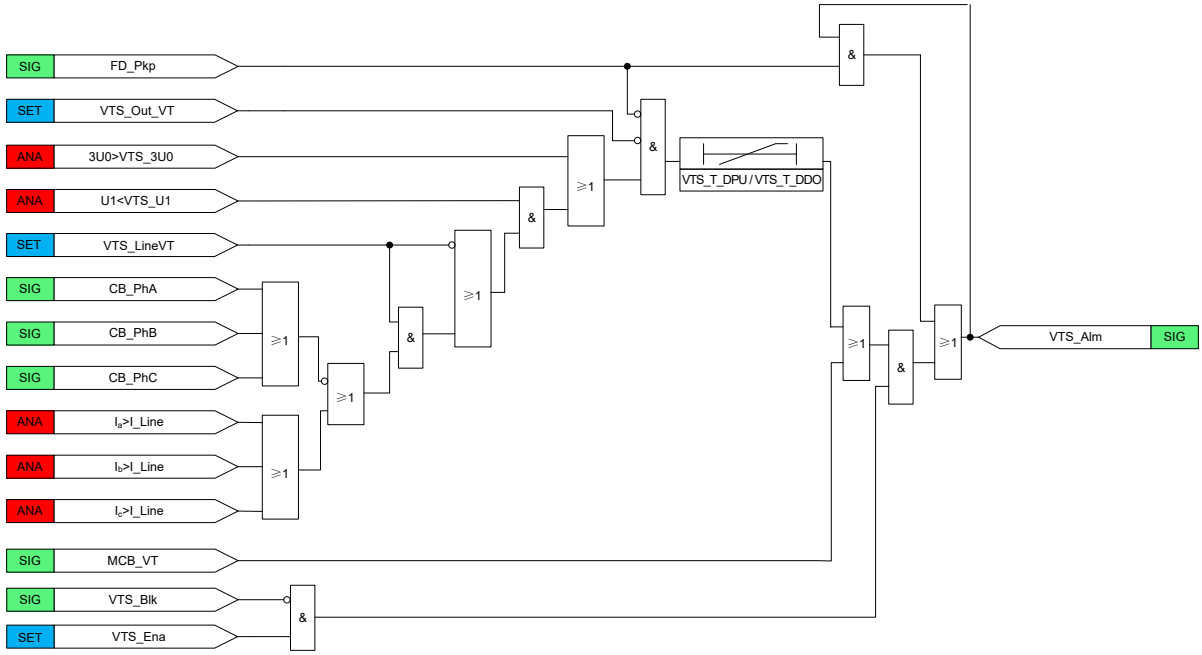


Figure 4.3.1 Logic Diagram of VTS

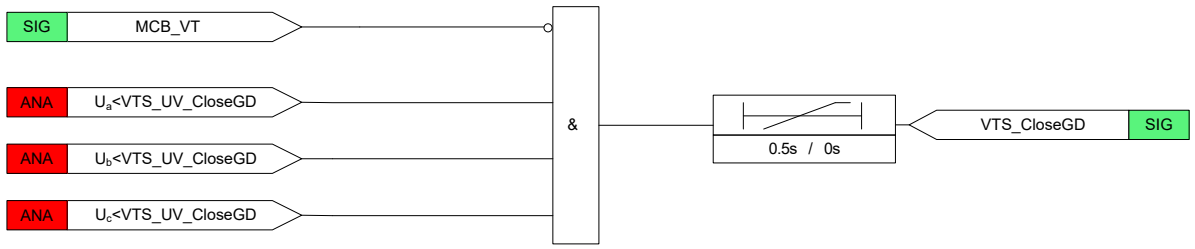


Figure 4.3.2 Logic Diagram of Permit closed gourd disconnector

4.3.4 Settings

Table 4.3-3 VTS Settings

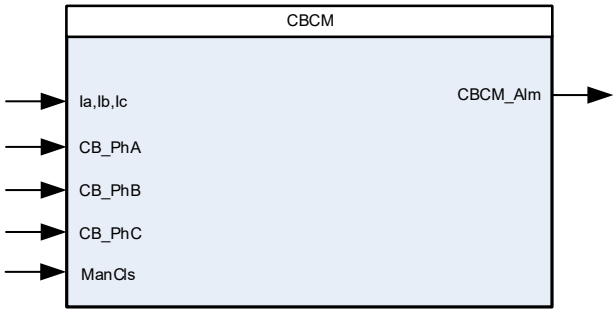
NO	Name	Range	Unit	Step	Default	Description
1	VTS_Out_VT	0 or 1	-	1	0	No voltage used for protection calculation 1: enable 0: disable In general, when VT is not connected to the device, this logic setting should be set as "1"
2	VTS_LineVT	0 or 1	-	1	0	Voltage selection for protection calculation from bus VT or line VT 1: line VT 0: bus VT
3	VTS_Ena	0 or 1	-	1	1	Alarm function of VT circuit supervision 1: enable 0: disable
4	VTS_T_DPU	0.2~100.000	s	0.001	1.3	Pickup time delay of VT circuit supervision
5	VTS_T_DDO	0.2~100.000	s	0.001	0.5	Dropoff time delay of VT circuit supervision
6	VTS_3U0	0.00~100.00	V	0.01	8	Zero-sequence voltage setting of VT circuit supervision
7	VTS_U1	0.00~100.00	V	0.01	6	Positive-sequence voltage setting of VT circuit supervision
8	VTS_UV_CloseGD	0.00~100.00	V	0.01	1.6	Voltage setting of VT circuit supervision for permit closed ground disconnector

4.4 CB Position Supervision CBCM

4.4.1 Overview

The status of circuit breaker (CB) position is applied for protection and control functions in this device, such as SOTF protection, auto-recloser, and VT circuit supervision, etc. The status of CB position can be applied as input signals for other features configured by user.

4.4.1.1 Function Block



4.4.1.2 Signals

Table 4.4-1 CBCM Input Signals

NO.	Signal	Description
1	Ia,Ib,Ic	Three-phase current input
2	CB_PhA	Normally closed contact of A-phase of circuit breaker
3	CB_PhB	Normally closed contact of B-phase of circuit breaker
4	CB_PhC	Normally closed contact of C-phase of circuit breaker
5	ManCls	Manual closing signal to initiate SOTF logic

Table 4.4-2 CBCM Output Signals

NO.	Signal	Description
1	CBCM_Alm	Circuit breaker position is abnormal

4.4.2 Operation Principle

The signal reflecting CB position is acquired via optocoupler with settable delay pickup and dropoff and forms digital signal used by protection functions. CB position can reflect the status of each phase by means of phase-segregated inputs.

In order to prevent that wrong status of CB position is input into the device via binary input, appropriate monitor method is used to check the rationality of the binary input. When the binary input of CB open position is detected, the status of CB position will be thought as incorrect and an alarm will be issued if current flow is detected in the line.

Together with the status of the circuit breaker and the information of external circuit, this function can be used to supervise control circuit of the circuit breaker.

This function includes manual closing and automatic closing, both of them will generate a signal keeping for the setting CBCM_T_SOTF to enable SOTF logic.

4.4.3 Logic

For single circuit breakers mode.

Figure 4.4.1 Logic diagram of circuit breaker position (phase A)

If there is any single phase tripping or breaker status Phx=1 (x can be A, B or C) and corresponding phase current is smaller than I_Line, then single pole open state is confirmed by the device.

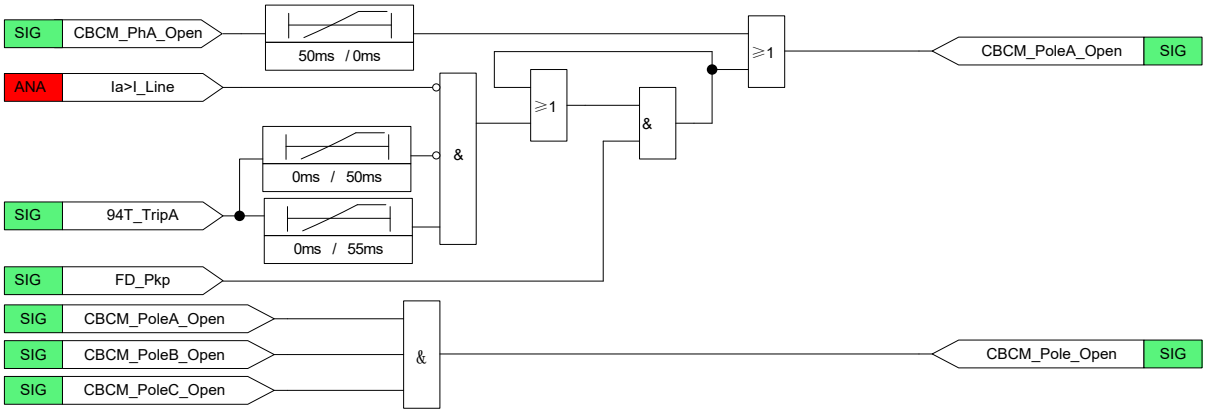


Figure 4.4.2 Logic diagram of pole open state (phase A)

Where:

94T_TripA, 94T_TripB and 94T_TripC are the tripping signals of the device.

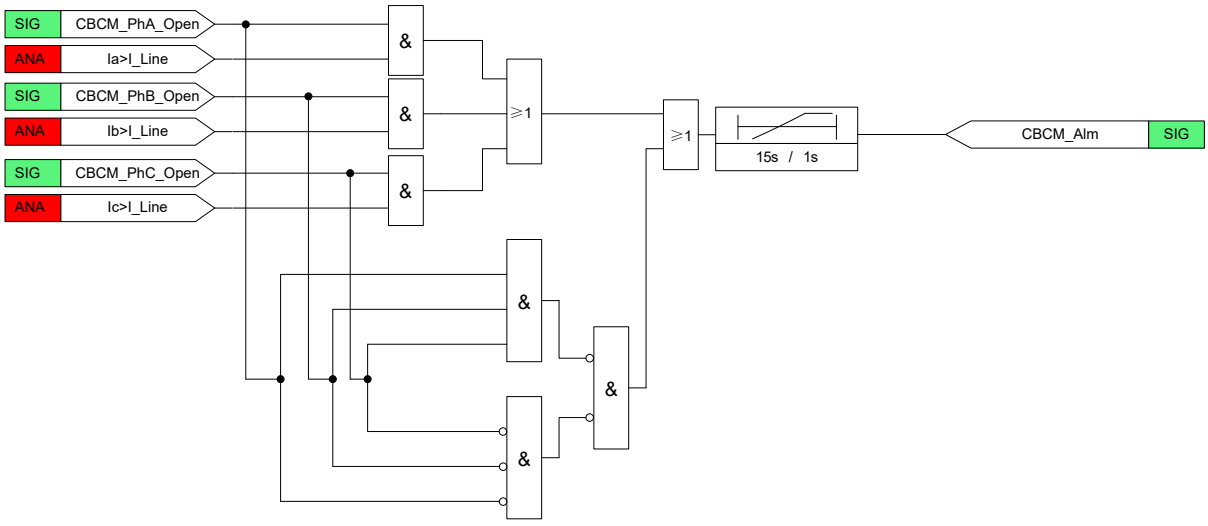


Figure 4.4.3 Logic diagram of CB position supervision

For accelerated tripping mode by manual closing signal, manual closing signal can be from circuit breaker position or external manual closing binary input.

When the device does not pick up, the circuit breakers in open position or external manual closing binary input energized will generate a signal, which will keep for the setting CBCM_T_SOTF and enable SOTF logic.

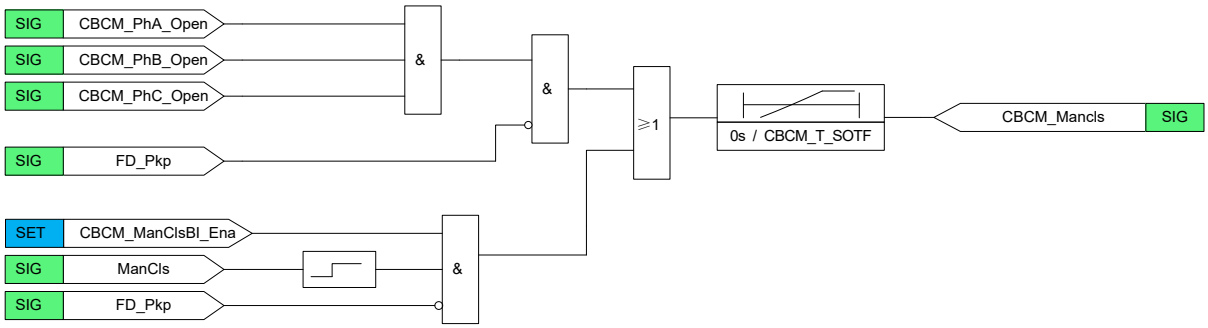


Figure 4.4.4 Logic diagram of manual closing signal

When the circuit breaker is in open position and corresponding phase current is greater than I_Line or the automatic reclosure is operated, then closing state is confirmed by the device. This signal will be kept for the setting CBCM_T_SOTF, which will enable SOTF logic.

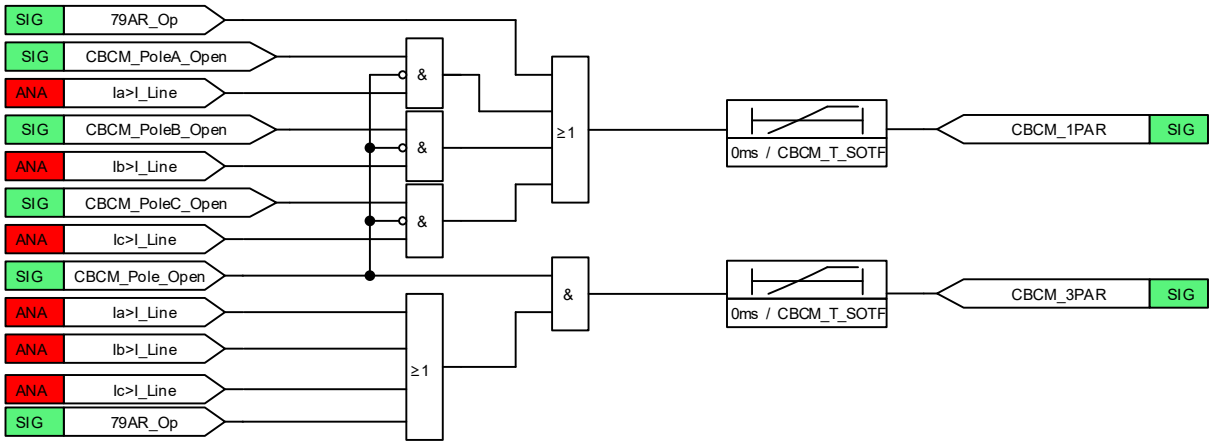


Figure 4.4.5 Logic diagram of automatic closing signal

4.4.4 Settings

Table 4.4-3 CBCM Settings

NO	Name	Range	Unit	Step	Default	Description
1	CBCM_ManClsBI_Ena	0 or 1	-	1	0	Enabling/disabling external manual closing signal binary input to initiate SOTF logic 0: disable 1: enable
2	CBCM_T_SOTF	0.000~10.000	s	0.001	0.2	Duration time for the SOTF keeping (shared by distance SOTF protection, and residual current SOTF protection)

4.5 Supervision Alarm and Block

The relay device has powerful real-time self-check capability. The device will automatically check

its own software and hardware running state during the process of operation. If there is any abnormal situation, the abnormal information will be displayed on the LCD, and the corresponding indicator and signal relay will issue prompt. Besides, these abnormal self-check and alarm signal can be uploaded to the SCADA through the IEC 61850 or IEC 60870-103 communication protocol.

Self-check scope of the device is as follows:

1. Self-check about the hardware:
   - Alarm signal of analog quantity circuit self-check
   - Alarm signal of BI circuit self-check
   - Alarm signal of BO circuit self-check
   - Alarm signal of storage self-check
   - Alarm signal of watchdog self-check
2. Self-check about the software and configuration
   - Alarm signal of software running state self-check
   - Alarm signal of configuration self-check
   - Alarm signal of internal communication self-check
3. Self-check about the external communication
   - Alarm signal of external communication self-check

If the relay device is in abnormal status, alarm signal will be issued. Some alarm signals will block the protection function, while some will not. The detailed information is shown as the following table.

Table 4.5-1 Alarm Signal and Block

Alarm Signal Name	Alarm Signal Description	Block Protection or Not
Kernel Comm Abn	Kernel Communication Abnormal	YES
Databus Comm Intr	Databus Communication Interrupt	YES
Databus Data Abn	Databus Data Abnormal	YES
LVDSIO Input Err	LVDSIO Input Error	YES
LVDSBus SelfChk Abn	LVDSBus SelfCheck Abnormal	YES
Comp SelfChk Abn	Component SelfCheck Abnormal	YES
RAM Scan Err	RAM Scan Error	YES
Sys Const SelfChk Abn	System Const SelfCheck Abnormal	YES
SelfChk Comp Port Err	SelfCheck Component Port Error	YES
SelfChk Comp Cfg Err	SelfCheck Component Configuration Error	YES
Setting SelfChk Err	Setting SelfCheck Error	YES
Setting CRC Err	Setting CRC Error	YES
Soft Sw SelfChk Err	Soft Switch SelfCheck Error	YES
Soft Sw CRC Err	Soft Switch CRC Error	YES
BO Cfg SelfChk Err	BO Configuration SelfCheck Error	YES
BO Cfg CRC Err	BO Configuration CRC Error	YES
Para SelfChk Err	Parameter SelfCheck Error	YES
Para CRC Err	Parameter CRC Error	YES
Prot Comp RAM Scan Err	Prot Component RAM Scan Error	YES
Databus Longtime Losing Pkg	Databus Longtime Losing Package	NO
Databus Wrong Pkg Alarm	Databus Wrong Package Alarm	NO

Alarm Signal Name	Alarm Signal Description	Block Protection or Not
A/D Sampling Err	A/D Sampling Error	NO
IRIG-B Syn Abn	IRIG-B Synchronization Abnormal	NO
Mana Bus Comm Intr	Mana Bus Comm Interrupt	NO
Setting Set CRC Err	Setting Set CRC Error	NO
Soft Sw Set CRC Err	Soft Switch Set CRC Error	NO
Para Set CRC Err	Parameter Set CRC Error	NO
Main Cfg Check Abn	Main Configuration Check Abnormal	NO
Cfg File Check Abn	Configuration File Check Abnormal	NO
Comp Cfg Check Err	Component Configuration Check Error	NO
WaveRcd Cfg File Abn	Wave Record Configuration File Abnormal	NO
WaveRcd File Abn	Wave Record File Abnormal	NO

5 Monitor & Control

5.1 Overview

Besides the protection and supervision functions, the relay provides some other auxiliary functions, such as protection and metering measurement quantities sampling, remote control, BI signaling, event recording and fault & disturbance recording etc. All these sub-functions are integrated components to fulfill the protection and control functions of the device.

5.2 Measurement

The general measurement quantities include both directly sampling and calculated quantities. These quantities are generally used for protection analyzing and metering calculation. All these quantities can be displayed in the local HMI or transmitted to the PRS IED Studio, SCADA or dispatching center through network communication.

Through the PRS IED Studio configuration tool, the measurement channels in the transformer module can be flexibly connected to any measurement quantity according to the designing requirements.

5.2.1 Protection Sampling

The protection sampling rate is 40 points per cycle. Different protection logic use different measurement quantities, including the RMS value, the phase angle, the frequency, the sequence components and so on. Some protection sampled values are displayed in HMI with 0.5s update rate.

5.2.2 Metering

The metering rate is 40 points per cycle. Different functions, such as controlling, monitoring and metering, use different measurement quantities, including the RMS value, the phase angle, the frequency, the harmonic content, the sequence components and so on. All these metering values are displayed in HMI with 0.5s update rate.

5.2.3 Settings

NO	Name	Range	Unit	Step	Default	Description
1	MC_Vol_Read_Zone	0.00-2.00	%	0.01	1	Mutation dead zone setting value of voltage
2	MC_Zero_Vol_Read_Zone	0.00-2.00	%	0.01	1	Zero dead zone setting value of voltage
3	MC_Cur_Read_Zone	0.00-2.00	%	0.01	1.5	Mutation dead zone setting value of current
4	MC_Zero_Cur_Read_Zone	0.00-2.00	%	0.01	1.5	Zero dead zone setting value of current

NO	Name	Range	Unit	Step	Default	Description
5	MC_DBI_Hold_T	0.000~60.000	s	0.001	0.02	Time period of debouncing
6	MC_Open0X_Pulse_T	0.001~60.000	s	0.001	0.2	remote-control trip pulse width
7	MC_Close0X_Pulse_T	0.001~60.000	s	0.001	0.2	remote-control close pulse width
8	MC_Sel_Max_T	1.000~60.000	s	0.001	30	Time period of selection operation
9	MC_Exe_Max_T	1.000~60.000	s	0.001	30	Time period of operate operation

5.3 Apparatus Control

The apparatus control is a combination of functions which continuously supervise and control the circuit breakers, switches and earthing switches within a bay. The selection and operation command to control an apparatus is given after the evaluation of other functions' conditions such as interlocking, operator place selection and the external or internal blocking.

The commands to an apparatus can be initiated from the local self-customized BI, the station HMI or the dispatching center. The local control self-customized BI can be configured on the PRS IED Studio. The control operation can be started by the activation of the corresponding BI signal. The remote control command can be remotely dispatched through the network communication like IEC61850 or DNP. Before executing a remote control command, it is necessary to turn the Local/Remote control switch to the “Remote” position.

The output relays in the BO module can be configured as output contacts so as to close or trip the apparatus. Each control output can be control with an interlock module (which can be configured through the PRS IED Studio) if the corresponding interlock logic setting (see Section 7.4.3) is set to activation.

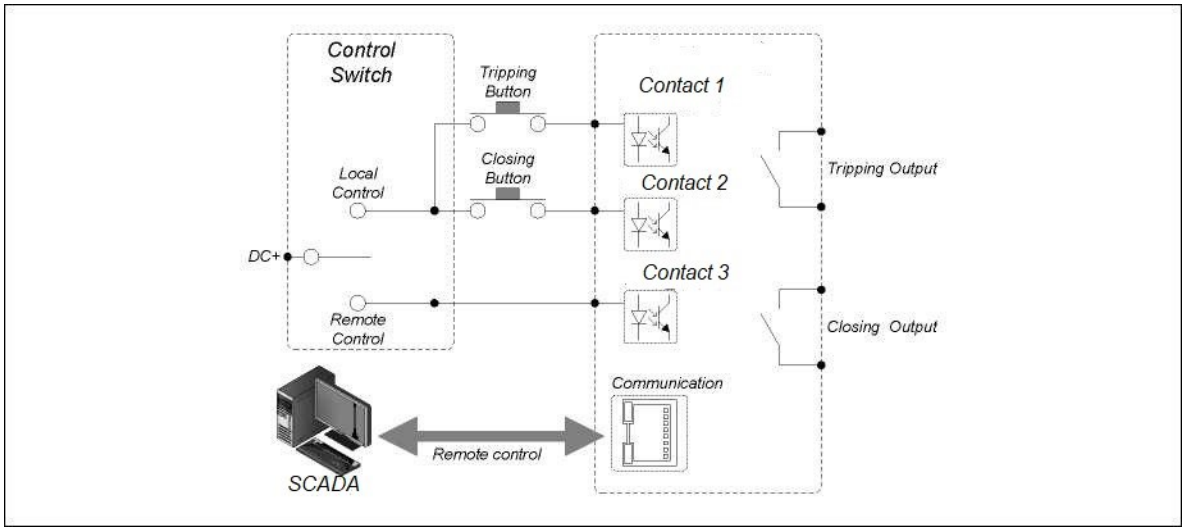


Figure 5.3.1 Demonstration Diagram of The Control Function

5.4 Signaling

All inputs of the protection hardware unit are configurable via PRS IED Studio software. Common binary inputs can be configured for the following purposes:

- Bay primary equipment state acquisition, such as circuit breaker position, insulator position. These signals can be sent to the substation monitoring system or dispatching automation system through the protection device.
- Used for BI condition of the protection logic to achieve the block or release of inner logic.
- Used to monitor the health condition of primary equipment such as SF6 low pressure alarm and transformer high oil temperature. These signals can be used as function input of protection logic, and also can be sent to substation monitoring system or dispatching automation system as separate alarm signals. Achieve remote monitoring.
- Transformer tap position input

All hardware input debouncing time can be set separately. Debouncing time setting can be done through the LCD or PRS IED Studio software.

5.5 Event Records

5.5.1 Overview

The protective device record events in an event log. This allows you to establish the sequence of events that led up to a particular situation. For example, a change in a digital input signal or protection element output signal would cause an event record to be created and stored in the event log. This could be used to analyze how a particular power system condition was caused. These events are stored in the IED's non-volatile memory. Each event is time tagged. The time resolution is 1ms.

The event records can be displayed on an IED's front panel but it is easier to view them through the configuration software. This can extract the events log from the device and store it as a file for analysis on a PC.

The event records are detailed in the EVENTS column. The first event (0) is always the latest event. After selecting the required event, you can scroll through the menus to obtain further details.

5.5.2 Fault Record Events (FaultEvents)

An event record is created for every fault the IED detects. This is also known as a fault record.

The IED contains a separate register containing the latest fault records. This provides a convenient way of viewing the latest fault records and saves searching through the event log. You access these fault records using the Select Fault setting, where fault number 0 is the earliest fault.

The event is logged as soon as the fault recorder stops. The time stamp assigned to the fault corresponds to the start of the fault. The fault operating relative time is the subtraction between the fault stop moment and the fault start moment, and the time is in milliseconds.

The IED can store 512 latest time tagged fault record events.

5.5.3 Alarm Record Events

The IED monitors itself on power up and continually thereafter. If it notices any problems, it will register an alarm event. The alarm records include protection alarm records and device self-check records.

5.5.3.1 Protection Alarm Record(WarmingRecords)

The IED provides self-check alarm information that reflects the communication status between devices, such as carrier channel abnormal, fiber channel abnormal, SV communication abnormal, GOOSE communication abnormal, etc.

The IED provides self-check alarm information that reflects the external circuit such as analog error information (CT disconnection, PT disconnection, etc.) and abnormal information of primary switch state (abnormal trip position, trip signal long time input, etc.)

The IED can store 512 latest time tagged alarm records.

5.5.3.2 Device self-check record (ChkRecords)

- **Hardware self-check record**

The IED provide hardware health condition self-check alarm, such as analog sampling circuit abnormal self-check, memory status self-check alarm.

- **Software self-check record**

The IED provides software operation status self-check alarm records, such as setting error, parameter verification error and the like.

- **Configuration file self-check record**

The IED provides self-check records that reflect the status of the device configuration file, such as configuration file error, configuration file change, etc.

The IED can store 128 latest time tagged alarm records

5.5.4 Device Record

5.5.4.1 Remote Control Record(YKRecords)

Device control objects include circuit breakers, disconnectors, earthing disconnectors close and open, reset signal, transformer tap adjustment, etc., when the device receives the remote control command, the device will generate control operation record. The remote control contents contain the command source, command time, operation result, failure reason, etc.

The IED can store 128 latest time tagged control records.

5.5.4.2 Device Operation Record(OptRecords)

The operation record includes the time when the event was generated, the operation object, the content of the operation, and the description of the operation result.

The IED can store 128 latest time tagged device operation records.

5.5.4.3 Device Running Record(RunRecords)

The running record is the device power-on, power-off record.

The IED can store 128 latest time tagged device running records.

5.5.5 Sequence of Event(SoeRecords)

The IED has event sequence record (SOE) function:

- When the state quantity input signal is from a hard contact, the time tag of the state quantity is marked by the device, and the time is defined before debouncing.
- When the state quantity input is GOOSE signal, the time tag of the state quantity adopts the external input source signal time tag, and GOOSE signal acquisition has no debouncing time.

The IED can store 2000 latest time tagged SOE records.

5.6 Fault and Disturbance Recording

This IED provides the fault and disturbance recorder for recording the sampled values of the fault and disturbance wave when a fault is occurred in the power system, which can be triggered by pickup signals, trip signals and configurable binary signal. The fault recorder feature allows you to record selected current and voltage inputs to the protection elements, together with selected digital signals.

The integral fault recorder has an area of memory specifically set aside for storing disturbance records. The fault memory of the device is automatically updated with every recording. When the fault memory is filled completely, the oldest records are overwritten automatically. Thus, the latest records are always stored safely. The maximum number of time tagged records is 36, contain16 fault disturbance waves, 16 start disturbance waves and 4 manual disturbance waves.

Each fault waveform includes the wave recording data both before and after the fault. Each trigger element operation will extend the wave recording time, until the appointed time delay is over after the trigger element restores, or until the maximum number of wave recording points is reached.

5.6.1 Wave Recording File Format

The wave recording file adopts COMTRADE common format, complying with the requirements of IEC 60255-24. Each COMTRADE record has up to four files associated with it, namely: a title file (xxxxxxxx.HDR), a configuration file (xxxxxxxx.CFG), a data file (xxxxxxxx.DAT), and an information file (xxxxxxxx.INF), where information file is optional file. The wave recording files can be extracted communication with relay.

5.6.2 Fault Wave File

For each fault wave file, the following items are included:

1. Sequence number

Each operation will be recorded with a sequence number in the record and displayed on LCD screen.

2. Date and time of fault occurrence

The date and time is recorded when a system fault is detected. Time & date stamped by relay real time clock. The time resolution is 1ms.

3. Relative operating time

An operating time (not including the operating time of output relays) is recorded in the record. The time resolution is 1ms.

4. Fault information

Including faulty phase, fault location and protection elements.

5.6.3 Waveform Recording Duration

A fault waveform contains all analog and digital quantities related to IED such as currents, voltages, differential current, alarm elements, and binary inputs and etc.

The overall duration of a single fault recording comprises the total duration of the recording criterion, the pre-trigger time and the post-trigger time. With the fault recording parameter, these components can be individually set. The pre-trigger waveform recorded duration is configured via the setting [RecT_PreFault]. The waveform recorded duration after the fault disappears is configured via the setting [RecT_PostFault]. The maximum waveform recorded duration is configured via the setting [MaxT_OneRec].

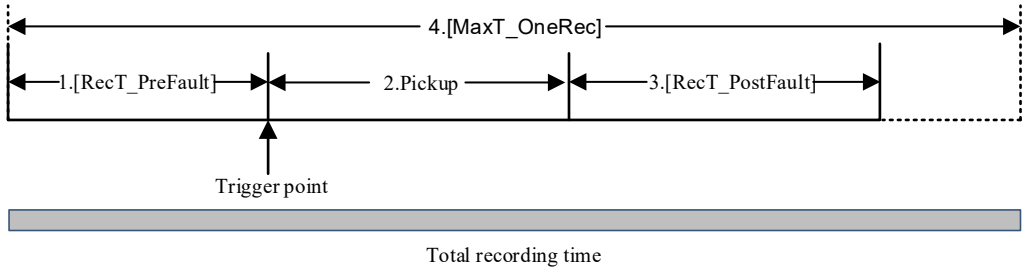


Figure5.6.1 Recording time diagram

1. Pre-trigger recording time

Use the setting [RecT_PreFault] to set this time.

2. Pickup recording time

The pickup recording time cannot be set. It continues as long as any valid trigger condition, binary or analog, persists.

3. Post-fault recording time

The recording time begins after all activated triggers are reset. Use the setting [RecT_PostFault] to set this time.

4.Maximum recording time

Use the setting [MaxT_OneRec] to set this time. If the summation of wave recording duration is

larger than maximum recording time, the one recording time shall be equal to the setting [MaxT_OneRec].

Table 5.6-1 Recording Time Settings

No.	Name	Range	Unit	Step	Default	Description
1	RecT_PreFault	60~1000	ms	1	100	Pre-trigger recording time.
2	RecT_PostFault	60~1000	ms	1	100	Post-fault recording time.
3	MaxT_OneRec	1000~8000	ms	1	8000	Maximum recording time

5.6.4 Fault Wave Recording

You can select any of the IED's analogue inputs as analogue channels to be recorded. You can also map any of the opto-inputs and output contacts to the digital channels. In addition, you may also map a number of DDB signals such as Starts and LEDs to digital channels.

The path to the configuration tool:

[IED]->[Const]->[WAVEANA]/[WAVEKI]/[WAVEKO]->[Ana Channel]/[KI Channel]/[KO Channel].

5.6.5 Logic Event Recording(EventRecords)

When there is wave recording, the relay will record all of the process signals in logic diagram by EventRecords, which configured by manufacture or super (If the permission setting is Show, it means super configuration is available).
The path to the configuration tool: [IED]->[Const]->[LNDOSOECFG].

6 Hardware

6.1 Overview

The modular design structure of this relay enables a qualified commissioning technician to easily check and locate the damaged hardware modular, so as to eliminate the fault in the very first time. The hinged front panel allows easy access to the HMI modules and the back-plugging design makes it easy to upgrade, maintain or replace any module.

There are several types of hardware modules in this relay, which play different roles in the practical application. The specific modules can be configured flexibly according to the practical engineering demands.

The overall hardware designing frame of this relay is shown as below.

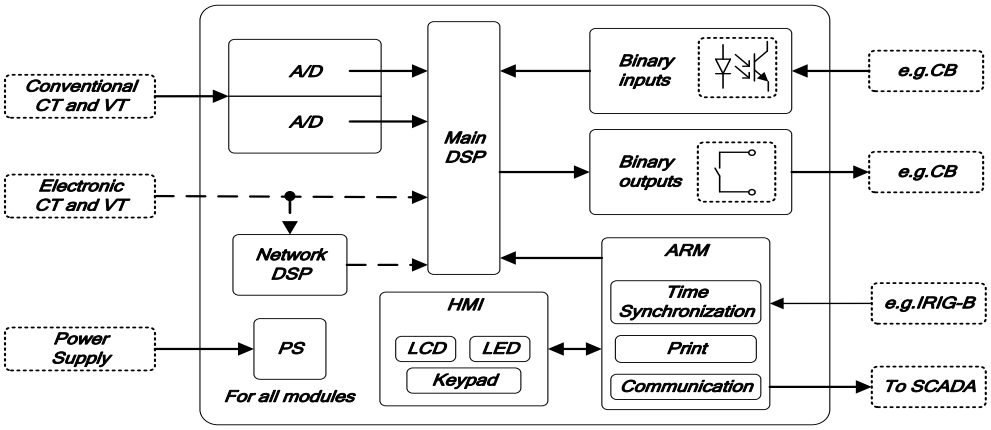


Figure 6.1.1 Hardware Frame of This Relay

The following figures show the front panel and the rear panel of 1/2 19" case.

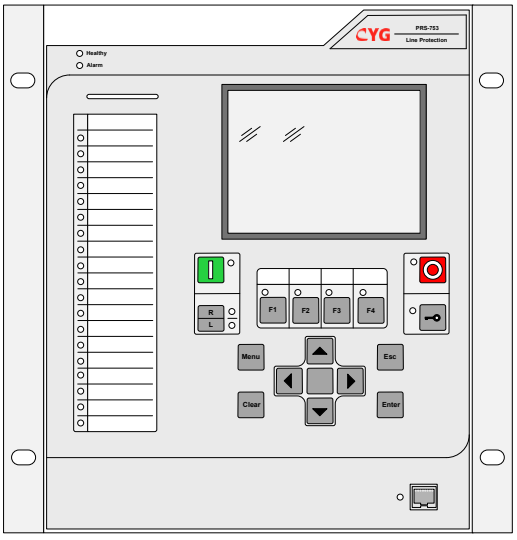


Figure 6.1.2 Front Panel of 1/2 19" Case

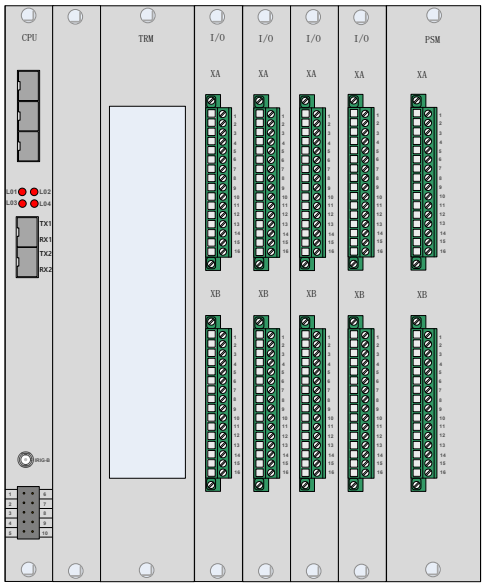


Figure 6.1.3 Rear Panel of 1/2 19" Case (Optical Ethernet)

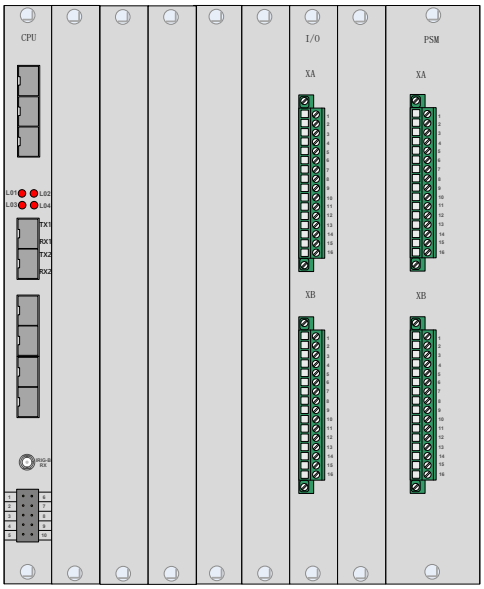


Figure 6.1.4 Rear Panel of 1/2 19" Case (Process Level)

The following figures show the front panel and the rear panel of 1/1 19" case.

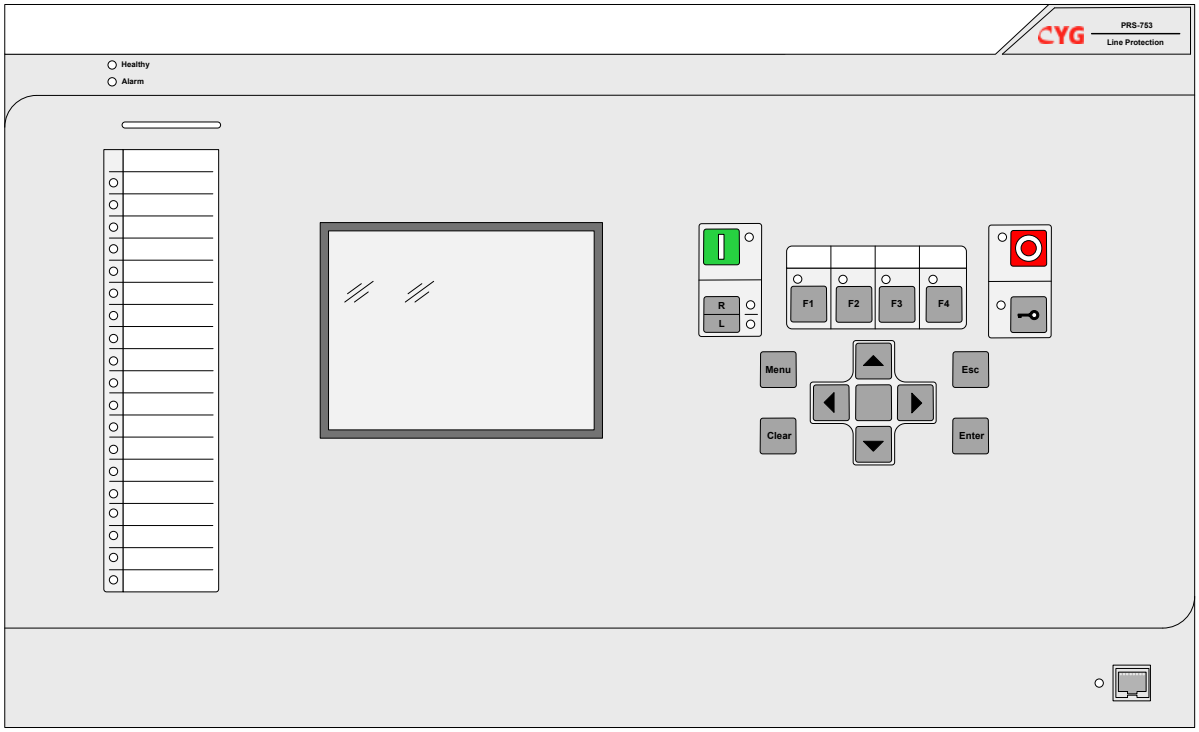


Figure 6.1.5 Front Panel of 1/1 19" Case

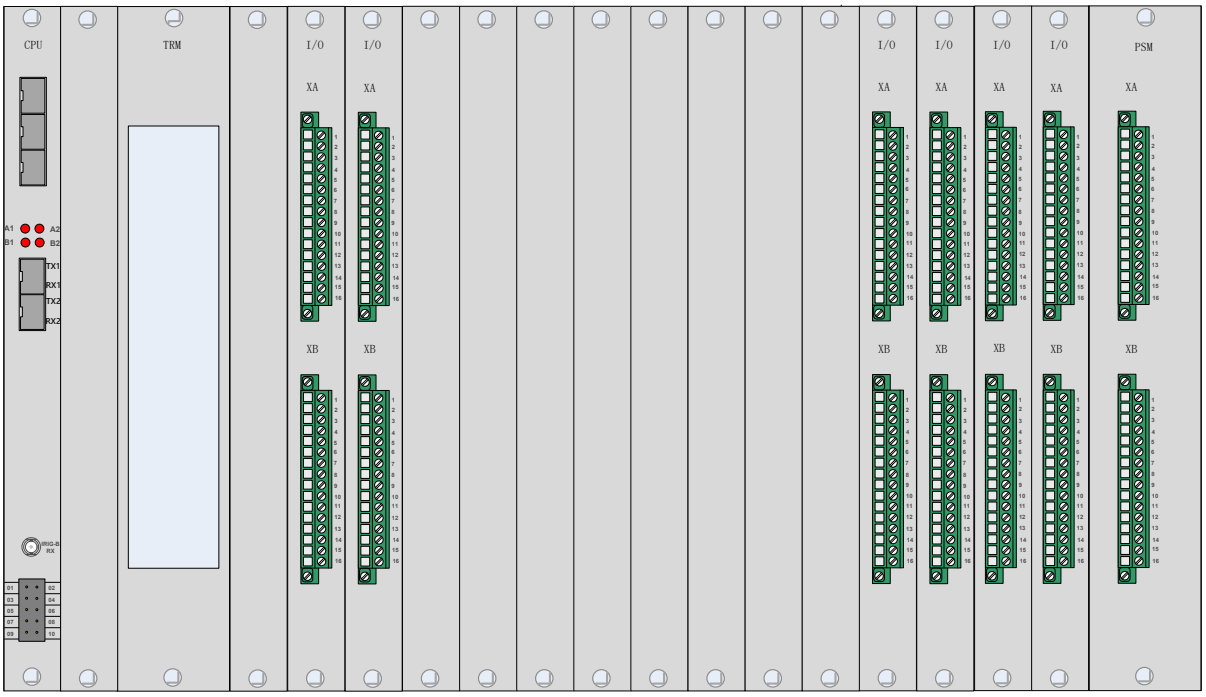


Figure 6.1.6 Rear Panel of 1/1 19" Case (Optical Ethernet)

NOTICE!

The hardware module configuration in the above figure is only for demonstrating one kind of typical configuration. Most often, the configuration has to be modified in most of

the project. The hardware module configuration of a practical engineering should be modified based on the practical designing requirement.

6.2 Hardware Module

The PRS-753 is comprised of randomly coordinated modules, except that a few particular modules, e.g., PWR module, CPU module and HMI module, cannot be replaced in the whole device. The other modules, including TF (current or voltage transformer) module and IO (input and output) module, can be flexibly configured and then placed in the remained slots. The TF module includes AC current transformer, AC voltage transformer, DC current transformer and etc. The IO (input and output) module includes binary input, tripping output, signal output and etc.

Table 6.2-1 Module Configuration

No.	ID	Module Description	Remark
1	SR7601	Power supply module (PWR module)	standard
2	SR7260	Protection calculation module (CPU module)	standard
3	SR7153	Current/voltage transformer module (TF module)	standard
4	SR7330	Binary input module (BI module)	standard
5	SR7300	Binary output module (BO module)	standard
6	SR7301	Binary output module (BO module)	standard
7	SR7310	Binary input/output module (IO module)	standard

6.3 Human Machine Interface Module

The human machine interface (HMI) module is installed behind the front panel of this device. It contains an LCD screen to modify the protection settings and system parameters and display information of this device, including the analogue quantities, the running status and event lists.

The menus are showed as tree structured, which facilitates the users to enter any specific menu. After entering the menu, the big LCD show all the relevant information in one screen, making it easier to get all the information.

6.4 Power Supply Module

The power supply module contains a small voltage converter with enough electrical insulation between the converter and the input/output terminals. A wide range input voltage is provided due to the sophisticated circuit design. The output voltage from the voltage converter are continuously monitored to ensure the stability and safety.

The power supply module provides 10 binary outputs, some dry contacts, which conduct the signal functions showing the operating conditions (device error) or tripping and closing commands

(protection, auto-recloser or remote control). The specific function is performed by setting the relevant settings and wiring the external copper cable.

Except for the Dev_Err Cls and Dev_Err Open output contacts (fixed as indication output contacts), all the other binary inputs or outputs can be visually and flexibly configured through the PRS IED Studio configuration tool, which determine what information do they transmit between the CPU module and PWR module.

The frame of all the power supply module terminal are shown below.

PWR			
01	POW(+)	TRIP06 Open	17
02	POW(-)	SIGN07 Common	18
03	Dev_Err Common	SIGN07 Open	19
04	Dev_Err Cls	SIGN07 Cls	20
05	Dev_Err Open	SIGN08 Common	21
06	TRIP01 Common	SIGN08 Open	22
07	TRIP01 Open	SIGN08 Cls	23
08	TRIP02 Common	SIGN09 Common	24
09	TRIP02 Open	SIGN09 Open	25
10	TRIP03 Common	SIGN09 Cls	26
11	TRIP03 Open		27
12	TRIP04 Common		28
13	TRIP04 Open		29
14	TRIP05 Common		30
15	TRIP05 Open		31
16	TRIP06 Common		32

Figure 6.4.1 Frame of the Power Supply Module Terminals

The specific terminal definition of the connector is described as below.

Table 6.4-1 Terminal Definition and Description of PWR Module

Name	Description
PWR+	Positive input of power supply for the device.
PWR-	Negative input of power supply for the device.
Dev_Err Common	Device abnormality alarm common terminal.

Name	Description
Dev_Err Cls	Device abnormality alarm normal close terminal.
Dev_Err Open	Device abnormality alarm normal open terminal.
TRIP01-06	The No.1 -6 programmable tripping or closing binary output. BOi (i=1-6) Open is the normal open binary output.
SIGN07-09	The No.7 -9 programmable signal binary output. BOi (i=7-9) Open is the normal open binary output, BOi (i=7-9) Cls is the normal close binary output.

6.5 Main CPU Module

The main CPU module, containing powerful microchip processors and some necessary electronic accessories, is the core part of this relay. This powerful processor executes all the functions of the relay and conduct the commands, including the protection logic, the control function and the internal and external information interfacing functions.

A high-accuracy crystal oscillator is installed on the module as well, ensuring the relay to operate exactly based on the accurate current time.

The main functions of the main CPU module include as below:

- AD conversion

  The module consists of a 16-bit high-accuracy AD converter which converters the sampling analog quantities to digital signals channel by channel. After the quick converter, all the digital signals are transmitted to microchip processors for latter application.

- Sampling information processing

  The values of each sampling point will be stored and then sent to different processing module for different function, including display, calculation, communication.

  The values of each binary IO contacts will also be stored and then sent to different processing module for different function, including display, calculation, communication.

- Protection, measuring and metering quantities calculation

  The CPU module can calculate all the relevant quantities (zero sequence current and voltage, negative sequence current and voltage, harmonic quantities of up to 13^{th}) on the basis of the directly sampling quantities (phase-to-earth voltages and currents, phase-to-phase voltages and currents) and binary inputs. After the calculation, all the quantities are sent to the protection function module or control module to decide whether the relevant dry contacts trip or close.

- Communication management

  The CPU module can effectively execute all communication procedures parallel and reliably interface coded messages through the selected communication interfaces. These interfaces are usually used to communicate with a SCADA or a Station Gateway through a switcher. The CPU module is also responsible for information exchanging with the HMI module. If any monitoring condition changes or any event occurs (SOE, protection tripping event, device

abnormality), this module will send out the relevant event information to all relevant receivers, so as to ensure a first time alarm to notice the users.

- Auxiliary calculations

  Besides all the quantities mentioned above, the CPU module can also calculate the metering values, such as active power, reactive power and power factor, etc., to provide overall monitoring information. All these quantities can be sent to a SCADA or a Station Gateway through a switcher.

- Time Synchronization

  The module provides an interface to receive time synchronized signals from external clock synchronization source. This module also has a local crystal oscillator to maintain the internal time accuracy when outside synchronization source breaks down. The synchronization mode includes PPS (pulse per second) mode and IRIG-B mode. Basing on the outside timing message (from SCADA or Station Gateway) or the PPS signal or the IRIG-B signal, this module can adjust its time within the timing accuracy.

The frame of the CPU module terminal is described as below. The detailed configuration is up to the project requirements.

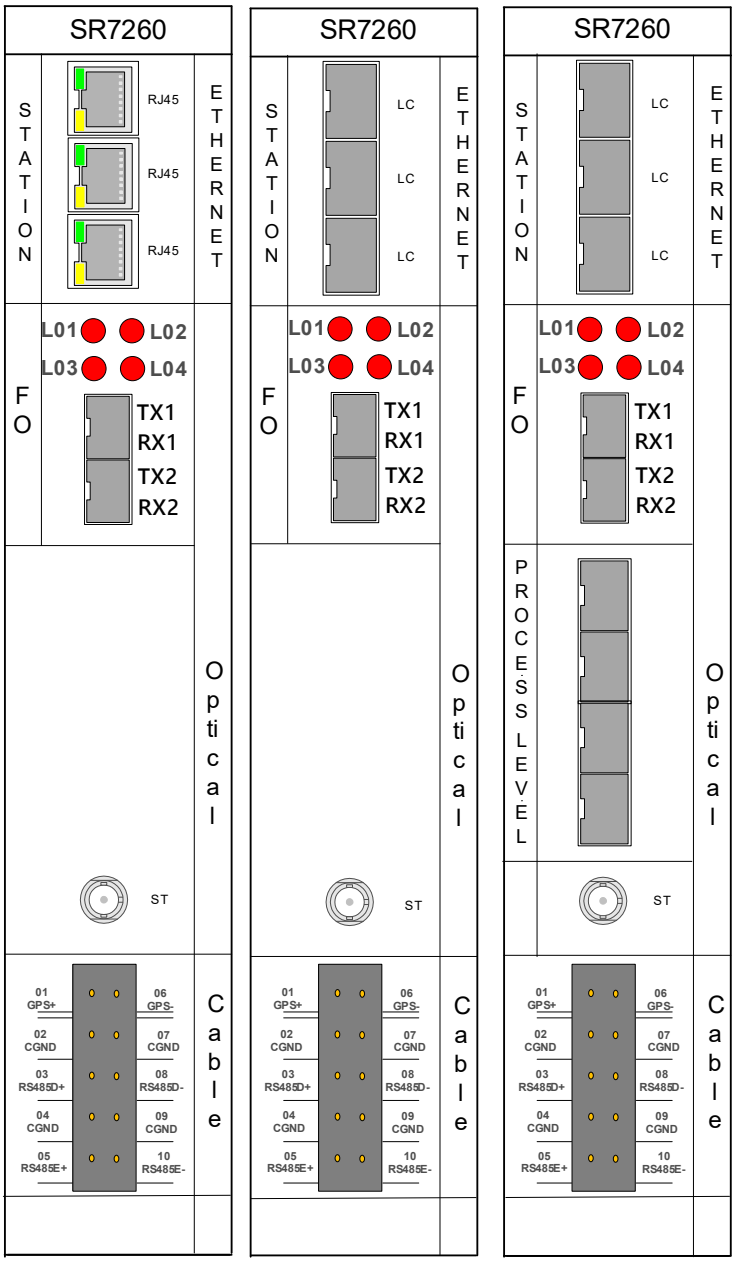


Figure 6.5.1 The frame of the CPU module terminal

NOTICE!

The third in the above picture is only used for digital devices.

6.6 Transformer Module

The transformer module can decrease the high input analog values to relevant low output analog values as to the small transformer ratio, acting as an effective isolation between the relay and the power system. The low output analog values, within the range of the AD module after the conversion, are sent to the AD module for further processing. A low pass filter circuit is used to reduce the noise of each analog channel.

The frame of two transformer modules of different specifications are shown below. The first one

consists of 4 voltage channels and 8 current channels. The second one consists of 8 voltage channels and 4 current channels.

In the first case, there are two applications. Firstly, for one CT group input, three phase currents (Ia1, Ib1 and Ic1) are input to AI module separately, another group three phase currents (Ia2, Ib2 and Ic2) should be disconnected. Secondly, for two circuit breakers configuration with two CT groups input, three phase currents corresponding to CB1 and CB2 respectively (Ia1, Ib1, Ic1 and Ia2, Ib2, Ic2) are input to AI module.

Three phase voltages (Ua, Ub, and Uc) for protection calculation and one synchronous voltage are input to the two types of AI module above. The synchronous voltage could be any phase-to-ground voltage or phase-to-phase voltage.

In the second case, when three phase voltage used for protection calculation comes from bus side, for double bus arrangement with two bus VT groups input, three phase voltages corresponding to bus 1 and bus 2 respectively (Ua1, Ub1, Uc1 and Ua2, Ub2, Uc2) are input to AI module. One synchronous voltage (Us1) is input to AI module, another group synchronous voltage (Us2) should be disconnected.

When three phase voltage used for protection calculation comes from line side, for double bus arrangement with two bus VT groups input, three phase voltages (Ua1, Ub1, Uc1) are input to AI module, another group three phase currents (Ua2, Ub2 and Uc2) should be disconnected. One synchronous voltage corresponding to bus 1 and bus 2 respectively (Us1 and Us2) are input to AI module.

The device can automatically switch protection calculation and synchronous voltage according to auxiliary contact of CB position or DS position.

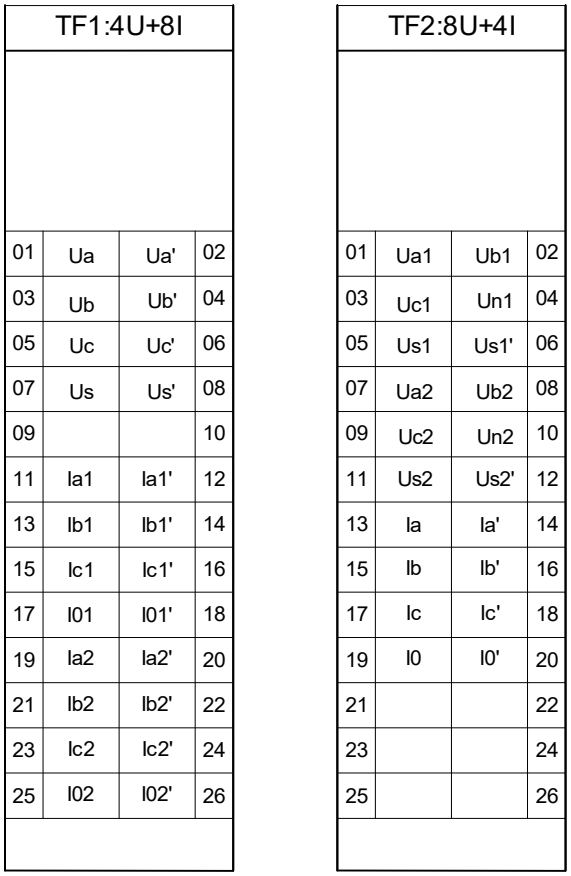


Figure 6.6.1 Transformer Module of Three Different Specifications

DANGER!

NEVER allow the secondary side of the current transformer (CT) to be opened while the primary apparatus is energized. The opened CT secondary circuit will produce an extremely high voltage and high heat. Although the current terminal will be automatically short circuited when it is plugged out, the safety precaution should be obeyed in order to prevent severe personal injury, person death or considerable equipment damage.

The terminal definition of the connector is described in the below diagram.

Table 6.6-1 Terminal Definition and Description of TF Module 1

Name	Description
Ua	The three phase voltage inputs.
Ua’	
Ub	
Ub’	
Uc	
Uc’	
Us	The synchronous voltage inputs.
Us’	

Name	Description
Ia1	The three phase current inputs.
Ia1’	
Ib1	
Ib1’	
Ic1	
Ic1’	
Io1	The zero sequence current inputs.
Io1’	
Ia2	The three phase current inputs.
Ia2’	
Ib2	
Ib2’	
Ic2	
Ic2’	
Io2	The zero sequence current inputs.
Io2’	

Table 6.6-2 Terminal Definition and Description of TF Module 2

Name	Description
Ua1	The three phase voltage inputs.
Ub1	
Uc1	
Un1	
Us1	The synchronous voltage input.
Us1’	
Ua2	The three phase voltage inputs.
Ub2	
Uc2	
Un2	
Us2	The synchronous voltage input.
Us2’	
Ia	The three phase current inputs.
Ia’	
Ib	
Ib’	
Ic	
Ic’	
Io	The zero sequence current inputs.
Io’	

6.7 Binary Input Module

The BI module contains 18 binary inputs, the optical isolated input terminals, which can perform different monitoring functions, such as detecting the breaker and switch positions of the corresponding bay. All the BI terminals can be used as general purpose binary inputs or special purpose (protection function or control function) binary inputs. For example, the general purpose binary inputs can be used to indicate the status (0 for normal condition and 1 for abnormal condition) of a certain apparatus. For another example, the special purpose binary inputs can be used to acting as the blocking or start signal for a certain protection function.

All the binary inputs can be visually and flexibly configured through the PRS IED Studio configuration tool, which determine what information do they transmit between the CPU module and BI module.

The frame of the BI module terminal is described as below.

INPUT			
01	BI01+	BI10+	17
02	BI02+	BI11+	18
03	BI01~02 Common-	BI10~11 Common-	19
04	BI03+	BI12+	20
05	BI04+	BI13+	21
06	BI03~04 Common-	BI12~13 Common-	22
07	BI05+	BI14+	23
08	BI05-	BI14-	24
09	BI06+	BI15+	25
10	BI06-	BI15-	26
11	BI07+	BI16+	27
12	BI07-	BI16-	28
13	BI08+	BI17+	29
14	BI08-	BI17-	30
15	BI09+	BI18+	31
16	BI09-	BI18-	32

Figure 6.7.1 Frame of Input Terminal

Table 6.7-1 Terminal Definition and Description of BI Module

Name	Description
BI01+	The No.1 and No.2 programmable binary input.
BI02+	
BI01~ BI02-	
BI03+	The No.3 and No.4 programmable binary input.
BI04+	
BI03~ BI04-	
BI05+	The No.5programmable binary input.
BI05-	
BI06+	The No.6 programmable binary input.
BI06-	
BI07+	The No.7 programmable binary input.
BI07-	
BI08+	The No.8 programmable binary input.
BI08-	
BI09+	The No.9 programmable binary input.
BI09-	
BI10+	The No.10 and No.11 programmable binary input.
BI11+	
BI10~ BI11-	
BI12+	The No.12 and No.13 programmable binary input.
BI13+	
BI12~ BI13-	
BI14+	The No.14programmable binary input.
BI14-	
BI15+	The No.15 programmable binary input.
BI15-	
BI16+	The No.16 programmable binary input.
BI16-	
BI17+	The No.17 programmable binary input.
BI17-	
BI18+	The No.18 programmable binary input.
BI18-	

6.8 Binary Output Module

The BO module consists of binary output, dry contacts, which conduct the signal functions showing the operating conditions or tripping and closing commands (protection, auto-recloser or remote control). The specific function is performed by setting the relevant settings and wiring the external copper cable. All the contacts can independently receive tripping or closing commands from the main CPU module and then conduct these commands.

All the binary outputs can be visually and flexibly configured through the PRS IED Studio configuration tool, which determine what information do they transmit between the CPU module and BO module.

This device can provide two types of binary output modules: SR7300 and SR7301.

The frame of the BO module terminal is described as below.

Table 6.8-1 Frame of BO Terminal

Output1		Output2	
1	TRIP01 Common	1	TRIP01 Common
2	TRIP01 Open	2	TRIP01 Open
3	TRIP02 Common	3	
4	TRIP02 Open	4	
5	TRIP03 Common	5	TRIP02 Common
6	TRIP03 Open	6	TRIP02 Open
7	TRIP04 Common	7	
8	TRIP04 Open	8	
9	TRIP05 Common	9	TRIP03 Common
10	TRIP05 Open	10	TRIP03 Open
11	TRIP06 Common	11	
12	TRIP06 Open	12	
13	SIGN07 Common	13	TRIP04 Common
14	SIGN07 Open	14	TRIP04 Open
15	SIGN08 Common	15	
16	SIGN08 Open	16	
17	SIGN09 Common	17	TRIP05 Common
18	SIGN09 Open	18	TRIP05 Open
19	SIGN10 Common	19	
20	SIGN10 Open	20	
21	SIGN11 Common	21	TRIP06 Common
22	SIGN11 Open	22	TRIP06 Open
23	SIGN11 Cls	23	
24	SIGN12 Common	24	
25	SIGN12 Open	25	TRIP07 Common
26	SIGN12 Cls	26	TRIP07 Open
27	SIGN13 Common	27	
28	SIGN13 Open	28	
29	SIGN13 Cls	29	TRIP08 Common
30	SIGN14 Common	30	TRIP08 Open
31	SIGN14 Open	31	
32	SIGN14 Cls	32	

The specific terminal definition of the connector is described as below.

Table 6.8-2 Terminal Definition and Description of output module 1

Name	Description
TRIP01-06	The No.1 -6 programmable tripping or closing binary output. TRIPi (i=1-6) Open is the normal open binary output.
SIGN07-10	The No.7-10 programmable signal binary output. SIGNi (i=7-10) Open is the normal open binary output
SIGN11-14	The No.11-14 programmable signal binary output. SIGNi (i=11-14) Open is the normal open binary output, SIGNi (i=11-14) Cls is the normal close binary output.

Note: The signal BO can only be used for signal transmission.

Table 6.8-3 Terminal Definition and Description of output module 2

Name	Description
TRIP01-08	The No.1 -08 programmable tripping or closing binary output.

6.9 Binary Input/Output Module

The IO module provides 7 binary outputs, some dry contacts, which conduct the signal functions showing the operating conditions (device error) or tripping and closing commands (protection, auto-recloser or remote control). The specific function is performed by setting the relevant settings and wiring the external copper cable.

The IO module also contains 9 binary inputs, the optical isolated input terminals, which can perform different monitoring functions, such as detecting the breaker and switch positions of the corresponding bay.All the BI terminals can be used as general purpose binary inputs or special purpose (protection function or control function) binary inputs.

All the binary inputs and outputs can be visually and flexibly configured through the PRS IED Studio configuration tool, which determine what information do they transmit between the CPU module and BO module.

The frame of the IO module terminal definition is described as below.

IO			
01	BI01+	SIGN01 Common	17
02	BI02+	SIGN01 Open	18
03	BI01~02 Common-	SIGN02 Common	19
04	BI03+	SIGN02 Open	20
05	BI04+	SIGN03 Common	21
06	BI03~04 Common-	SIGN03 Open	22
07	BI05+	SIGN04 Common	23
08	BI05-	SIGN04 Open	24
09	BI06+	SIGN05 Common	25
10	BI06-	SIGN05 Open	26
11	BI07+	SIGN06 Common	27
12	BI07-	SIGN06 Open	28
13	BI08+	SIGN06 Cls	29
14	BI08-	SIGN07 Common	30
15	BI09+	SIGN07 Open	31
16	BI09-	SIGN07 Cls	32

Figure 6.9.1 Frame of the IO Module Terminal

The terminal definition of the IO module is described as below.

Table 6.2-1 Terminal Definition and Description of IO Module

Name	Description
BI01+	The No.1 and No.2 programmable binary input.
BI02+	
BI01~ BI02-	
BI03+	The No.3 and No.4 programmable binary input.
BI04+	
BI03~ BI04-	
BI05+	The No.5programmable binary input.
BI05-	
BI06+	The No.6 programmable binary input.
BI06-	
BI07+	The No.7 programmable binary input.
BI07-	
BI08+	The No.8 programmable binary input.
BI08-	
BI09+	The No.9 programmable binary input.
BI09-	
SIGN01	The No.1 programmable signal binary output.
SIGN02	The No.2 programmable signal binary output.
SIGN03	The No.3 programmable signal binary output.
SIGN04	The No.4 programmable signal binary output.
SIGN05	The No.5 programmable signal binary output.
SIGN06	The No.6 programmable signal binary output.
SIGN07	The No.7 programmable signal binary output.

7 Human Machine Interface

7.1 Overview

HMI is known as the Human Machine Interface. HMI is the main communication interface between the control system and the operator. The friendly LCD facilitates the operator, providing all operating system information in the screen of the front display panel, including binary inputs or outputs, circuit breakers status, version of operating system program, alarm signals, tripping operation, disturbance records, and signal of measuring quantities (voltage, current and angle) etc., Besides these, its also useful for modifying the operating system configuration settings and protection function settings as well. The HMI can also be helpful during commissioning work.

Additionally, the PRS IED studio software helps to conduct all above listed function through communication port (Ethernet cable) on the PC or laptop.

7.1.1 Design Structure

The design structural of Human Machine Interface (HMI) is user friendly and easy to operate in different situations. The design structure detail of HMI is follow:

- For monitoring the signal status, fault records and configuration of settings, high quality 320×240 dot matrix LCD with dim lite green back light display is equipped.
- For the access of device functions and control settings. 1 enter and 1 cancel keys, 4 functional keys, 4 arrow keys, 2 remote and local control keys and 2 CB control keys.
- For the indication of different types of alarming and tripping signals. Front panel of HMI includes 21 LEDs light indicator.
- For the remote access from the PRS IED studio configuration software, Ethernet commissioning interface is available.

The front and back panels of relay shown in figure 6.1.2 and 6.1.3 respectively.

7.1.2 Function mode

- HMI screen is used to monitor the successively status and information of various events, and also helps to configure the protection settings and device operating mode
- Navigation menu keys help the operator to locate the required data or information.
- Data record and printing function is available in relay setting.

In simple words, all functions of relay are user friendly.

7.1.3 Operating panel keypad and keys

The relay front penal have 9 keypads and 8 function keys help the operator to change the device settings according to the required situation and locate the different kind of data access. These all keys and keypad have different kinds of functions.

Table 7.1-1 Keys information table

Symbol of keys	Description
	Arrow keys left, right up and down respectively
	Functional keys F1, F2, F3 and F4 respectively. These are configure according to user's demand.
	Different keys like Menu, Clear, Esc and Enter keys
	CB close key, Remote/Local control key, User login key and CB opening key respectively.

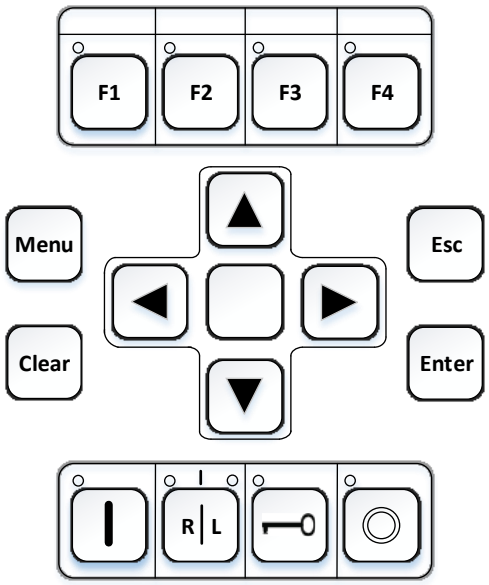


Figure 7.1.1 Overview of Front Panel Keypad and Keys

7.1.4 Indication of LED

The IED consists of 31 front panel LEDs. The local view of front panel HMI consists of two relay status LEDs above the display level: healthy and alarm. The nineteen other configurable LEDs on the front panel of local-HMI and each LEDs can be configured with three colors like green, red and yellow according to user requirement.These LEDs can be configured through local HMI or PRS IED Studio. Additionally, There are 19 LEDs, each of which can be configured with 3 colors. These LEDs can be triggered by a fault, alarm event or device record, and it indicate last information.

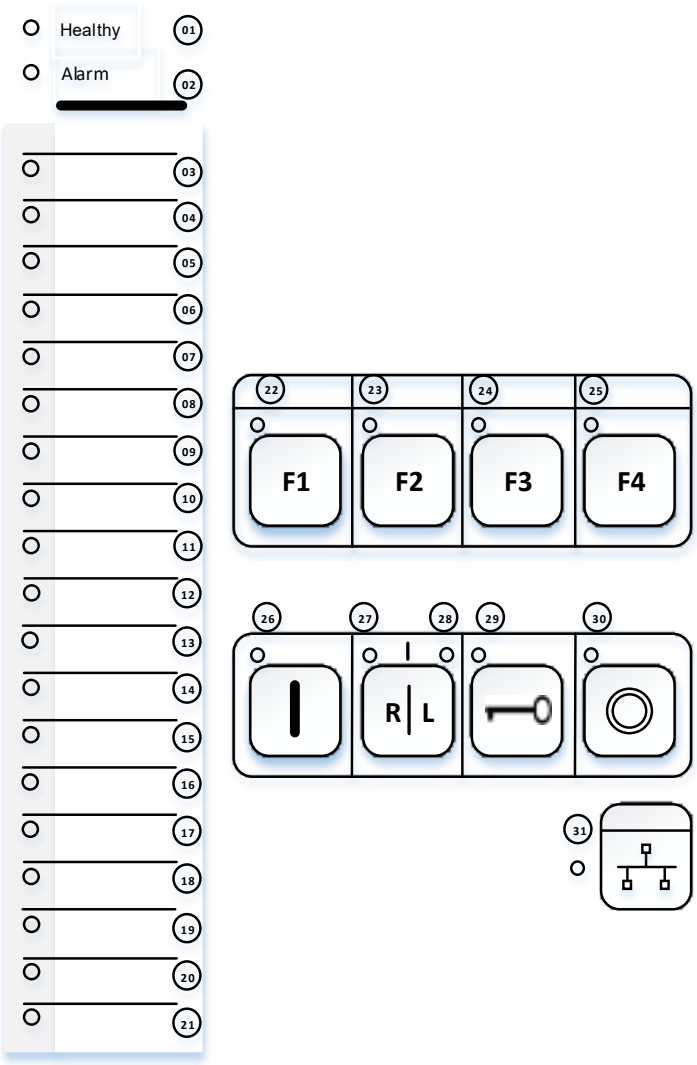


Figure 7.1.2 Overview of Front Panel LED's

Table 7.1-2 LED indications

No.	Key label	Status	Description
01	Healthy	Off	When the device is not energized.
		Green	When the device is in normal working mode and ready to operate
02	Alarm	Off	No alarm signal is energized when the device running normally.
		Yellow	Alarm signal is issued. When any kind of abnormality signal is detected. LED light color is fixed yellow.
03~21	Configurable	Off	None of signal is energized when the device running normally. If state configuration is "hold", it only can be reset by Pushbutton or Keypad.

No.	Key label	Status	Description
		Green/Yellow/Red	These LEDs can be configured according to user demand like different operating functions, such as tripping, alarm, reclose, CB open or close and synchro-check etc.
22~25	Configurable	Off	None of signal is energized when the functional key is deactivated.
		Red	These LEDs indicate the functional keys are deactivated.
26	CB Close	Off	None of signal is energized when the functional key is deactivated.
		Yellow	This LED indicate the CB Close key is activated.
27	Remote	Off	The operation mode is determined by the BI.
		Yellow	The device is in the “remote” mode
28	Local	Off	The operation mode is determined by the BI.
		Yellow	The device is in the “Local” mode
29	User login	Off	When user login function is not enable.
		Yellow	When user login function works normally.
30	CB Open	Off	None of signal is energized when the functional key is deactivated.
		Yellow	This LED indicate the CB Open key is activated.
31	Ethernet interface port	Off	When no Ethernet cable is connected with device.
		Green	When it works normally.

NOTICE!

No.01-02 and No.22-31 cannot set status because it is the fixed value.

- **General description of LEDs indication**

Healthy

This LED indication shows, device is energized through normal power supply, and ready to work under the normal atmosphere.

Alarm

This LED indication shows, when any abnormality alarm is detected in the system.

Trip

This LED indication shows, when any protection function is operated.

ARReady

This LED indication shows, when auto-recloser function is ready.

Reclose

This LED indication shows, when auto-recloser function is operated.

TripA

This LED indication shows, when 94T Trip A function is operated.

TripB

This LED indication shows, when 94T Trip B function is operated.

TripC

This LED indication shows, when 94T Trip C function is operated.

7.1.5 Configurable keys

The device HMI front panel consists of four configurable keys. These configurable functional keys provide shortcuts for certain menu or act as a control button. The default view of configurable functional keys (F1, F2, F3 and F4) are shown in above figure 7.1.1. The detail operation of functional keys is listed in below table 7.1.3:

Table 7.1-3 Information of functional keys

Keys	Function	Description	Remarks
F1, F2, F3 and F4	Control	For binary input and output control instantiated according to the configuration tool	This control function, control through three ways like puls, hold and exit.
	Shortcut	"System single line", "Measurement", “Binary input” “Fault record “ “Disturbance” “Clear” “Setting group” 7 selected 1	This shortcut function provide easy access to device operation settings and it is configurable according to user demand.
	Sign out	Do not perform the key function	-

7.2 LCD Display description of HMI

7.2.1 Overview

In this part of HMI, the detail of LCD display function is described.

7.2.2 Normal display structure of LCD

The normal operating condition of local HMI LCD display structure is shown below in figure 7.2.1, the single-line diagram is based on the practical arrangement of equipment, monitoring the position status of CB and Isolator in real time.

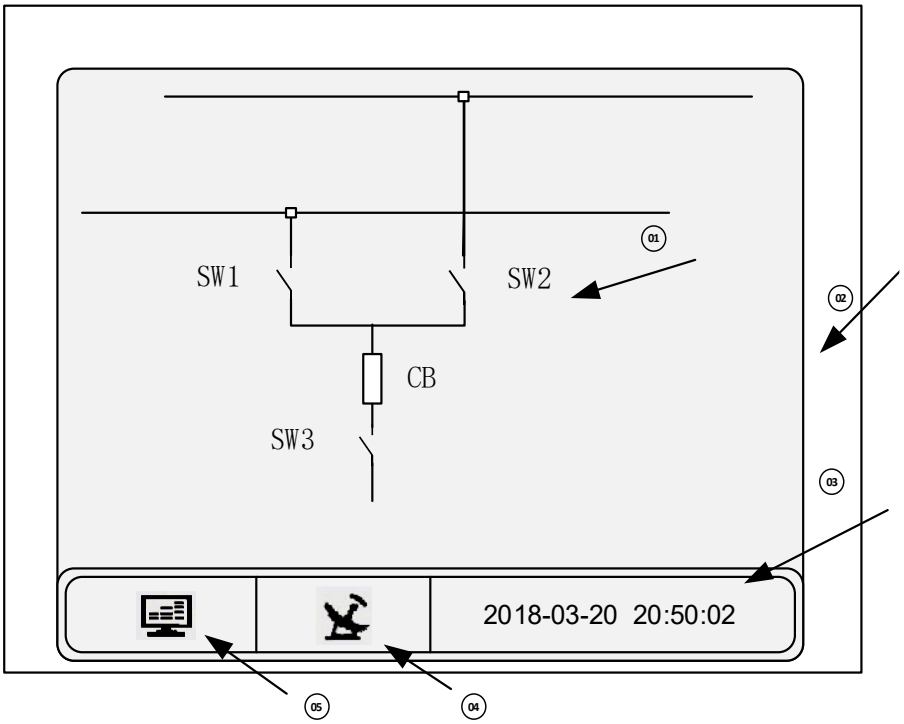


Figure 7.2.1 General Overview Display of Local HMI LCD Screen

According to the overview of local HMI. LCD display is divided into five parts. These parts are listed below:

1. Main data display zone
2. Outer boundary zone
3. Date and time display zone
4. Time synchronization or GPS
5. Data monitoring zone

Main data display zone provides information that the user wants to access like measurement value status, fault records, circuit breaker status, single line diagrams, alarm signals, protection function settings, and synchronization status etc.

Outer boundary zone is known as free text zone and no data display in this zone. It defines the boundary of LCD display zone.

Date and time display zone shows the real monitoring value of date and time. The user can set these date and time value according to requirement. The display format of date and time is yyyy-mm-dd and hh:mm:ss respectively. The time setting format can be easily set to the user time zone demand.

7.2.3 Main menu display

In order to make sure the user can control PRS-753 relay easier, simple and fast, the CYG Co, Ltd designs a flat-panel of main menu LCD display that contain ten main controlling function.

These controlling function are listed below:

1. Physical
2. Review
3. Monitor
4. Event
5. Record
6. Setting
7. Config
8. Test
9. Clear
10. Language

The main menu display screen shown in below figure 7.2.2. The main menu will deal with the operation of installation work together with providing basic support and instructions to help user control.

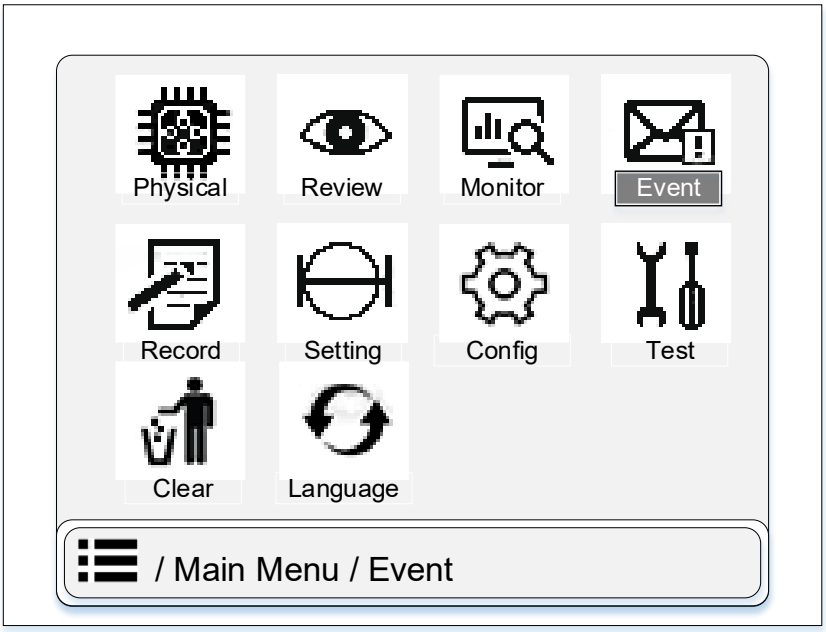


Figure 7.2.2 LCD General Overview Display of Main Menu

7.3 Sub menu functions of main menu

This part of HMI, the detail of menu sub-functions is described. These all sub-functions display on the front panel of HMI LCD.

7.3.1 Physical Information

In this section, describe all the physical information related to device firmware and device

communication. The overview display of physical information is shown in below figure 7.3.1.

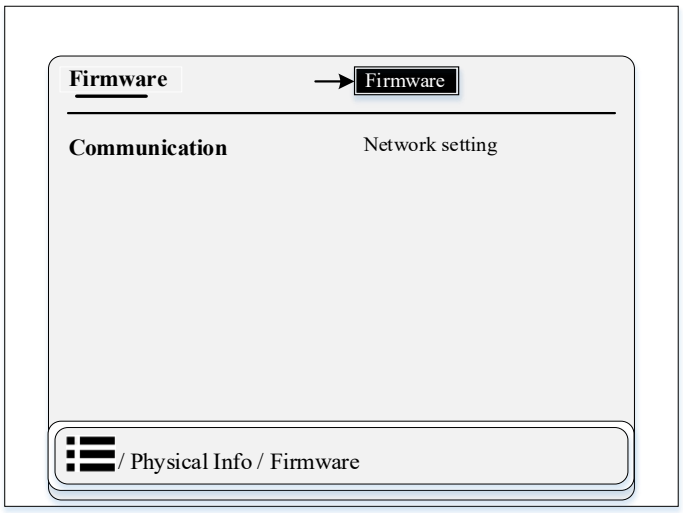


Figure 7.3.1 Overview Display of Physical Information Sub-functions

7.3.1.1 Software

In this sub-section of physical information, the firmware information of the protection relay is described, including the device type, protection relay software version, S/N code and protection date etc. User can access this function through the following path: “Physical > Firmware”. The firmware information data divided into two pages and the detail of information is listed in below figure 7.3.2 and table 7.3.1:

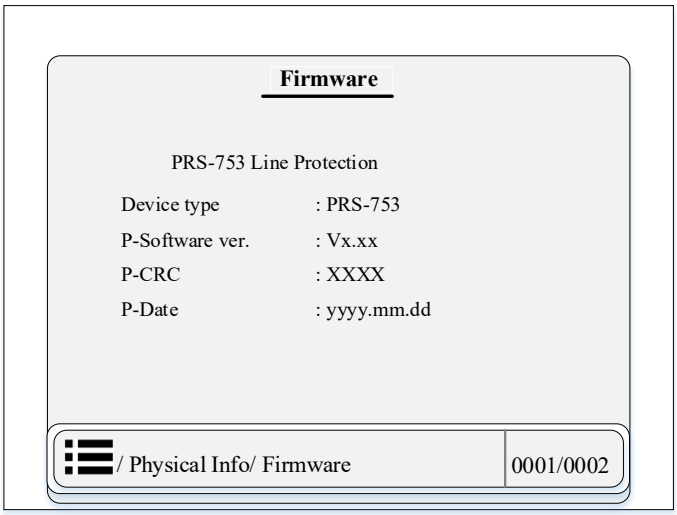


Figure 7.3.2 Overview Display Diagram of Software Information

Table 7.3-1 Detail of Software information

Name	Function display	Description
Device type	PRS-753	Discribe the type of protection relay
P-Software ver	Vx.xx	Describe the version of protection relay software
P-CRC	XXXX	Protection Cyclic redundancy check code
P-Date	Yyyy-mm-dd	Protection CPU date

Name	Function display	Description
M-Software ver.	Vx.xx	MCPU software version
M-CRC	XXXX	MCPU Cyclic redundancy check error
M-Date	Yyyy.mm.dd	Management CPU date
S/N code	***-****************	S/N code
Ordering Code	***-****-*-******-*****-**.**	Ordering Code
Config. Ver.	Vx.xx	The configuration version

For example: the relay used in one project, the detail of software information can be display in Table 7.3-2.

Table 7.3-2 Detail of Software information

Name	Function display	Description
Device type	PRS-753	Discribe the type of protection relay
P-Software ver	V2.03	Describe the version of protection relay software
P-CRC	8FE8	Protection Cyclic redundancy check code
P-Date	2018.03.01	Protection CPU date
M-Software ver.	V2.03	MCPU software version
M-CRC	66A7	MCPU Cyclic redundancy check error
M-Date	2018.03.01	Management CPU date
S/N code	CYSR30000000FFFFFFF	S/N code
Ordering Code	PRS-753-AACAA-BABXAABBDDXXXXXXXXAAXA	Ordering Code
Config. Ver.	V2.03	The configuration version

7.3.1.2 Communication

This section, describes the information communication of network setting of the protection relay including IP, MAC and NetMask of network 1, 2 and 3 respectively. User can access this function through the following path: “Physical information > communication”. The network setting data of communication information is listed in below figure 7.3.3 and table 7.3.2:

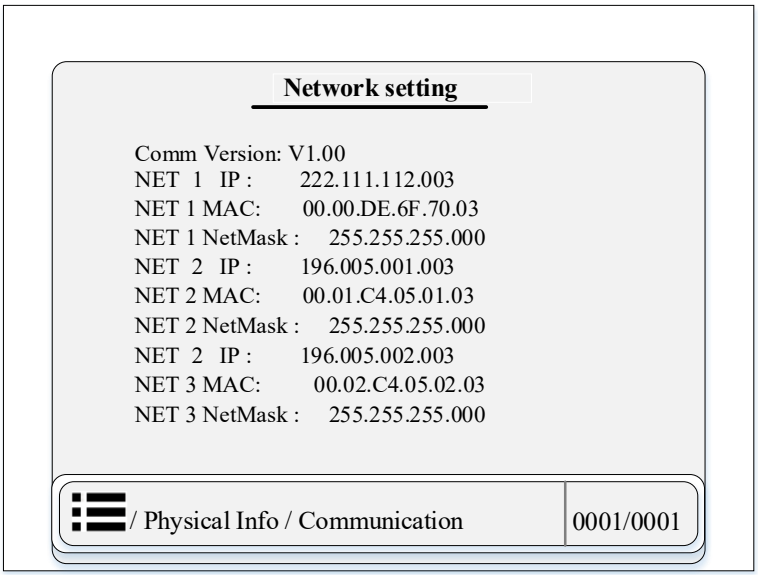


Figure 7.3.3 Overview Display Diagram of Network Setting

Table 7.3-3 Communication data detail

Name	Function display	Description
NET 1 IP	222.111.112.003	IP address of internet protocol for Ethernet port 1
NET 1 MAC	00.00.DE.6F.70.03	MAC address of internet protocol for Ethernet port 1
NET 1 NetMask	255.255.255.000	NetMask address of internet protocol for Ethernet port 1
NET 2 IP	196.005.001.003	IP address of internet protocol for Ethernet port 2
NET 2 MAC	00.01.C4.05.01.03	MAC address of internet protocol for Ethernet port 2
NET 2 NetMask	255.255.255.000	NetMask address of internet protocol for Ethernet port 2
NET 3 IP	196.005.002.003	IP address of internet protocol for Ethernet port 3
NET 3 MAC	00.02.C4.05.02.03	MAC address of internet protocol for Ethernet port 3
NET 3 NetMask	255.255.255.000	NetMask address of internet protocol for Ethernet port 3

7.3.2 Review Information

This section is divided into two sub-parts, including time mode and the information how to review protection relay monitoring data. This section only provides the setting view display and user can't change the display information of relay. The overview display of review information is shown in below figure 7.3.4.

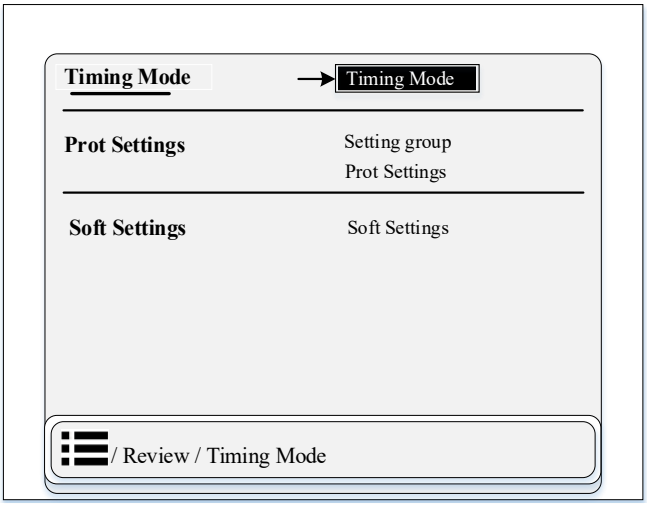


Figure 7.3.4 Overview Display of Review Information Sub-functions

7.3.2.1 Timing Mode

This section, the user can see the time information like Uart IRIG-B, Opti IRIG-B and SNTP (Simple Network Time Protocol) information and the user can't change any kind of information. Users can access this function through the following path: "Review > Timing Mode". The overview display of timing mode is shown in below figure 7.3.5.

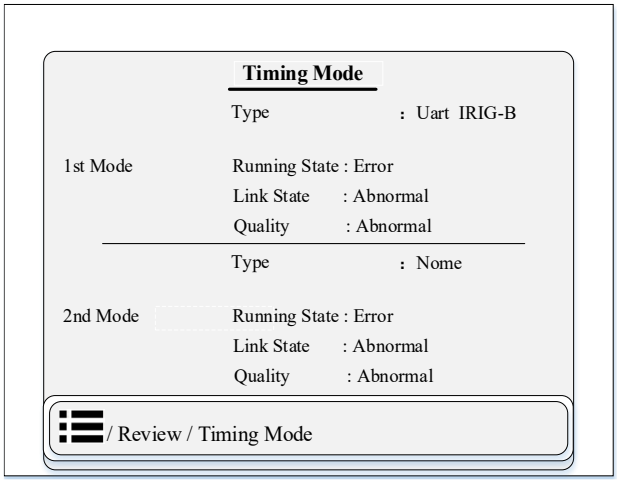


Figure 7.3.5 Overview Display of Timing Mode

7.3.2.2 Prot Settings

This section is divided into two sub-parts like setting group and protection settings.

1- Setting Group

This sub-section the user can see the information about which group is the current group. There are totally 4 groups. There are totally 4 groups, and the setting groups can be switched locally or remotely respectively.

2- Prot Settings

This section the user can see the different kind of protection function settings . User can access

this function through the following path: “Review > Prot Settings”. The information data structure of protection setting is listed in below figure 7.3.6:

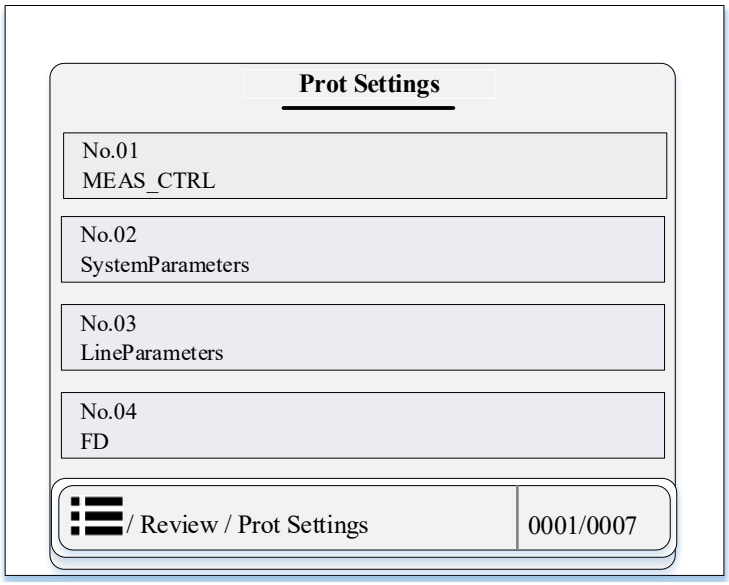


Figure 7.3.6 Overview Diagram of Prot Settings

7.3.3 Monitoring Information

This section divided into five sub-parts and describe the information of real time monitoring data of PRS-753 line protection. This section only provides the Sampling Value, BI, BO Count, Status, Prot Ch data information. In this section user can easily access the real-time monitoring data view of relay through arrow keys. The overview display of monitoring information are shown in below figure 7.3.7.

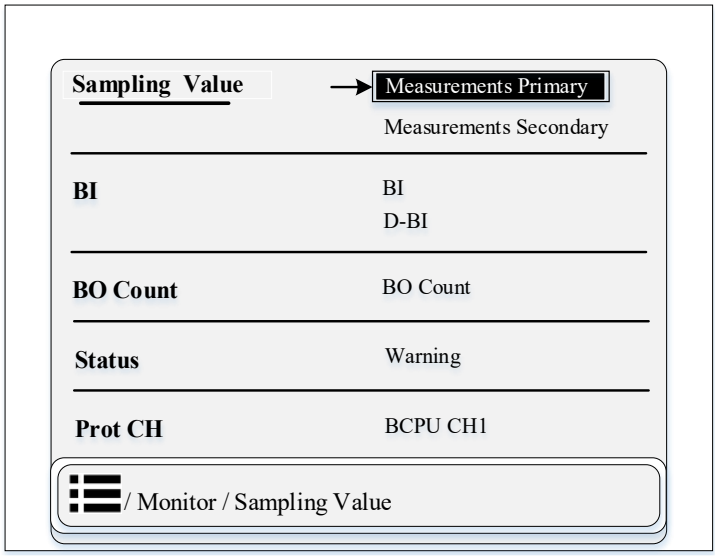


Figure 7.3.7 Overview Display of Monitoring Information Sub-functions

7.3.3.1 Sampling Value

This section divided into two sub part like Measurements Primary and Measurements Secondary. These both describe the detail information of all measurement values such as current, voltage and

angle etc. User can access this function through the following path: “Monitor > Sampling Value”. The measurement data structure of relay is listed in below figure 7.3.8 and table 7.3.4:

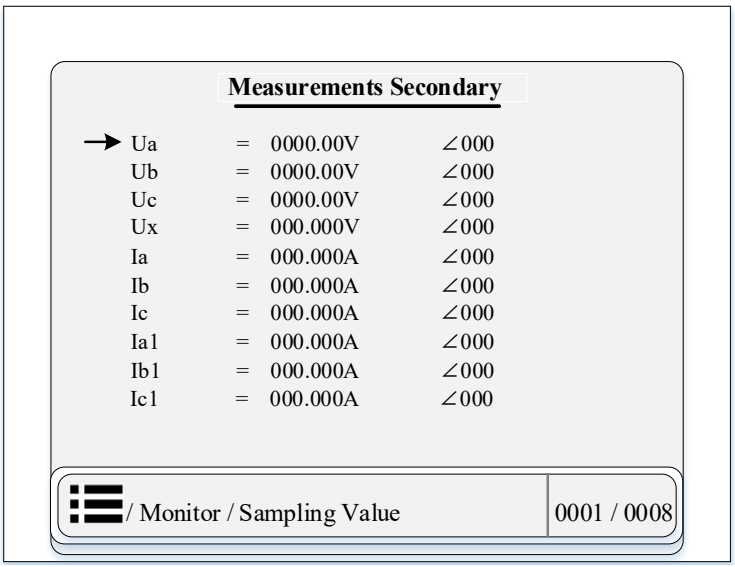


Figure 7.3.8 Overview Display of Measurement Section Quantities

Table 7.3-4 Measurement quantaties

No.	Measurment function	Value (range)	Description
1	Ua	0000.00V	Phase A voltage
2	Ub	0000.00V	Phase B voltage
3	Uc	0000.00V	Phase C voltage
4	Ux	0000.00V	Synchronism voltage
5	Ia	000.000A	Phase A current (For single circuit breaker mode, it’s from circuit breaker No.1, the setting CT_Group must set as “1”. For double circuit breaker mode, it’s the sum of circuit breaker No.1 and circuit breaker No.2, the setting CT_Group must set as “2”)
6	Ib	000.000A	Phase B current (For single circuit breaker mode, it’s from circuit breaker No.1, the setting CT_Group must set as “1”. For double circuit breaker mode, it’s the sum of circuit breaker No.1 and circuit breaker No.2, the setting CT_Group must set as “2”)
7	Ic	000.000A	Phase C current (For single circuit breaker mode, it’s from circuit breaker No.1, the setting CT_Group must set as “1”. For double circuit breaker mode, it’s the sum of circuit breaker No.1 and circuit breaker No.2, the setting CT_Group must set as “2”)
8	Ia1	000.000A	Phase A current for circuit breaker No.1
9	Ib1	000.000A	Phase B current for circuit breaker No.1
10	Ic1	000.000A	Phase C current for circuit breaker No.1
11	Ia2	000.000A	Phase A current for circuit breaker No.2 (It’s applied to double circuit breaker mode, and the setting CT_Group must set as “2”)

No.	Measurment function	Value (range)	Description
12	Ib2	000.000A	Phase B current for circuit breaker No.2 (It's applied to double circuit breaker mode, and the setting CT_Group must set as "2")
13	Ic2	000.000A	Phase C current for circuit breaker No.2 (It's applied to double circuit breaker mode, and the setting CT_Group must set as "2")
14	I01	000.000A	Residual current from external source for circuit breaker No.1(Not used)
15	I02	000.000A	Residual current from external source for circuit breaker No.2 (It's applied to double circuit breaker mode, and the setting CT_Group must set as "2") (Not used)
16	1_Uam	0000.00V	Phase-A voltage of optical fibre channel 1 at the local end
17	1_Ubm	0000.00V	Phase-B voltage of optical fibre channel 1 at the local end
18	1_Ucm	0000.00V	Phase-C voltage of optical fibre channel 1 at the local end
19	1_Uan	0000.00V	Phase-A voltage of optical fibre channel 1 from the remote end
20	1_Ubn	0000.00V	Phase-B voltage of optical fibre channel 1 from the remote end
21	1_Ucn	0000.00V	Phase-C voltage of optical fibre channel 1 from the remote end
22	1_Iam	000.000A	Phase-A current of optical fibre channel 1 at the local end
23	1_Ibm	000.000A	Phase-B current of optical fibre channel 1 at the local end
24	1_Icm	000.000A	Phase-C current of optical fibre channel 1 at the local end
25	1_Ian	000.000A	Phase-A current of optical fibre channel 1 from the remote end
26	1_Ibn	000.000A	Phase-B current of optical fibre channel 1 from the remote end
27	1_Icn	000.000A	Phase-C current of optical fibre channel 1 from the remote end
28	1_Ida	000.000A	Phase-A differential current of optical fibre channel 1
29	1_Idb	000.000A	Phase-B differential current of optical fibre channel 1
30	1_Idc	000.000A	Phase-C differential current of optical fibre channel 1
31	2_Uam	0000.00V	Phase-A voltage of optical fibre channel 2 at the local end
32	2_Ubm	0000.00V	Phase-B voltage of optical fibre channel 2 at the local end
33	2_Ucm	0000.00V	Phase-C voltage of optical fibre channel 2 at the local end
34	2_Uan	0000.00V	Phase-A voltage of optical fibre channel 2 from the remote end
35	2_Ubn	0000.00V	Phase-B voltage of optical fibre channel 2 from the remote end
36	2_Ucn	0000.00V	Phase-C voltage of optical fibre channel 2 from the remote end
37	2_Iam	000.000A	Phase-A current of optical fibre channel 2 at the local end
38	2_Ibm	000.000A	Phase-B current of optical fibre channel 2 at the local end
39	2_Icm	000.000A	Phase-C current of optical fibre channel 2 at the local end
40	2_Ian	000.000A	Phase-A current of optical fibre channel 2 from the remote end
41	2_Ibn	000.000A	Phase-B current of optical fibre channel 2 from the remote end
42	2_Icn	000.000A	Phase-C current of optical fibre channel 2 from the remote end
43	2_Ida	000.000A	Phase-A differential current of optical fibre channel 2
44	2_Idb	000.000A	Phase-B differential current of optical fibre channel 2
45	2_Idc	000.000A	Phase-C differential current of optical fibre channel 2
46	Uab	0000.00V	Phase AB voltage
47	Ubc	0000.00V	Phase BC voltage

No.	Measurment function	Value (range)	Description
48	Uca	0000.00V	Phase CA voltage
49	U1a	0000.00V	Positive sequence voltage
50	U2a	0000.00V	Negative sequence voltage
51	3U0a	0000.00V	Calculated residual voltage
52	Iab	000.000A	Phase AB current
53	Ibc	000.000A	Phase BC current
54	Ica	000.000A	Phase CA current
55	I1a	000.000A	Positive sequence current
56	I2a	000.000A	Negative sequence current
57	3I0a	000.000A	Calculated residual current
58	1_Idca	000.000A	Phase-A differential current of optical fibre channel 1 after capacitive current compensation
59	1_Idcb	000.000A	Phase-B differential current of optical fibre channel 1 after capacitive current compensation
60	1_Idcc	000.000A	Phase-C differential current of optical fibre channel 1 after capacitive current compensation
61	1_Idc0	000.000A	Calculated residual differential current of optical fibre channel 1 after capacitive current compensation
62	2_Idca	000.000A	Phase-A differential current of optical fibre channel 2 after capacitive current compensation
63	2_Idcb	000.000A	Phase-B differential current of optical fibre channel 2 after capacitive current compensation
64	2_Idcc	000.000A	Phase-C differential current of optical fibre channel 2 after capacitive current compensation
65	2_Idc0	000.000A	Calculated residual differential current of optical fibre channel 2 after capacitive current compensation
66	1_Ira	000.000A	Phase A restraint current optical fibre channel 1
67	1_Irb	000.000A	Phase B restraint current optical fibre channel 1
68	1_Irc	000.000A	Phase C restraint current optical fibre channel 1
69	2_Ira	000.000A	Phase A restraint current optical fibre channel 2
70	2_Irb	000.000A	Phase B restraint current optical fibre channel 2
71	2_Irc	000.000A	Phase C restraint current optical fibre channel 2
72	UabFr	000.000 Hz	Frequency
73	UxFr	000.000 Hz	Frequency of synchronism voltage
74	P	0000.00W	Active power
75	Q	0000.00Var	Reactive power
76	S	0000.00VA	Apparent power
77	UDiff	0000.00V	Voltage difference between reference voltage and synchronism voltage
78	AngDiff	000.00°	Phase angle difference between reference voltage and synchronism voltage

No.	Measurment function	Value (range)	Description
79	FrDiff	000.000Hz	Frequency difference between reference voltage and synchronism voltage

7.3.3.2 BI

This section divided into two sub-parts and describe the information of binary input (BI) of this IED seen in the above figure 7.3.7. This section only displays all the binary input data. User can access this function through the following path: “Monitor > BI”.

1- BI

This part of single BI monitoring data depends on the actual configuration. The BI display diagram of the IED is listed in below figure 7.3.9 (a):

2- D-BI

D-BI is stand for double binary input function. The D-BI display diagram of relay is listed in below figure 7.3.9 (b):

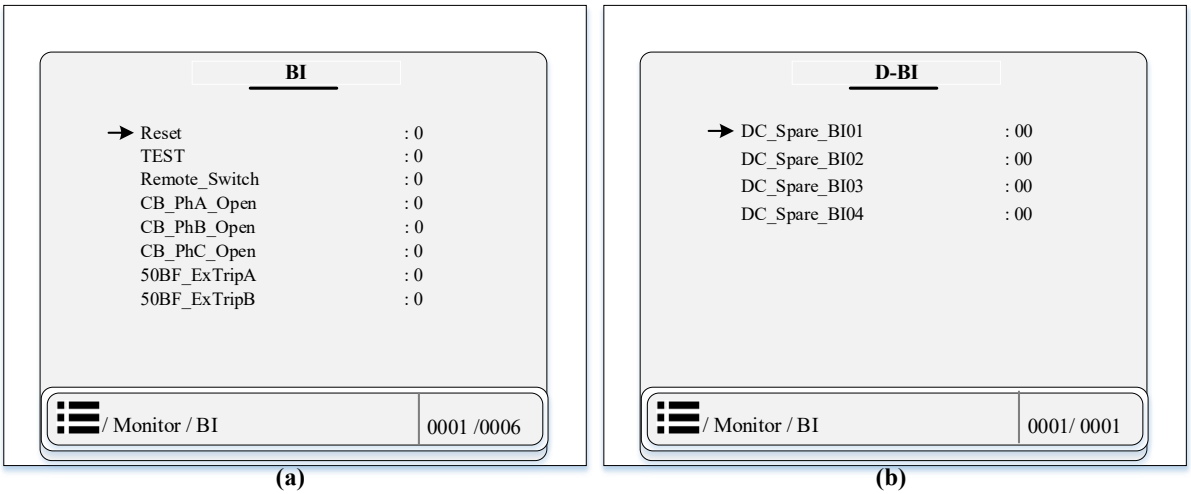


Figure 7.3.9 LCD Display Diagram of (a) BI Monitored Data (b) D-BI Monitored Data

7.3.4 Event Information

This section is divided into four sub-section and describe the information of all events, like start records, fault records, alarming information (warning records), selfchk info, SOE, remote control, user records and run records etc. The LCD display event diagram of the IED is listed in below figure

7.3.10:

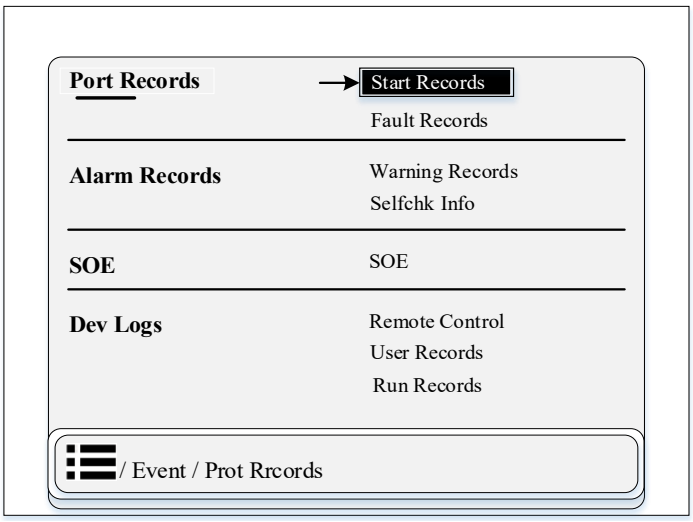


Figure 7.3.10 Overview Display of Event Information Sub-functions

7.3.4.1 Port Records

This section divided into two sub-function like start records and fault records. This device can store 512 latest protection records. User can access this function through the following path: “Event > Port Records”. Taking fault records as an example, the detail of this section divided into nine points:

1. Shows date and time
2. Protection function status
3. Shows operation of protection function like which protection function is acted.
4. Shows operated phases information
5. Shows fault clearance delay time
6. Shows slot info like protection slot (slot4).
7. Shows fault number
8. Not reverted
9. Shows fault events page number information, it will be increase or decrease w.r.to numbers of fault.

The diagram of fault event display of relay is listed in below figure 7.3.11:

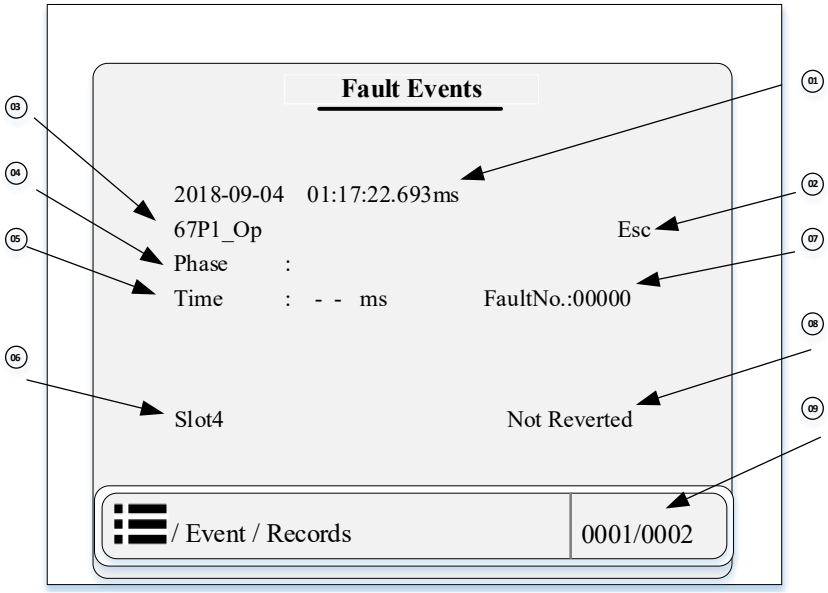


Figure 7.3.11 Overview Display of Fault Events

7.3.4.2 Alarm Records

This section divided into two sub-functions like warning records and selfchk Info see figure 7.3.10.

1- Warning Records

In this section user can see all warning records like protection warning records and TimingErr warning records etc. User can access this function through the following path: “Event > Alarm Records”. The IED can store 512 latest time tagged warning records. The overview display of warning record is shown in below figure 7.3.12.

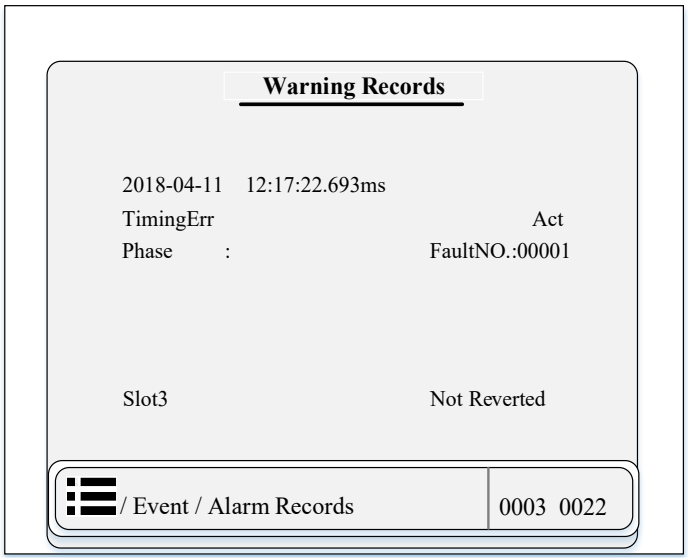


Figure 7.3.12 Overview Diagram of Warning Records Info

2- Selfchk Info

The self-check info checks the communication status between devices, such as carrier channel abnormality, fiber channel abnormality, GOOSE communication abnormality and internal AD sampling abnormality and etc. To summarize, this device also check hardware, software and configuration file and it can totally save latest 128 records. User can access this function through the following path: “Event > Alarm Records”. The overview display of SelfChk info is shown in below figure 7.3.13.

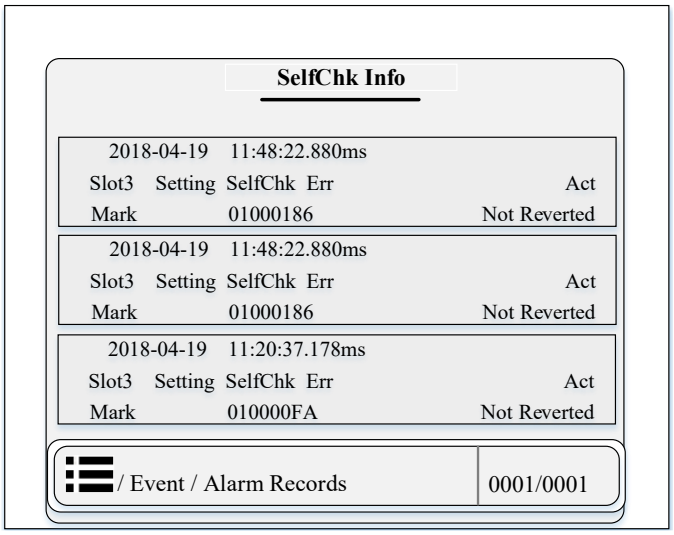


Figure 7.3.13 Overview Display Diagram of SelfChk Info

7.3.4.3 SOE

In this section SOE checks following condition:

- When the state of binary input signal changes, eg. a hard contact, the time tag of the state quantity is marked by the device and the time is defined after denouncing.
- When the state of GOOSE signal changes, the time tag of the state quantity adopts the external input source signal time tag. The GOOSE signal acquisition has no denouncing time.

User can access this function through the following path: “Event > SOE”. This device can save 2000 latest SOE records. The diagram of SOE record is shown in below figure 7.3.14.

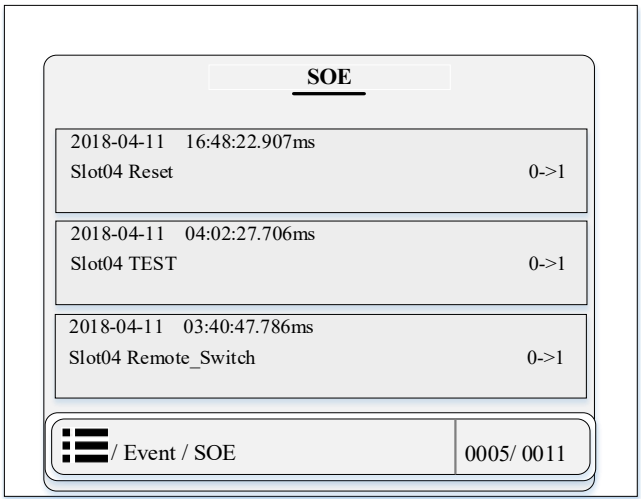


Figure 7.3.14 Overview Display Diagram of SOE

7.3.4.4 Dev Logs

This section divided into three sub-function like remote control, user records and power records see figure 7.3.10.

1- Remote Control

This part shows the remote control signals like circuit breaker, disconnector, reset signal, transformer tap changer, earthing switches etc. The recorded information includes the command source, command time, operation result and failure reason etc. This device can store 128 latest remote control records. User can access this function through the following path: “Event > Dev Logs”. The diagram of remote control functions are shown in below figure 7.3.15.

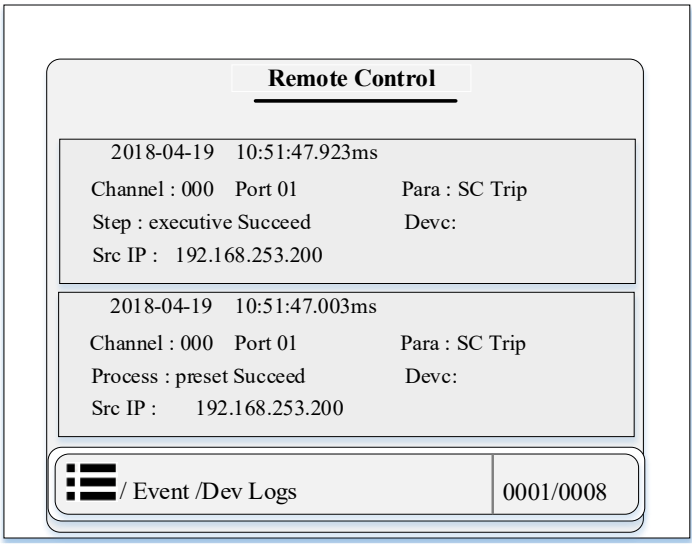


Figure 7.3.15 Overview Display Diagram of Remote Control Access

2- User Records

In this section user can see the setting of user records with slot number, time and date. User can access this function through the following path: “Event > Dev Logs”. The diagram of user records are shown in below figure 7.3.16.

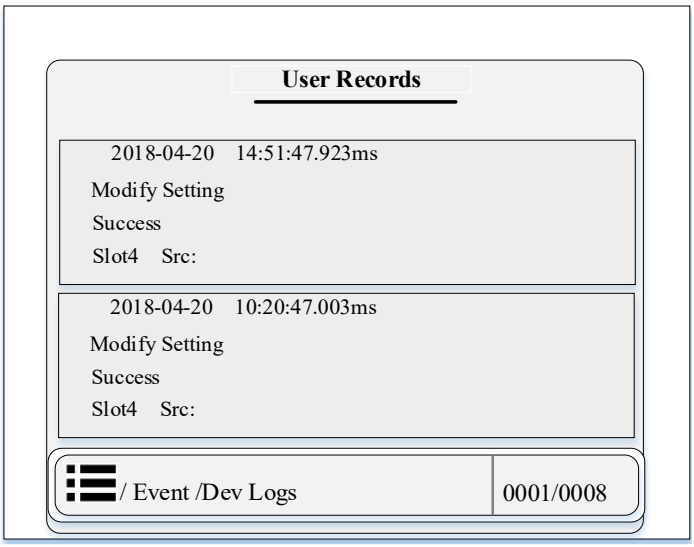


Figure 7.3.16 Overview Diagram of User Records

3- Run records

In this section user can see the setting of power records date and time with energizing and dis-energizing slot number. The number of pages of this section can be increase or decrease through the storage of power records. User can access this function through the following path: “Event > Dev Logs”. The diagram of power record is shown in below figure 7.3.17.

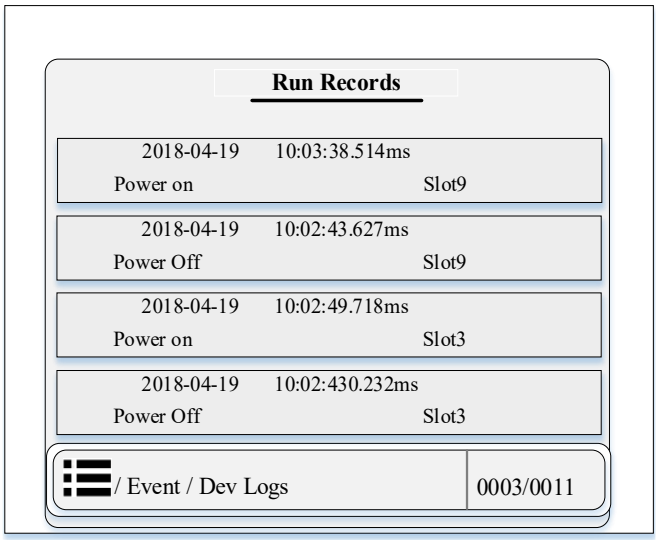


Figure 7.3.17 Overview Diagram of Run Records

7.3.5 Record Information

In this section, user can see the disturbance records and this section is divided into one sub-section. The diagram of disturbance record is shown in below figure 7.3.18.

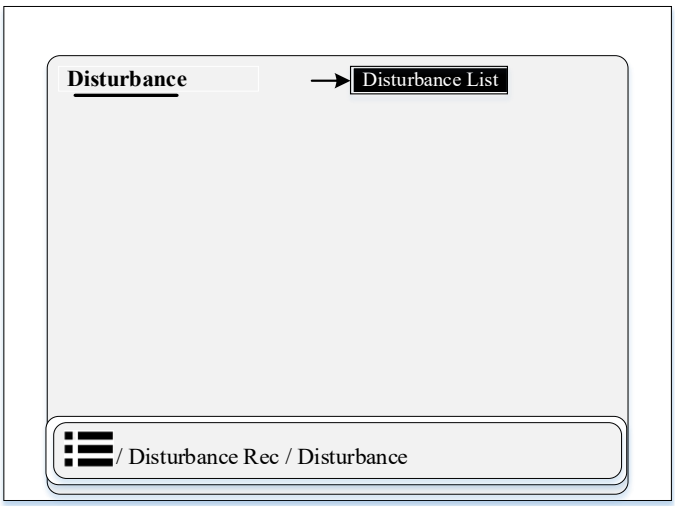


Figure 7.3.18 Overview Display of Records Information

7.3.5.1 Fault wave

In this section user can see the disturbance records of all the faults. User can access this function through the following path: “Disturbance > Disturbance List”. The diagram of faulty wave records are shown in below figure 7.3.19.

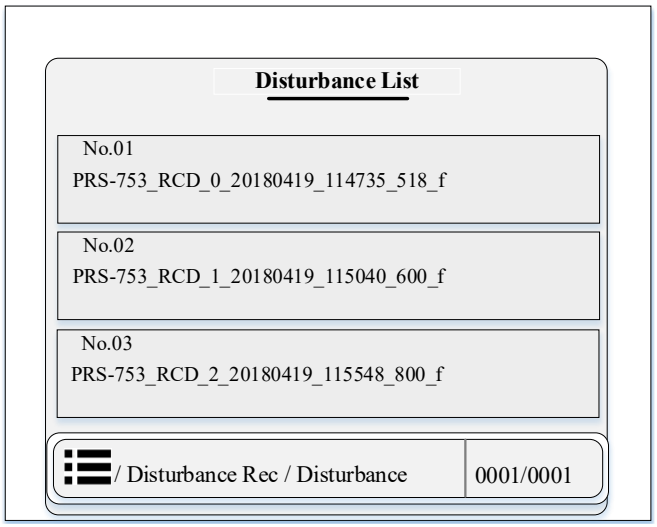


Figure 7.3.19 Overview Diagram of Disturbance List

7.3.6 Setting Information

This section divided into two sub-section like set group and protection settings. In this part user can set the device configuration according to operation demand. The overview display of setting information is shown in below figure 7.3.20.

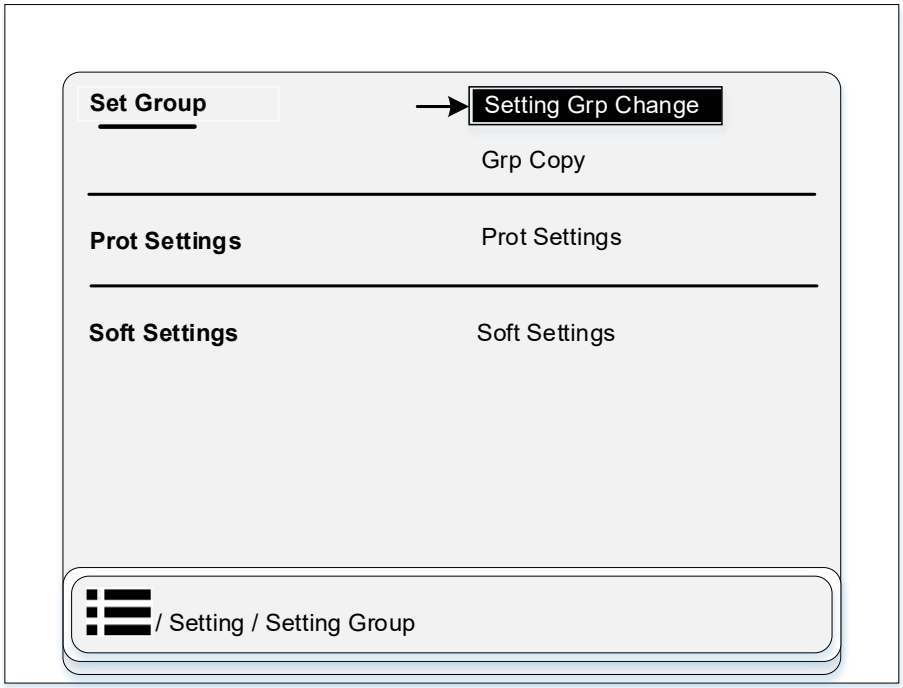


Figure 7.3.20 Overview Display of Setting Information Sub-functions

7.3.6.1 Set Group

This sub-section is divided into two further sub-section like Set Grp change and Grp Copy and in this part user can change the group setting.

1- Set Grp change

This device has four setting groups and user can easily configure the group setting according to operation demand. This setting is divided into four steps. User can access this function through the following path: “Setting > Setting group”. The procedure of group setting change is explaining in below figure 7.3.21.

Firstly, enter “Setting > Setting group > Setting Grp Change”. Secondly, select group setting. Thirdly, download new configuring setting. Fourthly, cancel to return back or exit.

Figure 7.3.21 Procedure Diagram of Group Setting Change

2- Grp Copy

This device has four setting groups and user can easily copy one group settings and save this same setting in other group. User can access this function through the following path: “Setting > Setting group”. The procedure detail of group setting copy is explaining in below figure 7.3.22.

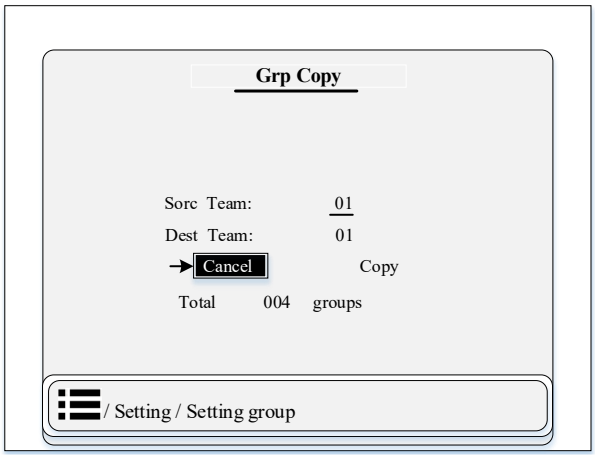


Figure 7.3.22 Procedure Diagram of Group Setting Copy

7.3.6.2 Prot Settings

In this section user can change the different kind of protection function settings. User can access this function through the following path: “Setting > Prot Settings”.

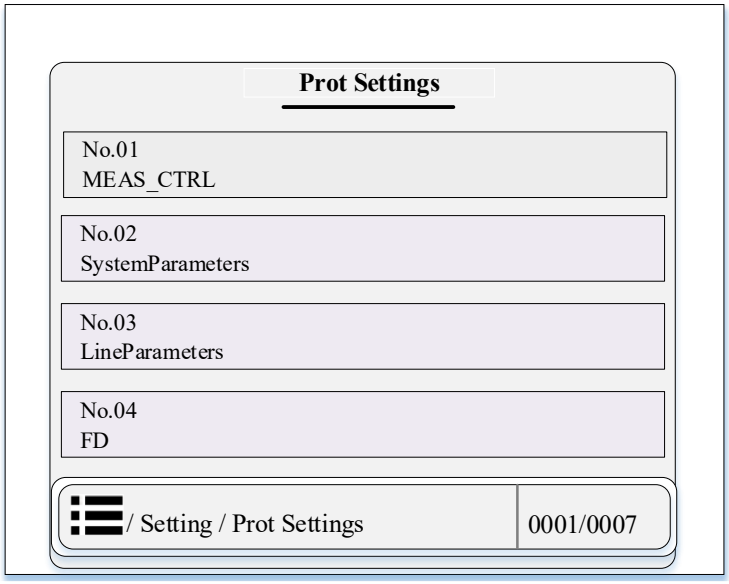


Figure 7.3.23 Diagram of Protection Setting

7.3.7 Configuration Information

This section divided into two sub-function like time and authorization. In this part user can set the device date and time according to the time zone of certain country. Besides that, the monitoring and controlling authorization of different users (of different post) can also be modified. The diagram of configuration information is shown in below figure 7.3.24.

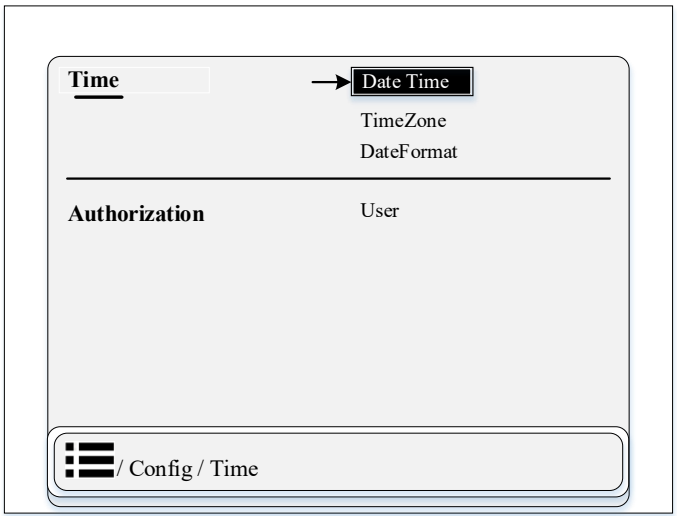


Figure 7.3.24 Overview Display of Configuration Information Sub-functions

7.3.7.1 Time

This part is divided into two sub-section date & time and time zone see figure 7.3.24. User can access this function through the following path: “Config > Time”.

1- Date and time

In this section user can easily set date and time according to practical demand. See figure 7.3.25 (a):

2- Time zone

In this section user can easily set time zone according to their region. See figure 7.3.25 (b):

3- Date Format

In this section user can easily set date format according to their region, such as yyyy-mm-dd, dd-mm-yyyy, MM/dd/yyyy and other 9 date formats. See figure 7.3.26 (c):

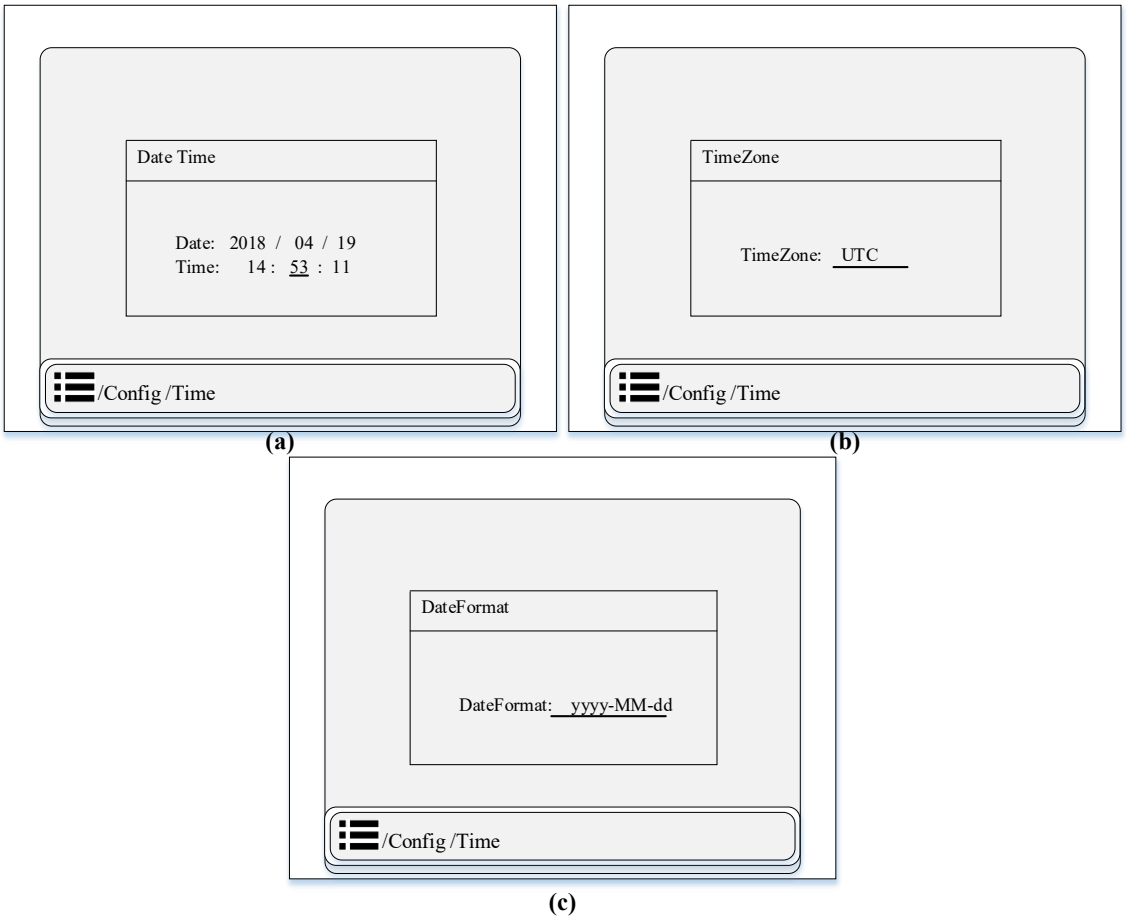


Figure 7.3.25 Diagram of (a) Date & Time Setting (b) Time Zone Setting(c) DateFormat Setting

7.3.7.2 Authorization

This part is divided into one sub-function. see figure 7.3.24. User can access this function through

the following path: “Config > Authorization”.

1- User

In this section user can easily set relay operator setting like operator 1 or 2 or guest 1. See below table 7.3.5 and figure 7.3.26:

Table 7.3-5 User setting detail

User operator selection options	Authorization
Manuf	The manufacturer user has all the configuration functions of access to device setting. At the same time, only the manufacturer's user has the access to hide, read, and write (display) to the logical device LD, logical component LN and logical component data item DO of 61850 protocol and logical picture subgraph. Therefore, as to realize the manufacturer's basic configuration of the device and not be suitable for opening up the correlation. The content settings for users are hidden and should not be opened to users to modify, but the contents they need to view are set to read-only. ***Note!*** Non of other users have access to this setting function except manufacturer.
Engin_1	The engineering user staff account has all the general access of configuration (view and modification) functions of the configuration tool, including drawing logical pictures, main wiring diagrams etc. ***Note!*** In this user login section, user cannot create an account configuration of the configuration device setting. The engineering account can only view and modify its own password.
Oper_1 & Oper_2	The operator user account, grnerally it can only view the configuration of the device, the logical picture, wiring diagram and the logical device component. In this section user can’t create and modify any of its configuration, such as moving the map element position and deleting port association etc.
Guest_1	Guest user account is only for visitors. In this section user have no rights to change or view any kind of configuration information.
Default	Default user account is only for visitors. In this section user have no rights to change or view any kind of configuration information.

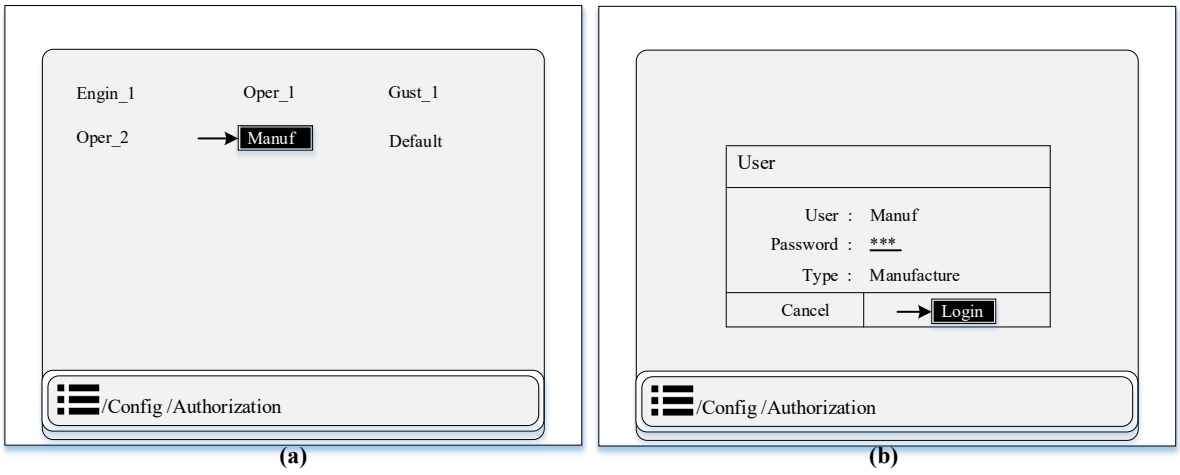


Figure 7.3.26 Diagram of Authorization User (a) Operator Selection List (b) Login or Cancel

7.3.8 Test Information

This section is divided into three sub-parts. In this section user can check the testing accuracy of relay like tripping test, operation test, warning test, status test and mandatory wave etc. The overview display diagram of test information is shown in below figure 7.3.27:

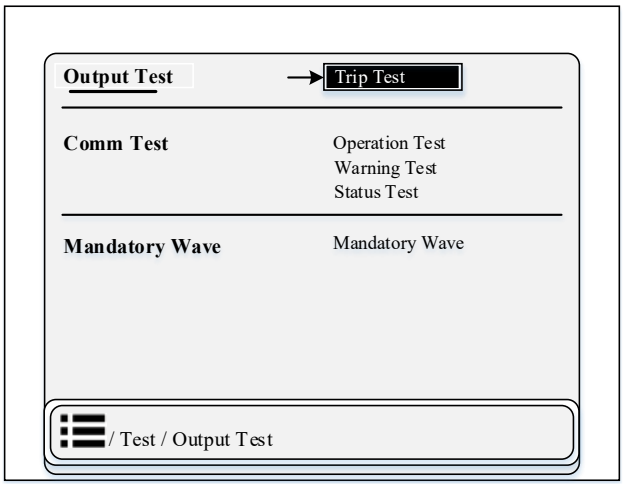


Figure 7.3.27 Overview Display of Test Information Sub-functions

7.3.8.1 Output Test

This section mainly realizes output test, including tripping test and signal test. See figure 7.3.27. User can access this function through the following path: “Test > Output Test”.

1- Trip Test

In this section user can simulate all kind of signal test like operation signal, alarm signal and trip signal, but the signal simulation can only be conducted when the IED is under maintenance. see below figure 7.3.28 :

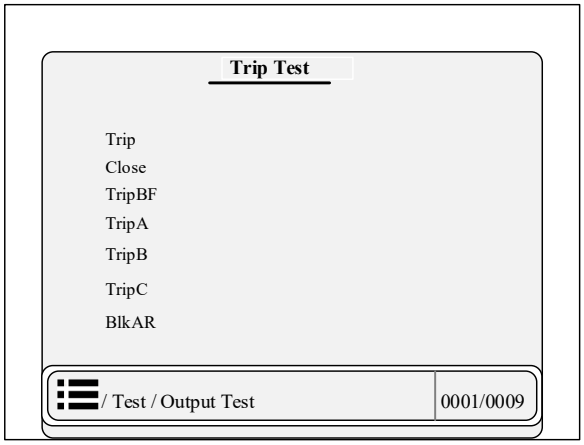


Figure 7.3.28 Overview Trip Test

7.3.8.2 Comm Test

Common test is divided into three sub-test like operation test, warning test and status test, etc. User can access this function through the following path: “Test > Comm Test”. The LCD overview display diagram of common test information of every tests is shown in below figure 7.3.29.

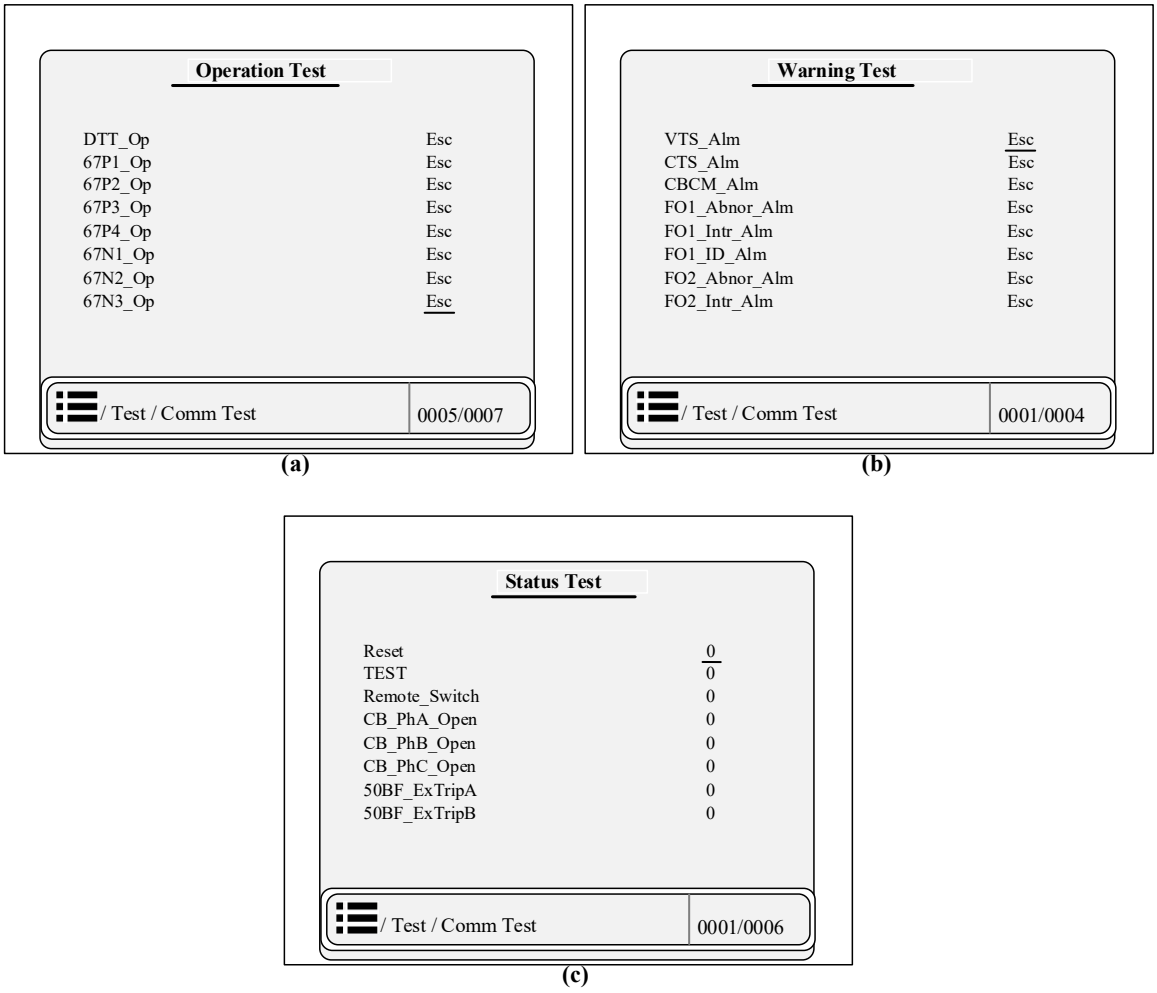


Figure 7.3.29 LCD Display Diagram of (a) Operation Test (b) Warning Test (c) Status Test

1- Operation Test

In this section user can simulate the protection operation event like DTT, 67P and 67N operation function etc. see above figure 7.3.29 (a):

2- Warning Test

In this section user can simulate the warning event like VTS alarm, CTS alarm and CBCM alarm etc. see above figure 7.3.29 (b):

3- Status Test

In this section user can simulate the BI changing status, like reset, TEST, and remote_Switch etc. see above figure 7.3.29 (c):

7.3.8.3 Mandatory Wave

In this section user can check the mandatory wave function. User can access this function through the following path: “Test > Mandatory wave”. After enter this section user can manually start disturbance recording in disturbance record section. See figure 7.3.27(Mandatory wave).

7.3.9 Clear Information

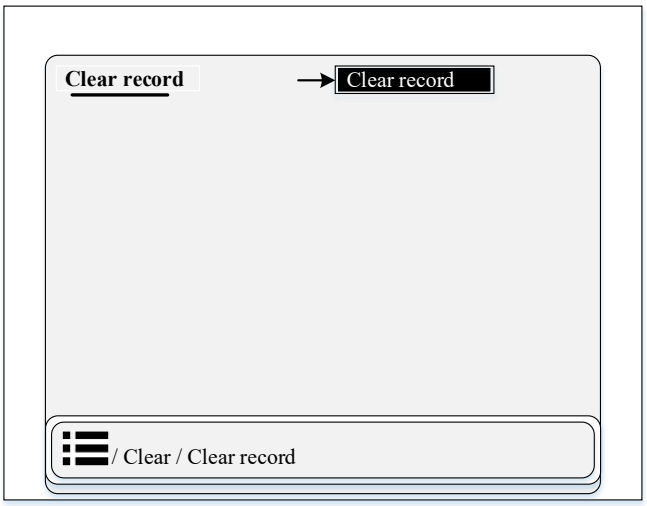


Figure 7.3.30 Overview Display of Clear Information Sub-functions

7.3.9.1 Clear record

In this section user can clear the record history of different functions like Alarm record, LED record and act record etc. User can access this function through the following path: “Clear > Clear record”. The clear record structure of LCD display is listed in below figure 7.3.31:

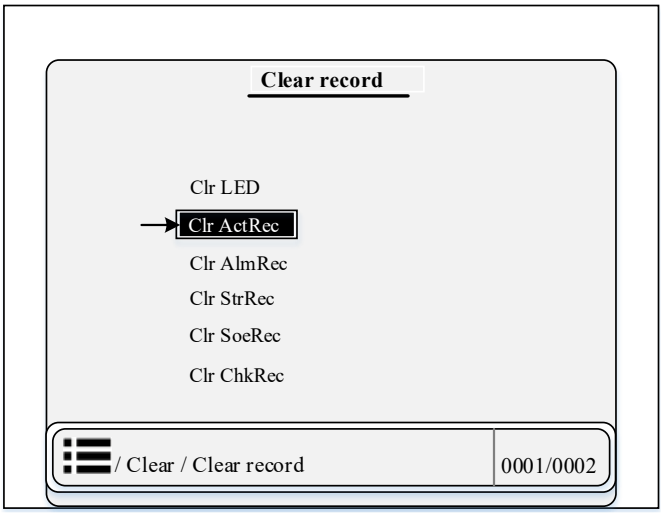


Figure 7.3.31 Diagram of Clear Record Display

7.3.10 Language Information

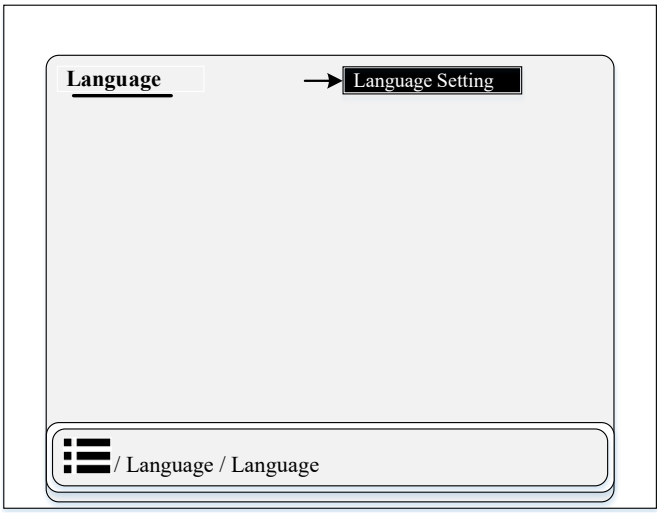


Figure 7.3.32 Overview Display of Language Information Sub-functions

7.3.10.1 Language Setting

In this section user can set the IED language according to their demand like Chinese, English, Spanish and Russian etc. User can access this function through the following path: “Language > Language setting”. The language setting diagram of relay is listed in below figure 7.3.33:

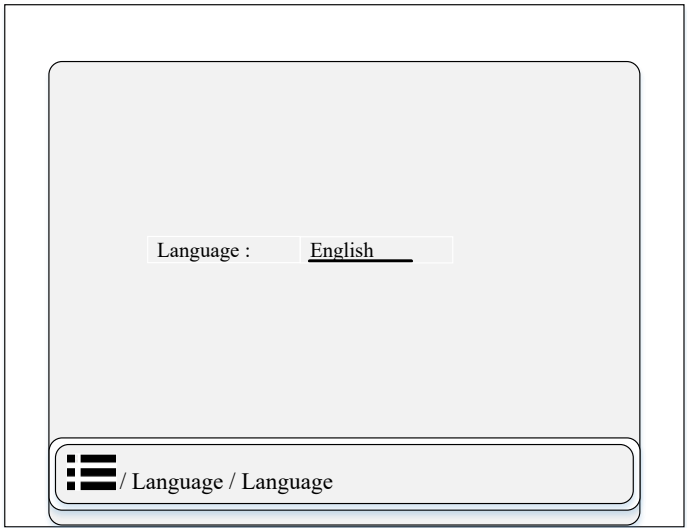


Figure 7.3.33 LCD Display diagram of Language Setting

8 Configurable Function

8.1 General Description

Each product has different configuration parameters according to the functions it has been designed to perform. There is a common methodology used across the entire product series to set these parameters.

The IED is equipped with flexible and powerful configuration functions, including the system configuration, the protection function configuration, the binary input configuration, the binary output configuration, the setting groups selection and the LED indicator configuration through the auxiliary software, which makes this IED meet various practical requirements.

8.2 PRS IED Studio Software

The PRS IED Studio software is developed in order to meet customer's demand on functions of the UAPC platform device, such as device configuration and programmable design. It selects substation as the core of data management and the device as fundamental unit, supporting one substation to supervise many devices.

The software provides two kinds of operation modes: on-line mode and off-line mode. The on-line mode supports the Ethernet connection with the device through the standard IEC60870-5-103 and can be capable of uploading and downloading the configuration files through Ethernet net. The relay parameters and status can be monitored while the device is connected, and the fault wave recording can read and analyzed. The off-line mode supports the off-line setting configuration, including protection logic programming, the binary input configuration, the binary output configuration and etc.

The software provides Online and Off-line comparison function, contain the setting and logic comparison. Online comparison can compare relay configuration and PC backup configuration. Off-line comparison can compare two devices off-line configuration.

8.3 Setting Group Selection

You can select the setting group using binary inputs. You can choose binary inputs through the configuration tool, different binary inputs correspond to different setting groups. You can set the setting group with binary inputs according to the following table:

Table 8.3.1 Recording Time Settings

BI_SETGRP1	setting group01
BI_SETGRP2	setting group02
BI_SETGRP3	setting group03
BI_SETGRP4	setting group04

The path to the configuration tool:

[IED]->[Logic]->[PLAT]->[PUB_SetVal].

8.4 Configuration File Introduction

8.4.1 Parameter-PUBLIC

8.4.1.1 Macro Set Functions and Parameters

Configuration location: [Parameter]-[PUBLIC]- [Macro Set]

This module is used to set the basic functions of the device, such as rated frequency, analog signal transmission type, PRP/HSR function disable and enable, device naming, etc.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
System_Frequency	Rated frequency (fn): 50/60Hz
If IEC850 Use Primary Value	FALSE: send with secondary values TRUE: send with primary values
NetMode_Stationbus	NORMAL: AB network enable PRP: PRP function enable HSR: HSR function enable
NetMode_Processbus1	NORMAL: AB network enable PRP: PRP function enable HSR: HSR function enable
NetMode_Processbus2	NORMAL: AB network enable PRP: PRP function enable HSR: HSR function enable
EquipName	Device name

8.4.1.2 Timing Mode Functions and Parameters

Configuration location: [Parameter]-[PUBLIC]- [Timing Mode]

This module is used to set up devices that support two synchronization methods simultaneously.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Timing Mode1	The device supports two timing methods: Timing Mode1 and Timing Mode2. Normally the first timing method Timing Mode1 is preferred for timing, while the second timing method Timing Mode2 is backup. When the first timing method is interrupted, it automatically switches to the second timing method.
Timing Mode2	

Configuration location: [Parameter]-[PUBLIC]- [Timing mode]-[Timing Mode1/Timing Mode2]

This module is a timing method supported by the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
SNTP	SNTP timing requires setting the IP address of the timing server on the corresponding timing component
IRIG-B	When checking the B code, it is necessary to set the electrical B or optical B code and verification method on the corresponding timing component
1588	1588 PTP timing requires setting a transparent clock (P2P or E2E) and receiving message network port on the corresponding timing component
None	No timing

8.4.1.3 SR76XX\SR73XX Module with Output Parameters

Configuration location: [Parameter]- [PUBLIC] -[SR76XX-XXIXXO] or [Parameter] -[PUBLIC] -[SR73XX-XXIXXO].

XXI means the XX binary input(BI), XXO means XX binary output(BO). SR76XX is power module with BOs, such as: SR7601_0I11O is with 11 BOs; SR73XX is module type with some or whole BOs, such as: SR7300_0I14O is with 14 BOs, SR7301_0I8O is 8 with BOs, SR7310_9I7O is 7 with BOs.

This module is for setting up the device output board.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Module NO.	The module number in the device
BOXX NO.	XX means the BO number. The NO. means the BO can be associated with output resources in the OUTPUT of the CONST node.
Relay State	The Relay State means maintain condition: Not Hold: the hardware BO is not maintained, it will reset when the associated output resources are reset when there is no fault. Hold: the hardware BO is maintained, it will reset when both the associated output resources and the Start signal are reset when there is no fault, the Start signal is default last for pulse time about 7s. Condition Hold: only used for OC with 79AR functions, when the 79AR reclosed several shots, only the last OC trip phase BO will be hold.

8.4.1.4 SR78X LED module Parameters

Configuration location: [Parameter]-[PUBLIC]-[SR780_32LED]

SR78X is an LED module with 32 LEDs. LED03 ~ LED21 are configurable for user.

This module is for setting up the device LED module.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
LEDXX NO.	XX means the LED number. The NO. means the LED can be associated with output resources in the OUTPUT of the CONST node.
Display State	Maintain the attribute, Not Hold is not held, and automatically extinguishes if the condition is not met; Hold is held, automatically held when illuminated; Conditional Hold is a condition held, and only a trip after the device coincides will extinguish the lights that do not meet the conditions
Color State	Select colors, green, yellow, and red are optional

8.4.1.5 SR73XX Input module parameters

Configuration location: [Parameter]-[PUBLIC]-[SR73XX-XXIXXO]

XXI means the XX binary input(BI), XXO means YY binary output(BO). SR73XX is module type with some or whole BIs, such as: SR7330_18I0O is with 18 BIs, SR7310_9I7O is 9 with BIs and 7BOs.

This module is for setting up the device input module.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
BIXX NO.	XX means the BI number. The NO. means the BI can be associated with input resources in the INPUT of the CONST node.
Debounce Time	Debouncing time setting, in milliseconds. If the input power is a DC power supply, the hard switch input debouncing time is usually set to 1000ms, the remote signal input debouncing time is usually set to 4ms, and the protection input debouncing time is usually set to 1ms; If the input power is AC power, the debouncing time is usually set to 6ms.
Pickup Voltage	Set the power supply voltage according to the actual situation

8.4.1.6 SR71XX Analog module parameters

Configuration location: [Parameter]-[PUBLIC]-[SR71XX]

SR71XX is an analog module with two configurations: 4U8I (4 sets of voltage and 8 sets of current) and 8U4I (8 sets of voltage and 4 sets of current).

This module is for setting up the device analog module.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
PTX Primary Rating Value	X means the ANA number. Associate PT with primary values, which can be associated with fixed value resources in SET under the CONST node
PTX Secondary Rating Value	X means the ANA number. Associate PT with secondary values, which can be associated with fixed value resources in SET under the CONST node
PTX NO.	X means the ANA number. Associate analog resources, which can be associated with analog resources in ANA under the CONST node
CTX Primary Rating Value	X means the ANA number. Associate CT with primary values, which can be associated with fixed value resources in SET under the CONST node
CTX Secondary Rating Value	X means the ANA number. Associate CT with secondary values, which can be associated with fixed value resources in SET under the CONST node.
CTX Index NO.	X means the ANA number. Associate analog resources, which can be associated with analog resources in ANA under the CONST node

8.4.1.7 User Functions and Parameters

Configuration location: [Parameter]-[PUBLIC]-[User]

This module is set for device login users.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
User Name	Login user name
User Type	Login user type
Password	Login user password

8.4.1.8 DNP_Para Functions and Parameters

When using the DNP protocol as the communication protocol, corresponding communication

parameters need to be set;

Configuration location: [Parameter]-[PUBLIC]-[DNP_Para]

This module is for setting the DNP parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
RetryTime	Number of retransmissions, default to 0. If there are no special requirements. The parameter can be set by default
Delay1	The retransmission interval 1, which is set to 0 by default. If there are no special requirements, the parameter can be set by default
Delay2	The retransmission interval 2, which is set to 0 by default. If there are no special requirements, the parameter can be set by default
Infinite	If the main station does not confirm whether to infinitely retransmit the flag, it defaults to 0. If there are no special requirements, the parameter can be set by default
FragSize	The application layer buffer size is set to 0 bytes by default
FlgLastConSet	Whether the last CON is set during multi frame transmission it defaults to 0. If there are no special requirements, the parameter can be set by default
TimeCycle	The DNP timing cycle is set to 0 by default. If there are no special requirements, the parameter can be set by default
IfUTCTime	Send with the UTC or local time flag. True: UTC, FALSE: local time, which defaults to FALSE and takes the local time
UNSEnable	The enable flag for non-request submission, Default setting is FALSE
BufferSizeSOE	Judgment mar of Buffer over Flow，Default setting is 0.
BufferSizeCOS	Judgment mar of Buffer over Flow，Default setting is 0.

8.4.1.9 Com_Para Functions and Parameters

Configuration location: [Parameter]-[PUBLIC]-[Com_Para_1/2/3]

This module is for setting the COM port parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
PortID	The port name corresponds to the hardware serial port
PortType	Port type, configure according to the type of serial port used
IfUsed	Whether to use, default to True
Protocol	Transport Protocol，default to UDP_INC_103

BaudRate	BAUD,default to 9600
DataBit	Data bits，default to 8
VerfMode	Parity verification type: None, Odd, Even, the default is None
StopBit	Stop bit,default to 1
MasterNo	Main Station Number, which is the address of the monitoring host or RTU, default to 1
StationNo	Substation number，for device address，default to 46

8.4.1.10 Net_Para Functions and Parameters

When using a network port communication protocol other than 61850 protocol, corresponding network port communication parameters need to be set.

Configuration location: [Parameter]-[PUBLIC]-[Net_Para_1/2/3/4/5/6]

This module is for setting the NET port parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
PortID	Monitoring physical network port selection, with NET_1, NET_2, and NET_3 corresponding to the three rear network ports of the CPU board
PortType	Port type, configure according to the type of serial port used
IfUsed	Whether to use, default to True
Protocol	Transport Protocol，default to UDP_INC_103
IfDblMac	Is it a dual MAC address, there is no concept of dual machine dual network in foreign countries, so the parameters related to the dual machine dual network concept do not need to be configured and can be kept as default
IfDblNet	Whether it is a dual network or not, there is no concept of dual machine dual network in foreign countries, so the parameters related to the dual machine dual network concept do not need to be configured and can be kept as default
NetPort	The monitoring number can be flexibly configured according to actual use
MasPortID	Host monitoring port selection, default to NET_A
SlaPortID	The selection of sub machine monitoring port defaults to NET-B
MonIP	Monitor the host IP and configure it according to actual usage needs, with a default value of 222.111.112.200
MonIP2	Monitor the host IP and configure it according to actual usage needs
SlaMonIP	Monitor the IP of the sub machine and configure it according to actual usage needs

SlaMonIP2	Monitor the IP of the sub machine and configure it according to actual usage needs
MasterNo	The main station number, which is the monitoring host or RTU address, defaults to 1
StationNo	The sub-station number is the device address, which defaults to 46

8.4.1.11 GOOSE_GOIN_DPCS Functions and Parameters

Configuration location: [Parameter]-[PUBLIC]-[GOOSE_GOIN_DPCS]

This module is used to set the GOOSE dual point signal parameters for the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
KIXXIndex	Composite dual point single point closing input signal, XX is the number
KIXXIndexDPS	Composite dual point single point opening input signal, XX is the number

Note: GOOSE_GOIN_DPCS need to be used in conjunction to synthesize GOOSE dual point inputs for device display.

8.4.2 Const

8.4.2.1 INPUT Functions and Parameters

Configuration location: [Const]-[INPUT]

This module is for setting the input parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Index	Resource sequence number
Name	Input Name
DNP Upload	Resource transmission method USE DNP: DNP protocol submission USE MMS: MMS protocol submission GOOSE IN: GOOSE input GOOSE OUT: GOOSE output STATION GOOSE: As a station goose PROCES BUS: As a process goose SV: Used as SV
Desc	Input Description

8.4.2.2 OUTPUT Functions and Parameters

Configuration location: [Const]-[OUTPUT]

This module is for setting the output parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Index	Resource sequence number
Name	Output Name
DNP Upload	Resource transmission method USE DNP: DNP protocol submission USE MMS: MMS protocol submission GOOSE IN: GOOSE input GOOSE OUT: GOOSE output STATION GOOSE: As a station goose PROCES BUS: As a process bus SV: Used as SV
Desc	Output Description

8.4.2.3 ANA Functions and Parameters

Configuration location: [Const]-[ANA]

This module is for setting the analog parameters of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Index	Resource sequence number
Unit	Analog quantity secondary value unit
KiloUnit	Analog quantity primary value unit
Name	Analog quantity name
Related Set	The primary rated value of analog quantity
TA Index	The secondary rated value of analog quantity
Desc	Analog quantity description

8.4.2.4 WAVANA Functions and Parameters

Configuration location: [Const]-[WAVANA]

This module is used to set the parameters for the analog recording of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Ana Number	Analog quantity number in waveform recording
Ana Channel	Analog channels in waveform recording

8.4.2.5 WAVAKI Functions and Parameters

Configuration location: [Const]-[WAVAKI]

The detail explanation of the data item description is as following:

Data item description	The detail explanation
StateCode	Number of input in waveform recording
SrcPinNO	Corresponding input in waveform recording

8.4.2.6 WAVAKO Functions and Parameters

Configuration location: [Const]-[WAVAKO]

This module sets the parameters for the recording output of the device.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
StateCode	Number issued in the recording
SrcPinNO	Corresponding output in waveform recording

8.4.2.7 ACTREC Functions and Parameters

Configuration location: [Const]-[ACTREC]

This module sets the parameters for device action events.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Index	Number issued in the recording
Name	Action Event Name
Desc	Action Event Description

8.4.2.8 ALMREC Functions and Parameters

Configuration location: [Const]-[ALMREC]

This module sets the parameters for device alarm events.

The detail explanation of the data item description is as following:

Data item description	The detail explanation
Index	Number issued in the recording
Name	Alarm Event Name
Desc	Alarm Event Description

8.4.2.9 WAVECFGBOOL Functions and Parameters

The device supports monitoring the exit sign output of a certain component as a WAVECFGBOOL, when a change in the flag is detected, it can be set as a wave start flag or a recording action flag. When monitoring the output of a component outlet on site, create a new WAVECFGBOOL in the component and modify the corresponding detection point parameters in WAVECFGBOOL under the CONST node.

Configuration location: [CONST]-[WAVECFGBOOL]-[WaveType/Name/Desc]

The detail explanation of the data item description is as following:

Data item description	The detail explanation
WaveType	Note: Recording type: TYPE_STR represents startup type, When the flag is set, it serves as the startup flag in recording. If there is only startup but not operation or action, the startup waveform file will be produced with type "_s". TYPE_ACT represents the type of action, and when the flag is set, it will be used as an action flag in the wave, if there are one or more operation or action, the action waveform file will be produced with type "_f". TYPE_NULL indicates other types, and the state of this type is normally monitored in "_s" or "_f" waveform recording file, but it will not trigger to product a new waveform recording file.
Name	The name of the disturbance wave signal.
Desc	The description of the disturbance wave signal.

Note: After creating the WAVECFGBOOL, the WaveType parameters must be set, otherwise the device will not run.

8.5 User login permissions

This module provides user login permissions.

Main Function Category	Function description	Super	Engineer	Operator
Create new users	Create new users with a lower level than the current user	Engineer, Operator	-	-
Change password	Change the login password	√	√	√
Right click dropdown menu for “New interval”	Creating a device through backup files	√	√	√
	Delete device group	√	√	√
Right click dropdown menu for "device"	Editing device: create, delete, copy	√	√	√
	Export backup files and driver files	√	√	-
Parameter	Edit parameters: New, Delete, Copy	√	-	-
	ANA module channel association	√	-	-
	IO module channel association, Module channel settings association, Renaming, Language, Timing method, IP address	√	√	-
Const	Edit interface resource properties (such as name, maximum, minimum, step size, setting value, etc.)	√	-	-
	Edit interface resource description	√	√	-
Logic	View logic diagram	√	√	√
	Renaming logical nodes, creating and editing subgraphs and properties, primitives, connections, signals, recording, etc.	√	√	-

Note: “√” means this function is available, and “-” means this function is not unavailable.

9 Communication Protocol

9.1 Overview

This chapter introduces the data communication and the corresponding hardware of the IEDs. The IED support a wide range of protocols via communication interface (RS-485 or Ethernet port). The protocols are of international standard for communication in substations and it can be selected by modifying the communication parameters.

Local communication with the IED via a computer is achievable through both the front and back Ethernet ports. Furthermore, remote communication with SCADA or the station gateway is also achievable by choosing the IEC60870-5-103, IEC61850, DNP3.0 communication protocol via RS485 or Ethernet port.

It should be noted that the descriptions contained within this chapter do not aim to fully detail the protocol itself. This section serves to describe the specific implementation of the protocol in the relay.

9.2 Rear Communication Interface

9.2.1 Ethernet Interface

This protective device can provide three rear Ethernet interfaces (optional) and they are unattached each other. Parameters of each Ethernet port can be configured in the menu.

9.2.1.1 Ethernet Standardized Communication Cable

It is recommended to use twisted screened eight-core cable as the communication cable. A picture is shown bellow.

Figure 9.2.1 Ethernet communication cable

9.2.1.2 Ethernet Communication protocol

Ethernet communication protocols are supported by the device including: IEC60870-5-103, PRP/HSR, DNP3.0, IEC61850 etc. For more details about these communication protocols, see the correlative standards.

9.3 Network Topology

9.3.1 Star Topology

Each equipment is connected with an exchanger via communication cable, and thereby it forms a star structure network. Dual-network is recommended in order to increase reliability. SCADA is also connected to the exchanger and will play a role of master station, so the every equipment which has been connected to the exchanger will play a role of slave unit.

9.3.2 PRP/HSR Topology

This network topoloty is supported by the device.

9.4 IEC61850 Protocol

9.4.1 Overview

The IEC 61850 standard is the result of years of work by electric utilities and vendors of electronic equipment to produce standardized communications systems. IEC 61850 is a series of standards describing client/server and peer-to-peer communications, substation design and configuration, testing, environmental and project standards. The complete set includes:

- IEC 61850-1: Introduction and overview
- IEC 61850-2: Glossary
- IEC 61850-3: General requirements
- IEC 61850-4: System and project management
- IEC 61850-5: Communications and requirements for functions and device models
- IEC 61850-6: Configuration description language for communication in electrical substations related to IEDs
- IEC 61850-7-1: Basic communication structure for substation and feeder equipment– Principles and models
- IEC 61850-7-2: Basic communication structure for substation and feeder equipment - Abstract communication service interface (ACSI)
- IEC 61850-7-3: Basic communication structure for substation and feeder equipment– Common data classes
- IEC 61850-7-4: Basic communication structure for substation and feeder equipment– Compatible logical node classes and data classes
- IEC 61850-8-1: Specific Communication Service Mapping (SCSM) – Mappings to MMS (ISO 9506-1 and ISO 9506-2) and to ISO/IEC 8802-3
- IEC 61850-9-1: Specific Communication Service Mapping (SCSM) – Sampled values over serial unidirectional multidrop point to point link
- IEC 61850-9-2: Specific Communication Service Mapping (SCSM) – Sampled values over

ISO/IEC 8802-3

- IEC 61850-10: Conformance testing

These documents can be obtained from the IEC (http://www.iec.ch). It is strongly recommended that all those involved with any IEC 61850 implementation obtain this document set.

9.4.2 Communication Profiles

The PRS-7000 series relay supports IEC 61850 server services over TCP/IP communication protocol stacks. The TCP/IP profile requires the PRS-7000 series to have an IP address to establish communications.

9.4.2.1 MMS protocol

IEC 61850 specifies the use of the Manufacturing Message Specification (MMS) at the upper (application) layer for transfer of real-time data. IEC 61850-7-2 abstract services and objects are mapped to actual MMS protocol services in IEC61850-8-1.

9.4.2.2 Client/server

The core ACSI defined by IEC 61850 is mapped to manufacturing message specifications (ISO 9506-1, ISO 9506-2). This is a connection-oriented type of communication. The connection is initiated by the client, and communication activity is controlled by the client.

The rules to map the ACSI services supported by PRS-7000 series units to the MMS are as shown in following table

Table 9-1 Mapping of ACSI to MMS service

ACSI		MMS
Server model	GetServerDirectory (read server directory)	GetNameList (read name list service)
Associate model	Associate (associate)	Initiate (initial service)
	Abort (abnormal abort)	Abort (abort service)
	Release (release)	Conclude (end service)
Logic device model	GetLogicalDeviceDirectory (read logic device directory)	GetNameList (read name list service)
Logic node model	GetLogicalNodeDirectory (read logic node directory)	GetNameList (read name list service)
	GetAllDataValues (read all data value)	Read (read service)
Data model	GetDataValues (read data value)	Read (read service)
	SetDataValues (set data value)	Write (write service)
	GetDataDirectory (define read data)	GetVariableAccessAttribute (read variable access attribute service)
	GetDataDefinition (read data directory)	GetVariableAccessAttribute (read variable access attribute

		service)
Data set model	GetDataSetValue (read data set value)	Read (read service)
	SetDataSetValue (set data set value)	Write (write service)
	CreateDataSet (establish data set)	DefineNamedVariableList (define named variable list service)
	DeleteDataSet (delete data set)	DeleteNamedVariableList (delete named variable list service)
	GetDataSetDirectory (read data set directory)	GetNamedVariableListAttribute (read named variable list attribute service)
Substituting model	SetDataValues (set data value)	Write (write service)
	GetDataValues (read data value)	Read (read service)
Setting group control block model	SelectActiveSG (select activating setting group)	Write (write service)
	SelectEditSG (select edit setting group)	Write (write service)
	SetSGValues (set setting group value)	Write (write service)
	ConfirmEditSGValues (confirm editting setting group value)	Write (write service)
	GetSGValues (read setting group value)	Read (read service)
	GetSGCBValues (read setting group control block value)	Read (read service)
Buffered report control block	Report (report)	InformationReport (information report)
	GetBRCBValues (read buffered report control block value)	Read (read service)
	SetBRCBValues (set buffered report control block value)	Write (write service)
Non-buffered report control block	Report (report)	InformationReport (information report)
	GetURCBValues (read non-buffered report control block value)	Read (read service)
	SetURCBValues (set non-buffered report control block value)	Write (write service)
Log control block model	GetLCBValues (read log control block value)	Read (read service)
	SetLCBValues (set log control block value)	Write (write service)
	QueryLogByTime (query log by time)	ReadJournal (read log service)
	QueryLogAfter (query log after)	ReadJournal (read log service)
	GetLogStatusValues (read log status values)	Read (read service)
GOOSE	GetGoCBValues (read GOOSE control block values)	Read (read service)
	SetGoCBValues (set GOOSE control block values)	Write (write service)
GSSE	GetGsCBValues (read GSSE control block values)	Read (read service)
	SetGsCBValues (set GSSE control block values)	Write (write service)
MSV	GetMSVCBValues (read MSV control block	Read (read service)

	values)	
	SetMSVCBValues (set MSV control block values)	Write (write service)
USV	GetUSVCBValues (read USV control block values)	Read (read service)
	SetUSVCBValues (set USV control block values)	Write (write service)
Control model	Select (select)	Read (read service)
	SelectWithValue (select with value)	Write (write service)
	Cancel (cancel)	Write (write service)
	Operate (operate)	Write (write service)
	CommandTermination (command termination)	InformationReport (information report)
	TimeActivatedOperate (time activated operation)	Write (write service)
File transmission model	GetFile (read file)	FileOpen, FileRead, FileClose (file open, file read and file close service sequence)
	SetFile (set file)	ObtainFile (obtain file service)
	DeleteFile (delete file)	FileDelete (file delete service)
	GetFileAttributeValues (read file attribute values)	FileAttributes (file attribute service)

9.4.2.3 Peer-to-peer

This is a non-connection-oriented, high speed type of communication usually between substation equipment, such as protection relays, intelligent terminal. GOOSE is the method of peer-to-peer communication.

9.4.2.4 Substation configuration language (SCL)

IEC 61850 has defined a series of configuration documents (ICD, IID, SCD, SED, CID), which are prepared with SCL (substation configuration language). The SCL includes the following:

Head: it is used to identify a SCL configuration document and its version, and also to designate relevant names into the mapping option of information (Function Name)

Substation: it is used to describe the function structure of the substation, and mark the primary devices and their electrical connection relationship.

IED: intelligent electronic device description, to describe the IED pre-configuration, access points, logic devices, logic nodes, data objects, etc.

DataTypeTemplate: the instantiated logic node type, and logic node type is a specific sample of logic node data.

The purpose to define and use SCL is: the description of intelligent electronic device capability and description of substation automation system can be exchanged in a compatible manner between the intelligent electronic device management tools and system configuration tools provided by different manufacturers.

9.4.2.5 GOOSE

GOOSE service is used to transmit fast messages, such as trip and switch position.

The GOOSE service adopts the pear-to-pear transmission, and is classified as GOOSE sending and GOOSE receiving.

9.4.2.6 GOOSE sending mechanism

GOCB is automatically enabled when the unit is powered on, when all status of the unit are determined, it performs sending according to the data set shifting mode, to quickly send the initial status of the own GOOSE information;

The time interval for immediate re-sending after shift of GOOSE message is the MinTime parameter (i.e. T1); the “timeAllowedtoLive” parameter in GOOSE message is 2 times the “MaxTime” configuration parameter (i.e. 2T0);

9.4.2.7 GOOSE receiving mechanism

The GOOSE receiving buffer zone of the unit receives the new GOOSE messages, after a strict check of the relevant parameters of GOOSE messages, the receiving side first compares if the StNum (status number) of the newly received frame and that in the GOOSE message of the previous frame are equal. If the StNum of the two frames of GOOSE messages are equal, the SqNum (sequence number) of the two frames of GOOSE messages are compared, if the SqNum of the newly received GOOSE frame is bigger than the SqNum of the previous frame, this GOOSE message is discarded, otherwise the data of the receiving side is updated. If the two GOOSE messages have different StNum, the data of the receiving side are updated;

When receiving GOOSE messages, the PRS-7000 series unit strictly checks if parameters such as AppID, GOID, GOCBRef, DataSet and ConfRev are matching;

In receiving GOOSE messages, it will take into account cases of communication interruption of fault with issuing unit, when the GOOSE communication is interrupted or the configured versions are not identical, the received GOOSE message should maintain the status before interruption.

9.4.3 Data set and control block

PRS-7000 series devices support real-time sending of data. The data objects requiring real-time monitoring are configured into data set, and the data set are associated to report control and GoCB, so that the change information of monitored objects can be sent in real-time to the background via the report service and GOOSE.

9.4.3.1 Data set

PRS-7000 series devices usually configure data sets in advance in the ICD document, such as protection event, protection digital input and protection measurement. The SCT (system configuration tool) can also add, delete and modify data set configuration according to the needs of existing actual projects.

A data set is an ObjectReference set of orderly DATA or DataAttrubutes. It usually include the following attributes:

- ldInst: the logic device containing the DATA or DataAttrubutes;
- lnClass: the logic node class containing the DATA or DataAttrubutes;
- lnInst: the logic node instant number containing the DATA or DataAttrubutes;
- Fc: all attributes of functional constraint required by DATA or DataAttrubutes;
- doName: name of DATA, or name belonging to the DataAttrubutes;
- daName: attribute name.

9.4.3.2 Report control block

IEC 61850 has defined the report control block, to describe how the changed information is actively submitted via report service when the data set members have changed. Report control blocks are classified into buffered report control block and non-buffered report control block. In case of communication interruption, the newly occurring event will still be stored as buffered report control block, otherwise, it is a non-buffered report control block.

The report control block performs the control of report submission via a series of attribute configurations. Specifically, it has the following important attributes:

RptID

The identity of report control block, globally unique within the scope of LD, if the RptID of the RCB is set by the client side as NULL, in the report submitted by device, RptID is full path.

OptFlds

The option fields OptFlds contained in the report. The PRS-7000 series device supports the following option fields:

- Bit 1: Sequence-number
  - Bit 2: Report-time-stamp
  - Bit 3: Reason-for-inclusion
  - Bit 4: Data-set-name
  - Bit 5: Data-reference
  - Bit 7: EntryID (for buffered reports only)
  - Bit 8: Conf-revision
- Bit 9: Segmentation

When an item is set as 1, the corresponding information will be embodied in the report.

DatSet

The name of the data set associated with the report control block and under the same LD. The members of this data set are monitored by this report control block.

BufTm

Buffer time, it is the buffer time internally prompted by the dchg (data change), qchg (quality change), and dupd (data updating) of the rcb, in ms, with missing value as 0, indicating not using the buffer time attribute, and the maximum value is 1h.

The timer is started when the first internal prompt arrives, after it is reached in timer, all event messages within the buffer time are packed into one report, and submitted to the client side.

When the second change of the same signal arrives in the buffer time, the buffered report is submitted immediately, and the timer is booted again, to start again the subsequent internal prompt buffer.

TrgOps

Trigger option, used to filter the conditions for sending reports. PRS-7000 supports the following trigger options:

- *Bit 1:* Data change
- Bit 2: Quality change
- Bit 3: Data updating (the service follow-up of Ed2)
- Bit 4: Completeness period
- Bit 5: Total call

IntgPd

Completeness period time, to be set by the client side. After successful device enabling (RptEna = TRUE), the timer is started immediately, and after the expiration of completeness period time, the current values of all members in the data set associated by the report are packed and submitted.

The completeness period time set as 0 means the completeness submission function is not enabled.

GI

Total call is launched by the client side with initiative. After the report is enabled, the client side takes initiative to issue GI = TRUE, then the device immediately submit all data values in the current data set.

PurgeBuf

Purge buffer. When the client side sets PurgeBuf = TRUE, all report entries in the IED buffer report are purged.

When the client side modifies RptID, DataSet, BufTime, TrgOps, IntgPd, the device will automatically set purging buffer reports, equivalent to setting PurgeBuf = TRUE.

9.4.3.3 GOOSE control block

The fast messages of the PRS-7000 series device is transmitted via GOOSE, and the transmission characteristics of GOOSE is controlled by the GOOSE control block (GoCB). GoCB has the following important characteristics:

App ID

The application ID, representing the logic device where the GoCB is located. The missing value of App ID is the Object Reference of GoCB.

DatSet

The values of members of the data set associated by GoCB are transmitted by GOOSE.

9.4.4 Logic nodes and data modeling

9.4.4.1 Logic nodes

IEC 61850 7-4 has defined a series of logic nodes, which constitute the minimum communication unit of intelligent electronic devices as classified by functions. There are three types of logic nodes used by the PRS-7000 series unit: management logic nodes (LLN0), physical device logic nodes (LPHD) and application function logic nodes.

LLN0

Management logic nodes provide the management and control functions for all logic nodes and data objects within the logic devices. Some common services are modeled in LLN0, such as setting group control block (SGCB), GOOSE control block (GoCB), SV control block (MsvCB), reported control block (BRCB and URCB) and log control block (LCB); some common data objects are modeled in this node, such as Loc, to represent the local and remote operation enabling of the unit, and the based function VEBI and common settings; some data objects represent the meaning of the whole logic device, such as Beh, it is jointly formed by the Beh value of all logic nodes in the logic device, to represent the behavior and status of the whole logic device.

LPHD

It represents the information of physical devices, including the device manufacturer, unit model, software version, unit serial No., if it has an agency and the device health status. In this logic node, it is also extended to include device information such as name of protected device and unit time calibration method.

Application function logic nodes

Application function logic nodes include when classified by functions:

A: automatic control logic nodes

C: monitoring related logic nodes, such as CSWI

G: general purpose function logic nodes, such as GGIO, GAPC

I: filing related logic nodes,

M: measurement and metering related logic nodes, such as MMXU

P: protection function logic nodes, such as PDIF, PDIS, PTOC, PTRC

R: protection related functional logic nodes, such as RREC, RBRF

S: sensors, monitoring

T: instrument transducer logic nodes, such as TVTR, TCTR

X: switching device logic nodes, such as XCBR, XSWI

Y: power transformer and related function logic nodes

PRS-7000 series unit uses the corresponding logic nodes according to the functions selected by user. For the corresponding logic nodes, please refer to the instruction manual for unit of the specific model.

9.4.4.2 Data object

IEC 61850 7-3 defined common data types, including:

- Status information: such as SPS, INS, ACT, ACD
- Measured value information: such as MV, CMV, WYE
- Controllable status information: such as SPC, INC, DPC
- Status set values: such as SPG, ING
- Analog set values: such as ASG
- Description information: such as LPL, DPL

The PRS-7000 series unit uses the above common data types, and instantiate the specific data objects according to the need of application functions, to meet the need of application functions. There are the following common data objects in all logic nodes (except for LPHD):

Mod

The model of logic node. It represents the behavior mode of the logic node, such as normal, testing and blocked.

Beh

The performance of the logic node, representing the current performance status of the logic node, the value of the same Mod is read-only and cannot be modified.

Health

Health status, it reflects the status of the relevant software and hardware of the logic node.

NamPlt

The name plate of the logic node

9.5 DNP3.0 Protocol

9.5.1 Overview

The descriptions given here are intended to accompany this relay. The DNP3.0 protocol is not described here; please refer to the DNP3.0 protocol standard for the details about the DNP3.0 implementation. This manual only specifies which objects, variations and qualifiers are supported in this relay, and also specifies what data is available from this relay via DNP3.0.

The DNP3.0 communication uses the Ethernet ports (electrical or optical) at the rear side of this relay.

9.5.2 Link Layer Functions

Please see the DNP3.0 protocol standard for the details about the linker layer functions.

9.5.3 Transport Functions

Please see the DNP3.0 protocol standard for the details about the transport functions.

9.5.4 Application Layer Functions

9.5.4.1 Function Code

Table 9-2 Function Code

Function Code	Function
0 (0x00)	Confirm
1 (0x01)	Read
2 (0x02)	Write
3 (0x03)	Select
4 (0x04)	Operate
5 (0x05)	Direct Operate
6 (0x06)	Direct Operate No Acknowledgment
13 (0x0D)	Cold Restart
14 (0x0E)	Warm Restart
20 (0x14)	Enable Unsolicited Responses
21 (0x15)	Disable Unsolicited Responses
22 (0x16)	Assign Class
23 (0x17)	Delay Measurement

9.5.4.2 Communication Table Configuration

This relay now supports 3 Ethernet clients and 2 serial port clients. Each client can be set the DNP related communication parameters respectively and be selected the user-defined communication table.

The user can configure the user-defined communication table through the PRS IED Studio configuration tool auxiliary software. The object groups “Binary Input”, “Binary Output”, “Analog

Input" and "Analog Output" can be configured according to the practical engineering demand.

9.5.4.3 Analog Input and Output Configuration

To the analog inputs, the attributes "deadband" and "factor" of each analog input can be configured independently. To the analog outputs, only the attribute "factor" of each analog output needs to be configured. If the integer mode is adopted for the data formats of analog values (to "Analog Input", "Object Variation" is 1, 2 and 3; to "Analog Output", "Object Variation" is 1 and 2.), the analog values will be multiplied by the "factor" respectively to ensure their accuracy. And if the float mode is adopted for the data formats of analog values, the actual float analog values will be sent directly.

The judgment method of the analog input change is as below: Calculate the difference between the current new value and the stored history value and make the difference value multiply by the "factor", then compare the result with the "deadband" value. If the result is greater than the "deadband" value, then an event message of corresponding analog input change will be created. In normal communication process, the master can online read or modify a "deadband" value by reading or modifying the variation in "Group34".

9.5.4.4 Binary Output Configuration

The remote control signals, logic links and external extended output commands can be configured into the "Binary Output" group.

To an extended output command, if a selected command is controlled remotely, this command point will output a high ~ level pulse. The pulse width can be decided by the "On ~ time" in the related "Binary Command" which is from the DNP3.0 master. If the "On ~ time" is set as "0", the default pulse width is 500ms.

9.5.4.5 Class Configuration

If the DNP3.0 master calls the Class0 data, this relay will transmit all actual values of the "Analog Input", "Binary Input" and "Analog Output". The classes of the "Analog Input" and "Binary Input" can be defined by modifying relevant settings. In communication process, the DNP3.0 master can online modify the class of an "Analog Input" or a "Binary Input" through "Function Code 22" (Assign Class).

9.6 IEEE 1588-2008 Protocol

9.6.1 Overview

The Precision Time Protocol (PTP) is a protocol used to synchronize clocks throughout LAN. On a local area network, it achieves clock accuracy in the sub-microsecond range, making it suitable for measurement and control systems.

9.6.2 Time Synchronization

Time synchronization of the device support IEEE 1588-2008 Protocol via ethernet interface or optical interface.

10 Commissioning

10.1 General

This part contains a brief description about how to verify the function, including functional verification items, functional verification methods and more.

With high degree of self-checking, any fault with the internal hardware and software can be diagnosed by the device itself. So for the commissioning, only hardware interface and the application-specific software function are necessary to verify.

Before carrying out commissioning, users should pay close attention to the safety, technical data and the ratings on the front panel label.

10.2 Safety Instructions

This section contains some safety information, some of which are given warning signs to avoid personal injury or equipment damage, to prompt the user to be careful.

10.2.1 Safety Identification


Electrical warning icon indicating a danger of electric shock.


Notice icon, indicating important information or warnings involved in the article. This icon may indicate a danger of software, equipment or property damage.


Information icons alert readers to important facts or conditions.


Prompt staff not to forget the dangers of static electricity and make prevention.


Forbid to energize the device while not grounded, to avoid endangering the personal safety due to electrical insulation damage!

Although these markings warn of the danger, it is important to note that operating damaged equipment under certain operating conditions can result in reduced process performance and may result in death or personal injury. Therefore, be sure to fully comply with all warnings and cautions.

10.2.2 Safety Identification Examples

For the various safety instructions given in the previous section, the following are examples

10.2.2.1 Warning Signs


Do not touch the circuit during operation. There may be fatal voltage and current. Strict compliance with safety regulations. Work in high voltage environment need to be serious to avoid personal injury or equipment damage.


When measuring signals in an open circuit, remember to use a properly isolated test clamp that can have fatal voltages and currents.


During normal operation, never disconnect or connect the wires or connectors connected with the terminals. It may cause deadly dangerous voltage and current, may also interrupt the operation of the equipment, damage the terminals and the measuring circuit.


Never disconnect the secondary winding of the current transformer. Current transformers that operate when the secondary windings are open will create strong potentials that may damage the transformers and may cause personal injury.


When the protective device is energized, never plug the module. Hot plug may damage the protection device and measuring circuit, may also result in injury.

10.2.2.2 Caution Signs

Do not connect the protective shell to the live wire, charging the shell may damage the internal circuit.


During installation and commissioning, be careful not to get an electric shock if you touch the leads and connecting terminals

10.2.2.3 Notice Signs


Do not modify the settings in the running protection device. After modify the setting, verify it according to the rules.

10.2.2.4 Anti-static Signs


Remember to avoid touching circuits, including electronic circuits, and the device may be damaged if subjected to static electricity. Electronic circuits may also contain deadly high voltages.


Remember to use a certified conductive bag when transporting the module. Remember to connect the anti-static wristband to the ground when handling the module and remember to operate it on a suitable anti-static surface. Static electricity discharge may cause damage to the module.


Remember to wear the anti-static wristband connected to the ground when replace the module, Static electricity discharge may damage the module and protection device.

10.2.2.5 Earthing Signs


Regardless of operating conditions, remember to connect the protective device to the earth, also needed for special occasions such as testing, demonstrating and off-line configuration on the desk. Operation of the protective device without proper earthing may damage the protective device and the measuring circuit and may also cause an injuring accident.

10.2.2.6 Information Signs

Effective value and step of settings explanation: The protection setting supports as much as 6 significant figures, of which the decimal point occupies one digit (the highest digit can not be a decimal point). The minimum setting step is 0.01.

10.3 Commission Tools

10.3.1 Instrumentation and Meters Notice:

- Instruments, meters must pass the inspection, and within the validity of the inspection
- instruments, meters should be accurate level higher than the seized equipment related indicators 2 to 4 levels.

10.3.2 Tools Requirement:

- Relay protection testing devices: Multifunctional dynamic current and voltage injection test set with interval timer.
- Regulative DC power: DC output can be adjustable within 0 ~ 240V.
- Accuracy meter: support three-phase voltage, three-phase current output.
- Tong-type ammeter
- Multifunction phase meter
- Multimeter
- Megger
- Laptop: with appropriate software
- Network cable
- Optical power meter
- EIA RS-485 to EIA RS-232 converter

10.4 Commission Preparation

10.4.1 Basic Knowledge

When commissioning this device for the first time, sufficient time should be allowed to become familiar with the manual to understand the basic operation, protection principles, and related basic performance of the devices as much as possible. If find any doubt in the process, consult the manufacturer's field service personnel or technical support staff of our company.

Alternatively, if a laptop is available together with suitable setting software (such as PRS IED Studio software), the menu can be viewed one page at a time to display a full column of data and text. This PC software also allows settings to be entered more easily, saved to a file on disk for future reference or printed to produce a setting record. Refer to the PRS IED Studio Instruction manual

for details.

If the application-specific settings have been applied to the relay prior to commissioning, it is advisable to make a copy of the settings so as to allow them restoration later. This could be done by extracting the settings from the relay itself via printer or manually creating a setting record.

10.4.2 Operation Preparation

Check the printer wiring is normal, the print paper is ample, in order to print the test settings, version, and a variety of experiment data.

Attention! The device should be checked before power on. The appearance should be no damage. The module is plugged and fastened, and the insulation of the DC voltage circuit meets the specified requirements. The indicators can refer to the commissioning record of the device.

Attention! Disconnect the external AC circuit of the cubicle before the test to avoid causing a safety accident, which will cause serious damage to the construction workers on site.

Attention! When you need to plug and unplug the device module, you should ensure the device is powered off and make the anti-static measures to prevent the module damage or performance degradation.

Attention! Temporarily open or shorted terminals should be well documented for reliable recovery after the end of the test.

If it has been necessary to disconnect any of the external wiring from the protection in order to perform any of the following tests, it should be ensured that all connections are replaced in accordance with the relevant external connection or scheme diagram. Confirm current and voltage transformer wiring.

10.5 Product Checks

These product checks cover all aspects of the relay which should be checked to ensure that it has not been physically damaged prior to commissioning, is functioning correctly and all input quantity measurements are within the stated tolerances.

10.5.1 Document Check

Document acceptance check include: protection inspection and factory test reports, certificates, drawings, technical manual of related equipment.

10.5.2 Appearance Inspection

Check the the front and back of the cubicle of various electrical components, terminal blocks, hard-switch. All should be marked with the number, name, application and operating position. The marked handwriting should be clear, neat, and not easy to bleach.

The device mark inspection shall include the product type, name, manufacturer's name and trademark, date of manufacture and serial number, safety mark, etc., the mark and installation location shall be consistent with the design drawings.

Inspect the surface of the device. There shall not be scratches, bumps, groove marks, rust, deformation and other defects that affect the quality and appearance;

Check the device panel keyboard is complete, flexible operation, the LCD is clear, the indicator shows normal;

Uncharged metal part of the device should be connected as one, and reliable grounding;

Check the cubicle shell of the device must be grounded reliably;

10.5.3 Insulation Check

Disconnect the weak electric link with other devices and short circuit the AC voltage circuit terminal, AC current circuit terminal, DC circuit terminal and signal circuit terminal inside the cubicle terminal block, and measure the insulation resistance value using the tester whose open circuit voltage is 500V. Insulation should meet the following requirements:

Device independent circuit and exposed conductive parts, 500V megger insulation resistance measured value should be no less than 100MΩ;

Between electrically disconnected independent circuits, 500V megger insulation resistance measured value should be no less than 100MΩ;

After the insulation test is completed, make sure that all external wiring is properly connected.

10.5.4 External Wiring Check

External protection wiring should be consistent with the design drawings; Internal and external wiring on the terminal block and cable marking on it is correct, complete, and consistent with the drawings; Secondary circuit wiring should be neat and beautiful, solid and reliable;

All secondary cables and terminal blocks wiring connection should be solid. Cable mark should be complete, correct and clear;

The correct mark should be attached to the optical fiber (including optical cable, pigtail, jumper) and both ends of the device port. Such fiber-optic annotation should include the optical fiber number, destination. The starting point of the fiber should indicate the cubicle number. The content of the port mark should include the port number and destination. The starting point of the port should include the cubicle number, switch number and port number.

10.5.5 Test Category

The following tests are necessary to ensure the normal operation of the equipment before it is first put into service.

These tests are performed for the following hardware to ensure that there is no hardware defect. Defects of hardware circuits other than the following can be detected by self-monitoring when the power supply is energized.

- User interfaces test
- Binary input circuits and output circuits test

- AC input circuits test
- Function tests

These tests are performed for the following functions that are fully software-based. Tests of the protection schemes and fault locator require a dynamic test set.

- Measuring elements test
- Timers test
- Metering and recording test
- Conjunctive tests

The tests are performed after the relay is connected with the primary equipment and other external equipment.

- On load test.
- Phase sequence check and polarity check.

10.6 With the Relay Energized

Check that the input range of the external power supply should meet the power requirements of the "technical data" section within the permissible power supply input voltage range.

Attention! All external circuits connected to the unit must be checked to ensure correct installation before the unit is powered on or the test procedure started.

10.6.1 LCD Display Check

After the device is powered on, the LCD will be lit. After the device is initialized, if the device is in normal operation, the LCD displays the status of the main single line diagram.

Attention! If the device is in the alarm state after power-on, the LCD displays the alarm status information. At this point you can refer to the "Supervision" section to analyze the cause of the alarm and treatment.

10.6.2 Date and Time

If the time and date is not being maintained by substation automation system, the date and time should be set manually.

Set the date and time to the correct local time and date using menu item “Clock”.

For devices using IRIG-B (DC) time code and SNTP, IEEE 1588 time synchronization, you can verify the timing accuracy by modifying the clock setting of the device. For PPM, PPS time synchronization system, through the time synchronization binary input check.

10.6.3 Light Emitting Diodes (LEDs)

The device has two lights that can not be defined. the two lights are as follows:

"Healthy": indicates that the device is in normal operation, no software, hardware failure. When the

"healthy" light goes out, it indicates a serious problem with the device, resulting in the device not functioning properly.

"Alarm": indicates that there are some alarm events on the device. On this condition, you can analyze the cause of the alarm and how to handle it by checking the "supervision" section of the manual.

The rest of the indicators are configurable indicators.

If the indicator of the device is set to the self-retaining state, if the signal is not reset before the latest power-off, the signal will continue to be triggered when the device is powered on again, and the indicator can be reset by resetting operation. It is likely that alarms related to voltage transformer supervision will not reset at this stage.

10.6.3.1 Test the HEALTHY and ALARM LEDs

Apply the rated power supply and check that the “HEALTHY” LED is lighting in green. We need to emphasize that the “HEALTHY” LED is always lighting in operation course except that this device finds serious errors in it.

Produce one of the abnormal conditions listed in Chapter 4, the “ALARM” LED will light in yellow. When abnormal condition reset, the “ALARM” LED extinguishes.

10.6.3.2 Test the Other LEDs

Test the other LEDs according to the configuration of the LEDs (through the PRS IED Studio software). If the conditions which can turn on the selected LED are satisfied, the selected LED will be on.

10.6.4 Test the AC Current Circuit

Attention! The wiring must be checked in strict accordance with the AC current connection drawings provided.

The purpose of this test is to check whether the wiring of the AC circuit in the cubicle is correct and whether the sampling precision meets the requirements. The sampling accuracy and polarity of the device can be checked through sourcing rated AC current at the AC current input terminal on the back of the cubicle .

Protection current measurement accuracy requirement shall follow Measurement Range and Accuracy. However an additional allowance must be made for the accuracy of the test equipment being used.

Apply current equal to the current transformer secondary winding rating to each currenttransformer input in turn, see the following table, checking the magnitude using a multimeter/test set readout. The corresponding reading can then be checked in the relays menu.

10.6.5 Test the AC Voltage Inputs

Attention! The wiring must be checked in strict accordance with the AC voltage connection drawings provided.

The purpose of this test is to check whether the wiring of the AC voltage in the cubicle is correct and whether the sampling precision meets the requirements. The sampling accuracy and polarity of the device can be checked through sourcing rated AC voltage at the AC voltage input terminal on the back of the cubicle .

Protection voltage measurement accuracy requirement shall follow Measurement Range and Accuracy. However an additional allowance must be made for the accuracy of the test equipment being used.

Apply voltage equal to the voltage transformer secondary winding rating to each voltagetransformer input in turn, see the following table, checking the magnitude using a multimeter/test set readout. The corresponding reading can then be checked in the relays menu.

10.6.6 Test the Binary Inputs

The purpose of this test is to check whether the connection of binary input circuit is correct. During the test, the voltage applied to the binary input terminal must be within the allowable operating range.

Each binary input status can be checked by the device LCD panel, and the status "1" indicates that the binary input has been applied with an input voltage, and the opening status becomes "0" when the input voltage disappears.

10.6.7 Test the Binary Onputs

The purpose of this test is to check whether the binary output circuit connection is correct. According to the protection logic of the device and various kinds of signal output logic, stimulate a fault condition. The corresponding relay contact of the device shall be operated with the corresponding action or alarm signal.

10.6.8 Protection Function Checks

The purpose of this experiment is to verify the correctness of the protection logic. Protection function tests generally include the following types:

- Impedance protection test
- Current protection test
- Voltage protection test
- Frequence protection test
- Secondary system supervision function test

For details on how to implement the protection logic function, refer to "Operation Theory"

10.6.9 On-load Checks

The objectives of the on-load checks are:

- Confirm the external wiring to the current and voltage inputs is correct.
- Measure the magnitude of on-load current and voltage (if applicable).

- Check the polarity of each current transformer.

10.6.10 Final Checks

After the above tests are completed, remove all test or temporary shorting leads, etc. Restore the original correct wiring. Tighten the secondary circuit terminals, especially for the current terminals, circuit breaker closing and opening, operating power supply circuit.

If a test block is installed, remove the test plug and replace the cover so that the protection is put into service.

Ensure that all event records, fault records, disturbance records and alarms have been cleared and LED’s has been reset before leaving the protection.

Ensure that the protection has been restored to service.

11 Installation

11.1 General

Design and installation chapter is suit for design, installation, commissioning and maintenance staff. Designers must have a wealth of experience in electrical design. The installer must have the basic knowledge of electronic equipment and cubicle drawing reading. Commissioning and maintenance personnel must have extensive experience in operating protective equipment and test equipment. The equipment must be shipped, stored and installed with the greatest care.

Choose the place of installation such that the communication interface and the controls on the front of the device are easily accessible.

Air must circulate freely around the equipment. Observe all the requirements regarding place of installation and ambient conditions given in this instruction manual.

Take care that the external wiring is properly brought into the equipment and terminated correctly and pay special attention to grounding. Strictly observe the corresponding guidelines contained in this section.

11.2 Safety Instructions

Warning! Only insert or withdraw a module while the device power supply is switched off. To this end, disconnect the power supply cable that connects with the power supply module.

Attention! A module can only be inserted in the reserved slot. Components can be damaged or destroyed by inserting module in a wrong slot.

The basic precautions to guard against electrostatic discharge are as follows:

- Should boards have to be removed from this relay installed in a grounded cubicle in an HV switchgear installation, please discharge yourself by touching station ground (the cubicle) beforehand.
- Only hold electronic boards at the edges, taking care not to touch the components.
- Only works on boards that have been removed from the cubicle on a workbench designed for electronic equipment and wear a grounded wristband.
- Always store and ship the electronic boards in their original packing. Place electronic parts in electrostatic screened packing materials.

11.3 Checking the Shipment

Vehicles, trains, ships and all other means of transport are available, but to prevent snow and rain, shock, impact and collision, to ensure product packaging integrity.

Check that the consignment is complete immediately upon receipt. Notify the nearest CYG SUNRI CO., LTD. Company or agent, should departures from the delivery note, the shipping papers or the order be found.

Visually inspect all the material when unpacking it. When there is evidence of transport damage, lodge a claim immediately in writing with the last carrier and notify the nearest CYG SUNRI CO., LTD.Company or agent.

- **Unpacking and checking procedures**

1. Remove the shipping package.
2. Before unpacking, you should first check the equipment packaging intact, whether there are signs of serious collision and phenomenons that equipment in the box may be damaged. If found abnormal, it is recommended to take pictures as a record, confirm and contact with the manufacturer at first time.
3. When unpacking, you should use a claw, and pull out the nails, and then pry off the box lid; If the crowbar is used, never take the device as a fulcrum, and it is forbidden to stick into the wooden box carelessly with the crowbar. Open the box with the greatest care and avoid excessive vibration.
4. Check the appearance of the device is intact.
5. Check the delivery list. Check the device certificate of competency, supporting documents, attachments, spare parts, etc. are consistent with the order requirements, whether the packing list and the type, name, quantity, etc. are consistent and complete. If correct, sign the confirmation.
6. Manufacturer documents and spare parts should be assigned to personal keeping and registration.
7. If any abnormalities occur during unpacking, feedback CYG SUNRI CO., LTD. Company or agent at the first time, so as to avoid the follow-up of unclear responsibilities.

If the equipment is not going to be installed and commissioned immediately, store all the parts in their original packing in a clean dry place and keep air circulation. And to prevent the intrusion of various harmful gases, non-corrosive items stored in the same place.

11.4 Material and Tools Required

The necessary mounting kits will be provided, including screws, pincers and assembly instructions.

A suitable drill and spanners are required to secure the cubicles to the floor using the plugs provided (if this relay is mounted in cubicles).

11.5 Device Location and Ambient Conditions

The mechanical and electrical environmental conditions at the installation site must comply with the requirements of "Chapter 2 Technical Data". Avoid adverse conditions caused by the environment:

- Avoid installing in wet, dark and other places likely to cause damp and rust. If in unavoidable rainy area, install the device in a higher position;
- If the area is an earthquake prone area, fix the protection device tightly;
- If there is a lot of dust in the installation place, clean it before installing.

The place of installation should permit easy access especially to front of the device, i.e. to the human machine interface of the equipment. There should also be free access at the rear of the equipment for additions and replacement of electronic boards.

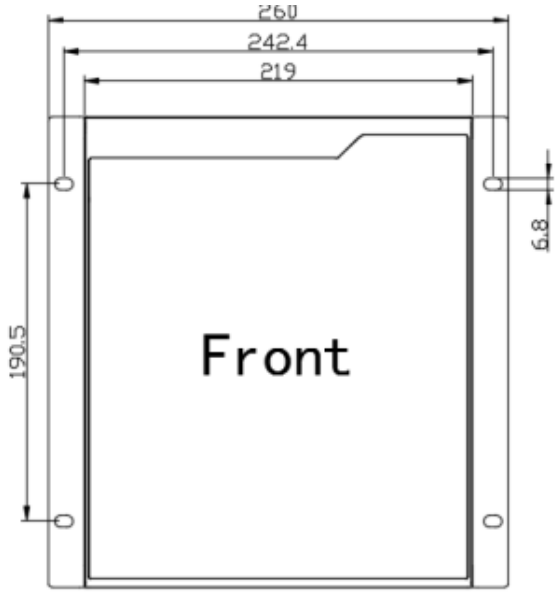
11.6 Mechanical Installation

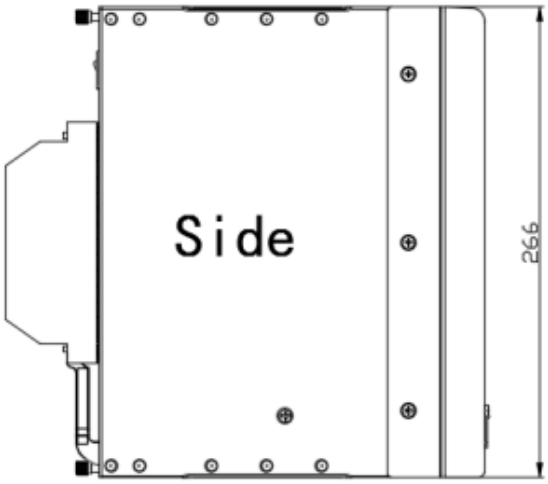
In the case of equipment supplied in cubicles, place the cubicles on the foundations that have been prepared. Take care while doing so not to jam or otherwise damage any of the cables that have already been installed. Secure the cubicles to the foundations.

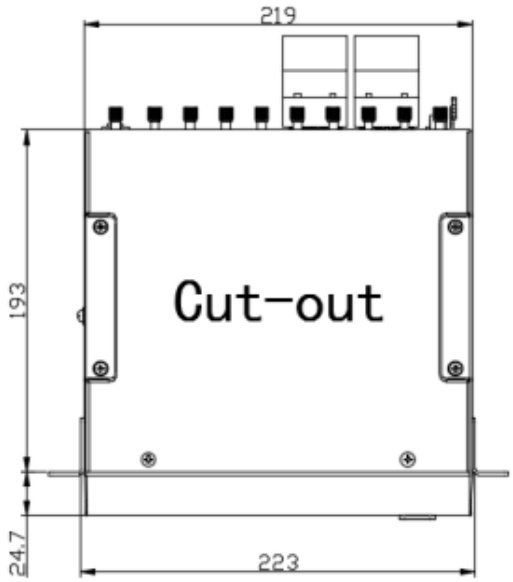
The device should be firmly fixed in the cubicle(cabinet), and the connecting screws should be tightened. The grounding wire of each device should be connected with the copper grounding busbar inside the cubicle, and reliably connected with the secondary grounding network. Device wiring should be consistent with the wiring diagram requirements.

The device features a 6U height, 1/1 19 "or 1/2 19" width chassis, integral panel and pluggable functional modules with lock. The device is designed conforming to IEC 60297-3. Embedded Installation as a whole, rear wiring. The current/ voltage connector structure are in the same size, and can be expanded, combined flexibly. Installation hole size as below.

Attention! It is necessary to leave enough space top and bottom of the cut-out in the cubicle for heat emission of this relay.


260
242.4
219
6.8
190.5
Front


Side
266


219
193
Cut-out
24.7
223

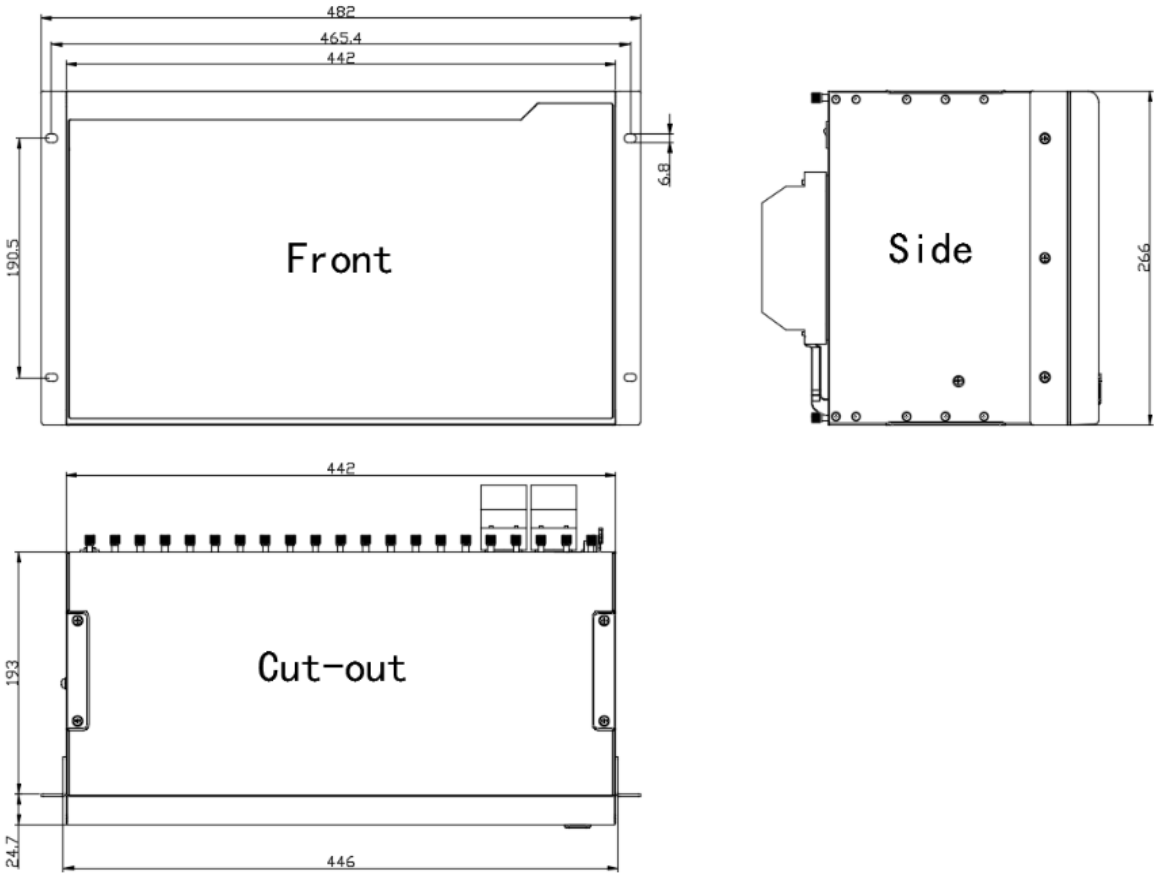


Figure 11.6.1 Dimensions of this relay and the cut-out in the cubicle (unit: mm)

11.7 Electrical Installation and Wiring

11.7.1 TA Circuit Connection

According to the wiring diagram of the device, connect the terminal block of rear AC module with the CT loop using multiple wires, of which the cross-sectional area should be 2.5 ~ 4.0mm^2.

11.7.2 Power Supply, TV, BI and BO, Signal Wiring

According to the wiring diagram of the device, connect the AC, Phoenix terminal of module and the terminal block in the cubicle side with multiple wires.

DC voltage power supply wiring power +, power - should be distinguish in different colors, for example power + (brown), power - (blue).

Power supply, binary inputs & outputs: stranded conductor, 1.0mm^2 ~ 2.5mm^2.

AC voltage inputs: stranded conductor, 1.5mm^2.

Grounding: braided copper cable, 2.5mm^2 ~ 6.0mm^2.

For wires connected to two points, there should be no joint in the middle, and the wire core should not be damaged. If the wire length is not enough during the process of wiring or rewiring, the worker must replace it. There should be no excess wire in the slot. If it is required to

remove the wire, the whole wire must be completely removed.

When wiring the AC terminal of module, current and voltage wires must adopt 12mm size cable lug, to avoid loose contact. Strictly prohibit electric screwdriver, so as to avoid terminals damage.

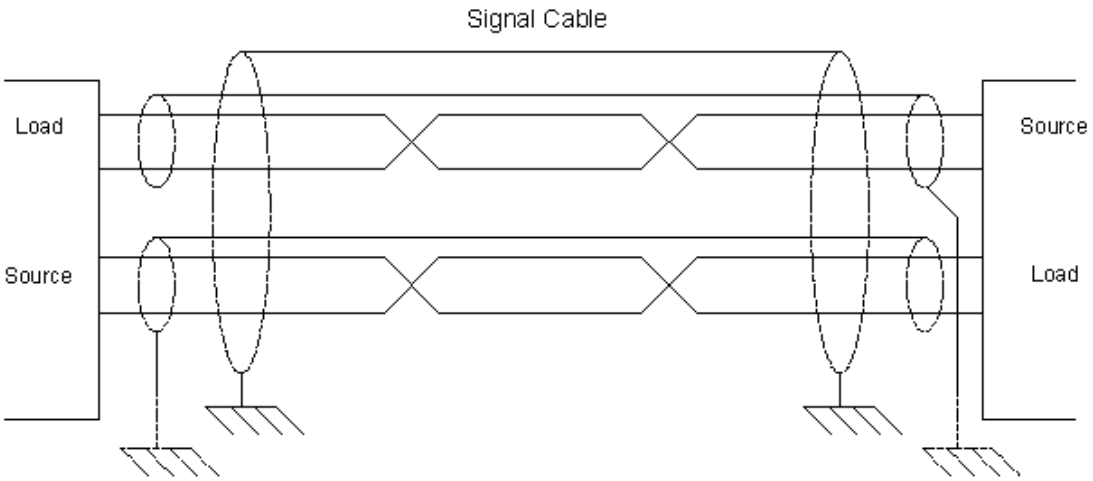
Attention! Never allow the current transformer (CT) secondary circuit connected to this equipment to be opened while the primary system is live. Opening the CT circuit will produce a dangerously high voltage.

11.7.3 Grounding

Use a yellow-green multi-core cable with a cross-section of at least 2.5 mm^2 to connect the grounded copper bars. The cubicle should reliably connected to the secondary ground network.

11.7.4 Shielded cable connection

When using a shielded cable, connect the shielded cable to ground and follow the engineering application method. This includes checking of the appropriate grounding point near the device, such as the grounding point inside the cubicle and the grounding point near the measurement source. Ensure a single shield connection a suitable short cross-sectional wire (maximum 10CM) for ground connection.



11.7.5 Install the optical cable

Care should be taken to handle the cable without substantial bending. The minimum curvature radius of the plastic optical fiber is 15 cm and the glass optical fiber is 25 cm. To use the cable clamp, a loose buffer sleeve should be used.

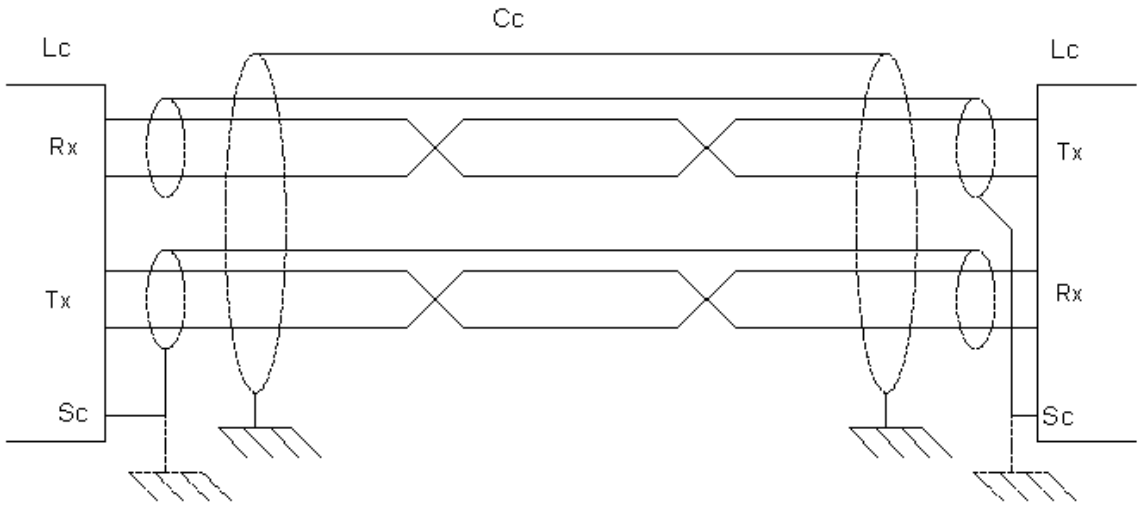
When connecting or removing the optical fiber, please take hold of the connection ends. Do not take the cable. Do not twist, stretch, bend the cable. Invisible damage can increase the attenuation of the fiber and can destroy the communication.

11.7.6 Install the communication cable

When using electrical connections between the protection device and the communication device,

or point-to-point electrical connections between the two protection devices, it is important to install the cables carefully. Due to the low electrical level of communication signals, the factors susceptible to noise interference must be considered.

The best way is to use shielded twisted pair(STP), one for each twisted pair and the other for the all twisted pairs for surround shielding. Each signal uses the twisted pair shown in the following figure to shield each individual twisted-pair cable by connecting its internal shielded cable to the device's ground connection or, alternatively, to a device near the signal transmitter Connected, at the receiving end, shielded line let it hang in the air, not connected with the ground. The outer shield surrounding all twisted pairs is physically connected near each end of the equipment.



Cc: communication cable

Lc: line connector

Rx: receive signal input

Tx: transmit signal output

Sc: shielded (grounding) connection

11.8 Installation check

11.8.1 Check the installation

Check that all terminal screws with external wiring are tightened, the wiring is neat, and all wiring labels are clearly defined.

11.8.2 Confirm the hardware and software version

Hardware and software version information is available on the device label. After the device is powered on, the software version can also be checked through the LCD interface.

11.8.3 Device start

if confirm that the wiring is correct during the installation check, you can supply device with power

and start it.

Configuration file needs to read during device startup process. It needs a certain period of time for the startup process. The startup time is related to the size of configuration file. In general, the startup time is less than 1 minute.

The "HEALTHY" indicator lights up when the unit starts up normally. If a fault is detected during the startup procedure, the "ALARM" indicator is lit and the internal fault code, alarm information can be checked via LEDs.

12 Maintenance

12.1 Maintenance General

A strict and detailed laboratory test is carried out in the development and design of the relay device. All the relay devices are strictly tested according to national or international standards.

The relay device has powerful real-time self-check capability. However, during the long time running of the relay device, there is no real time supervision for the input terminals and output circuits. Therefore, some periodic tests should be done to ensure that the relay is functioning correctly and the external wiring is intact.

The maintenance of the relay device mainly includes the following two conditions:

- Regular testing;
- Failure maintenance

12.2 Regular Testing

Regular testing is to test the normal relay devices in a certain period of time, so as to find potential defects or failures and eliminate hidden dangers to ensure the healthy operation of the devices.

The regular testing cycle depends on a number of factors, such as the environment conditions, the complexity, etc. Advices of CYG are as the following:

- The relay device must be tested for the first time in the first year of operation, mainly including protection logic, AC circuit, tripping circuit and power supply circuit.
- A partial test should be carried out every 3 years, mainly including the inspection of the AC circuit and the tripping circuit.
- An overall test should be carried out every 6 year, mainly including the protection function logic, the AC circuit, the tripping and closing circuit, the power supply circuit.

12.3 Failure Maintenance

Failure maintenance refers to the maintenance of a faulty relay device.

12.3.1 Hardware Failure

1) Check whether the hardware is in trouble or not according to the device alarm signal.
2) visual check of the device
   - Check whether the device has obvious physical fault
   - If you can find a clear physical fault point of the device, please contact CYG for repair or replacement
3) Confirm the scope of the fault
   - Check whether this fault is caused by an external circuit.
   - Carry out the input and output test for the relay device by test instrument.

- If it is determined that the fault belongs to the relay device, please contact CYG for repair or replacement

12.3.2 Software Failure

1) Check whether the hardware is in trouble or not according to the device alarm signal.
2) Try to restart the device and check if the fault is recoverable if possible.
3) If the fault is not recoverable, please contact CYG for repair or replacement

12.4 Replace Failed Modules

If the failure is identified to be in the relay module and the user has spare modules, the user can replace the failed modules to recover the protection device.

Repair at the site should be limited to module replacement. Maintenance at the component level is not recommended.

Before replacement, the user should check that the replacement module has an identical module name and hardware type-form as the removed module. Furthermore, the replaced module should have the same software version. For the replaced analog input module and power supply module, it should be confirmed of the same ratings.

NOTICE!

After replacing modules, it must be checked that the same configuration is set before and after the replacement. If it is not the case, there is a danger of the unintended operation of switchgear taking place or of relay device not running correctly. Persons may also be in danger.

Units and modules must only be replaced while the power supply is switched off and only by appropriately trained and qualified personnel. Strictly observe the basic precautions to guard against electrostatic discharge.

Take anti-static measures such as wearing an earthed wrist band and placing modules on an earthed conductive mat when handling a module. Otherwise, the electronic components may suffer damage. After replacing the main CPU module, check the settings and configurations.

13 Decommissioning and Disposal

13.1 Decommissioning

13.1.1 Switching off

To switch off this relay, break down the cable connected to the power supply module or switch off the external miniature circuit breaker.

13.1.2 Disconnecting cables

Disconnect the cables in accordance with the rules and recommendations made by relational department.

DANGER!

Before disconnecting the power supply cables that connected with the power supply module of this relay, make sure that the external miniature circuit breaker of the power supply is switched off.

DANGER!

To decline the possibility of electrical shock, all current terminal should be shorted before attempting to remove or replace any modules.

13.1.3 Dismantling

The rack of this relay may be removed from the system cubicle, after which the cubicles may also be removed.

DANGER!

When the station is in operation, make sure that there is an adequate safety distance to other operating parts or equipments, especially as dismantling is often performed by unskilled personnel.

13.2 Disposal

In every country there are companies specialized in the proper disposal of electronic waste.

NOTICE!

Each module used in the device is fixed to several specific module type, as oftenly indicated with a label on the backside of the chassis. There are some chances that the modules will be damaged if they are installed in the wrong chassis slot. When removing and replacing modules, it is best to use the label in the chassis as a indicator, so as to make sure each module is installed in the proper slot.

NOTICE!

Strictly observe all local and national regulations when disposing of the device.

14 Connection Diagrams

14.1 Drawing of structure(6U 1/2 19")

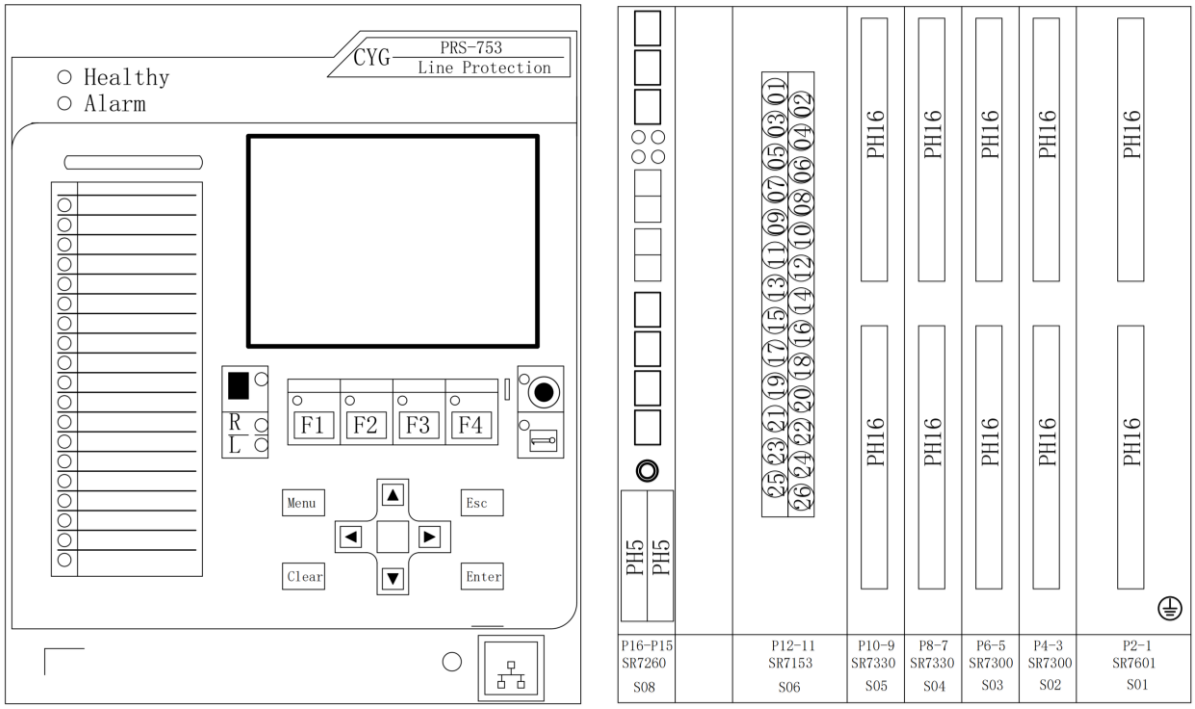
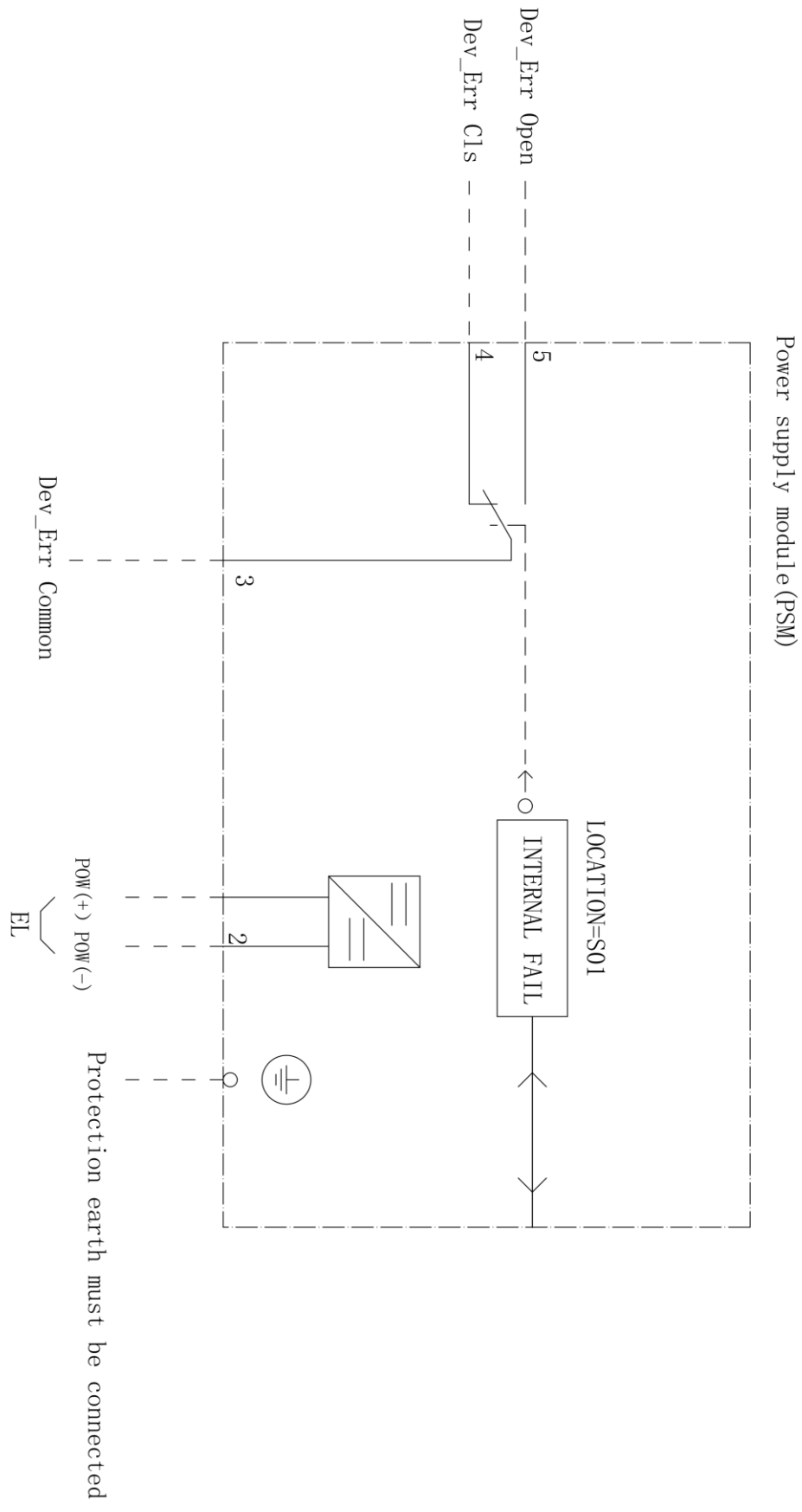


Figure 14.1.1 Drawing of structure

14.2 Drawing of Modules(6U 1/2 19")



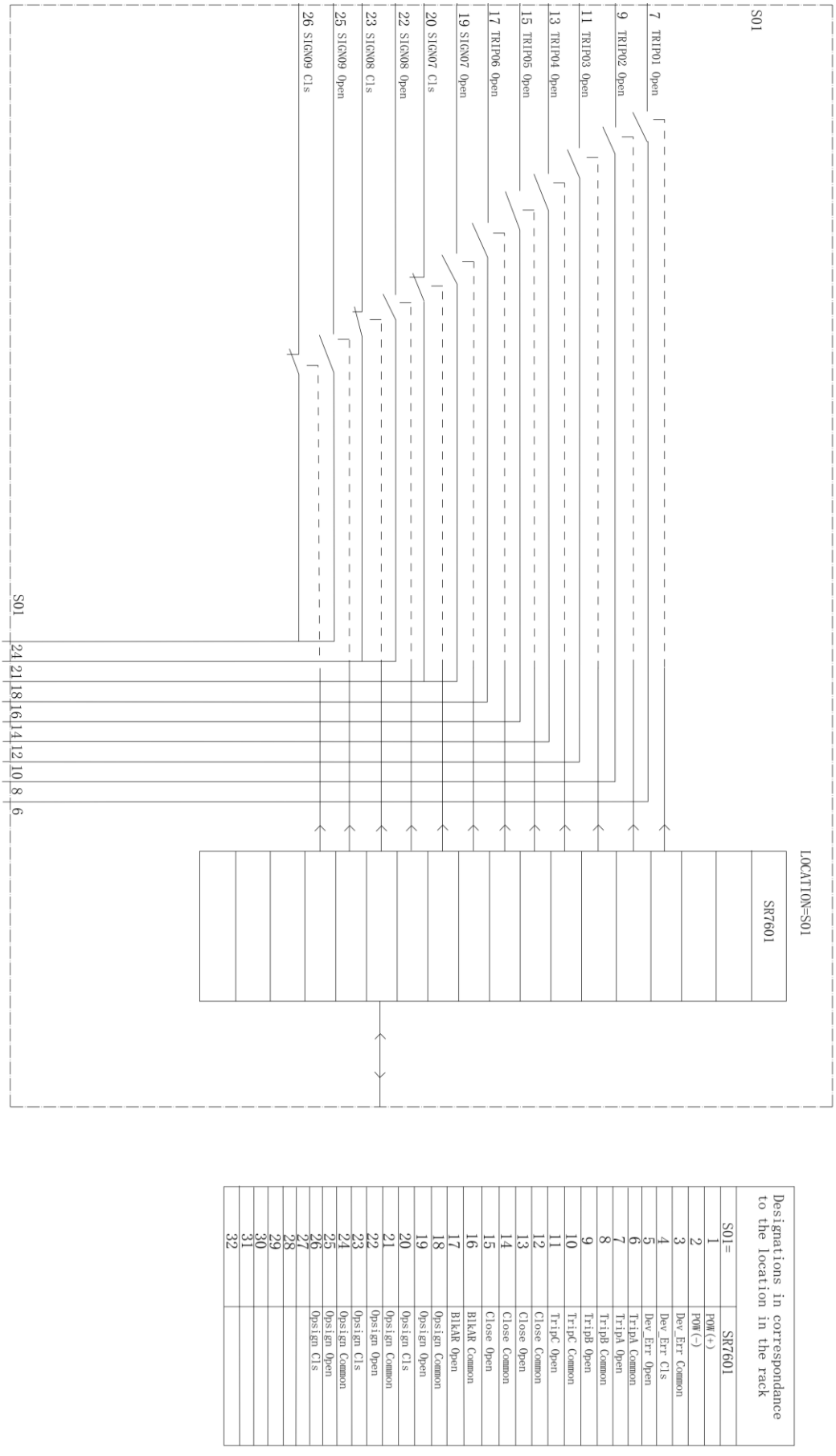


Figure 14.2.1 Power supply module

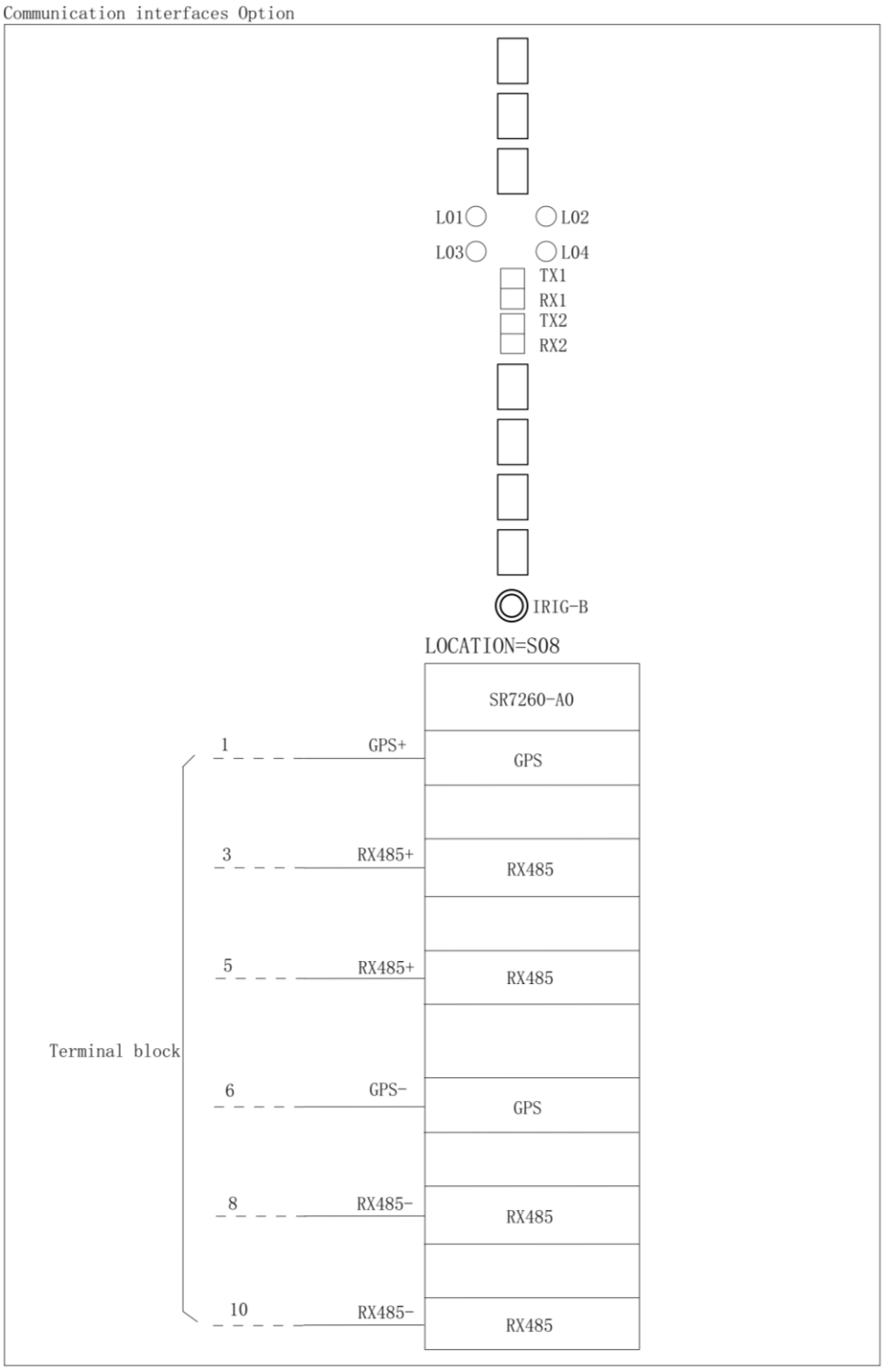


Figure 14.2.2 Communication interfaces

Note: The diagram of all CPU modules are same.

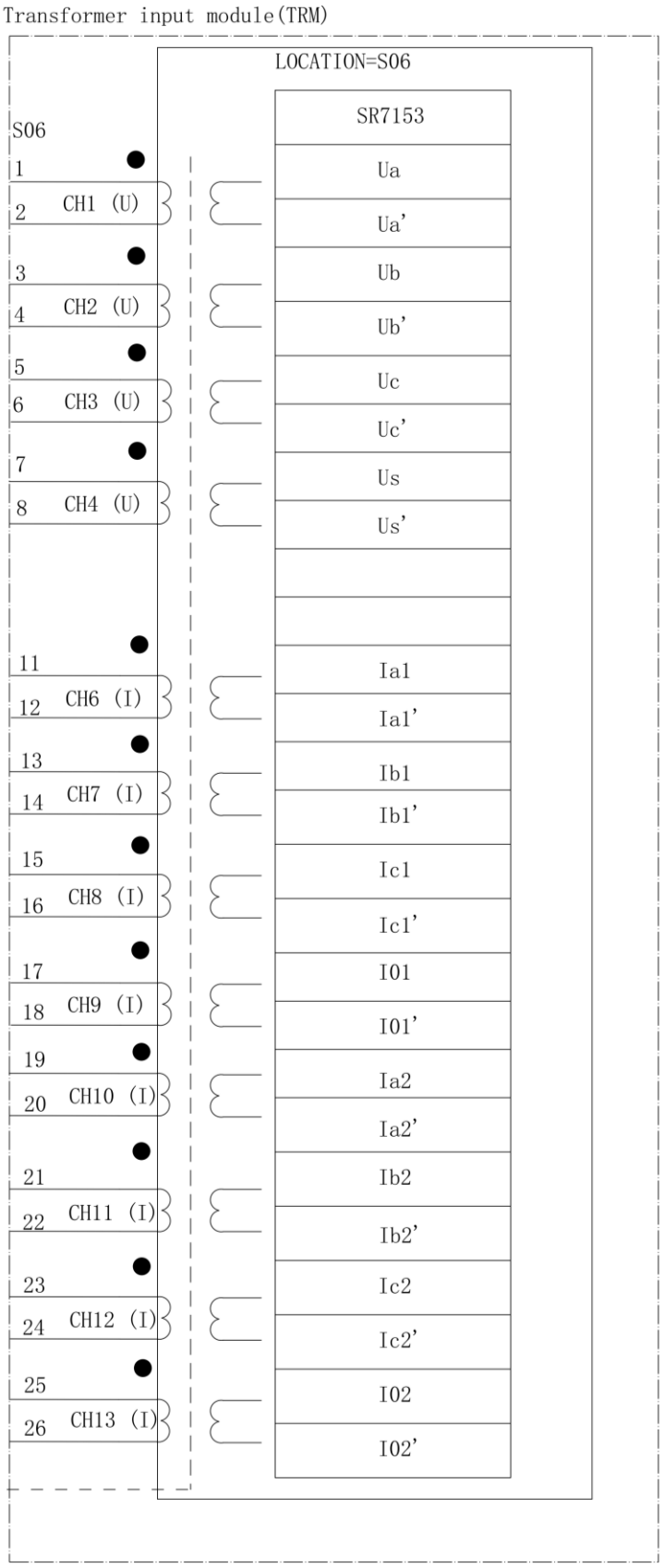


Figure 14.2.3-1 Transformer input module: SR7153-BQ(4VT+8CT)

Note: The default configuration has 4VT+8CT.

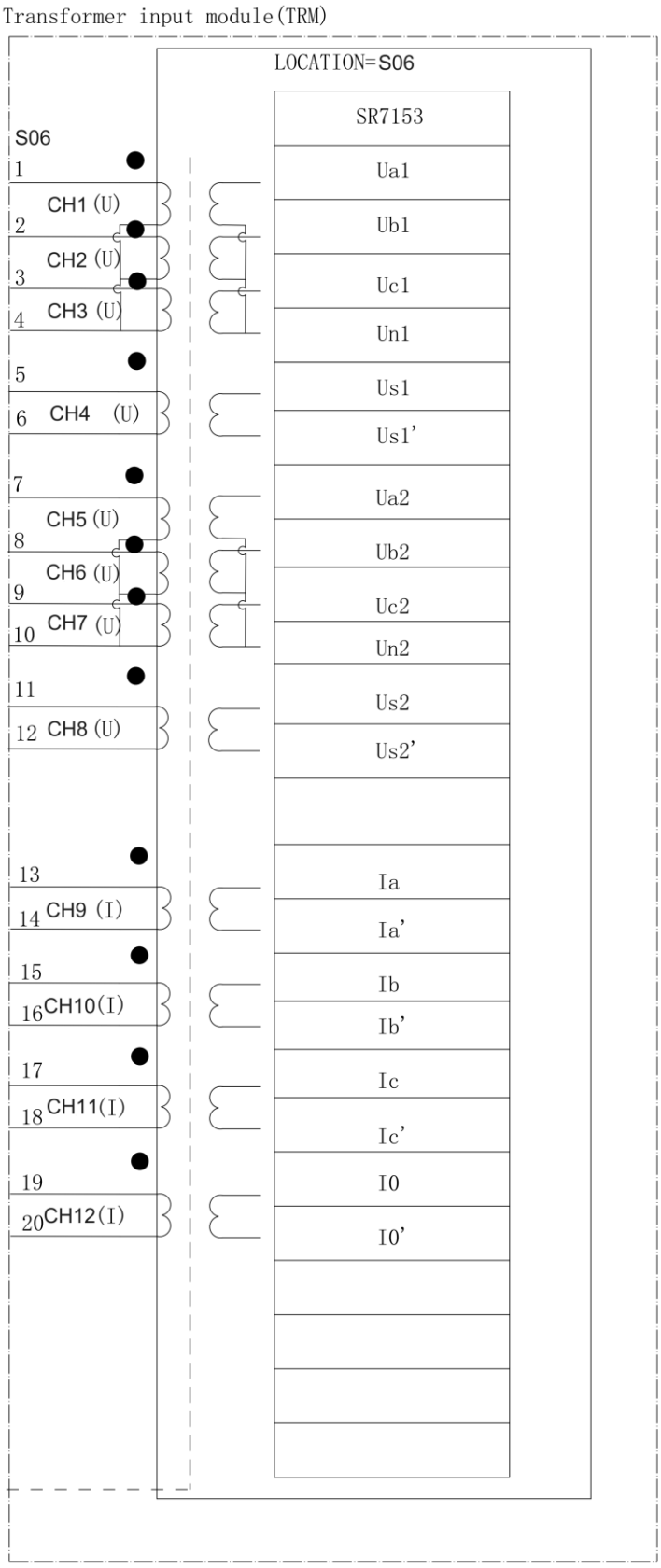
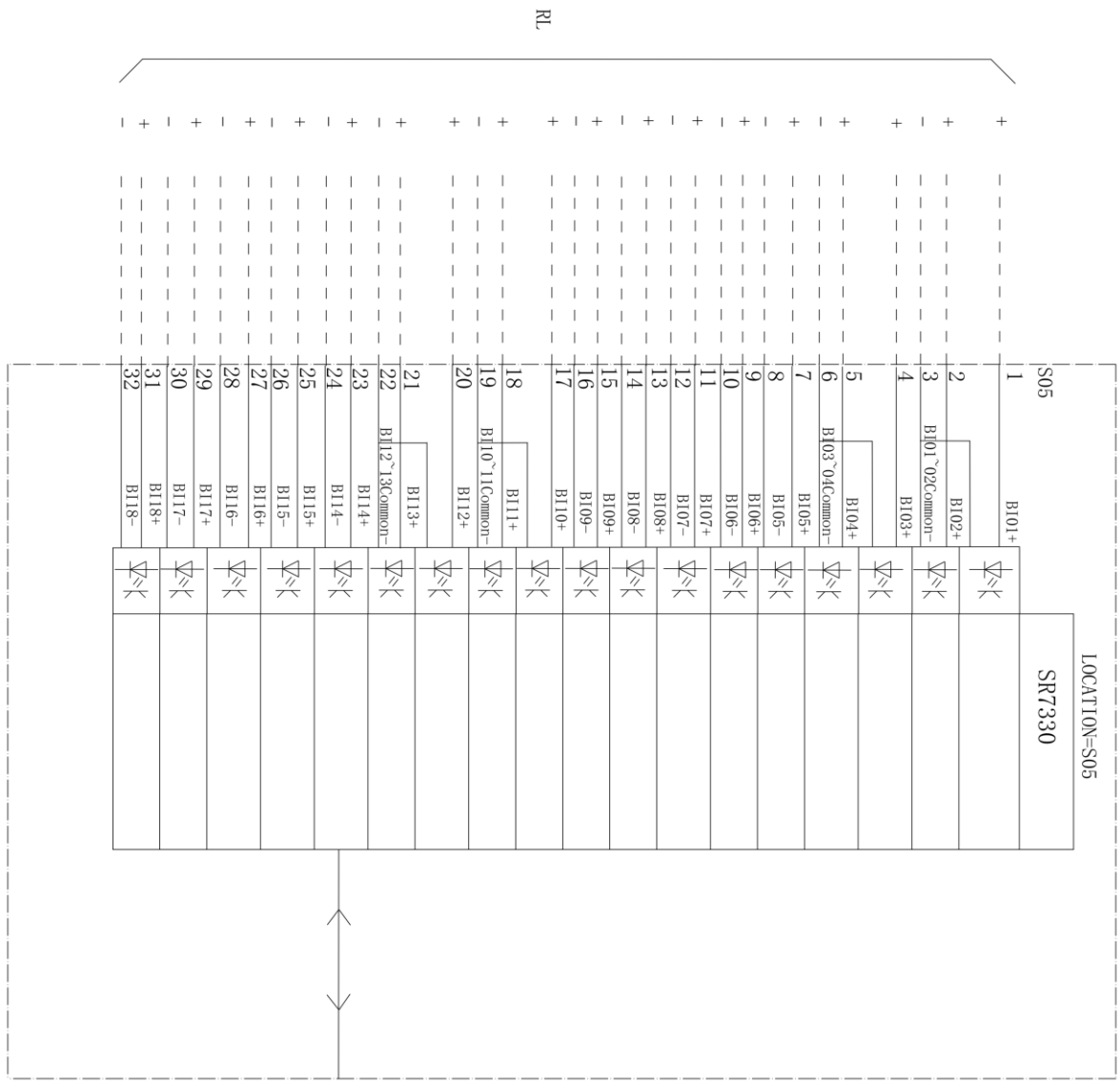


Figure 14.2.3-2 Transformer input module: SR7153-CQ(8VT+4CT)

Note: If the user needs 8VT+4CT, SR7153-CQ can be configured.



Designations in correspondance to the location in the rack

S05=	SR7330
1	85_RecvC+
2	85_Unblk+
3	01~02 common-
4	85_ExTrp+
5	DTT_TT+
6	04~05 common-
7	CTRL_BI_Close01+
8	CTRL_BI_Close01-
9	CTRL_BI_Open01+
10	CTRL_BI_Open01-
11	CTRL_BI_Close02+
12	CTRL_BI_Close02-
13	CTRL_BI_Open02+
14	CTRL_BI_Open02-
15	CTRL_BI_Close03+
16	CTRL_BI_Close03-
17	CTRL_BI_Open03+
18	CTRL_BI_Close04+
19	17~18 common-
20	CTRL_BI_Open04+
21	MCB_Open+
22	20~21 common-
23	85_Recv2+
24	85_Recv2-
25	DTT_Recv+
26	DTT_Recv-
27	BI34+
28	BI34-
29	BI35+
30	BI35-
31	BI36+
32	BI36-

Figure 14.2.4 Binary input module: SR7330

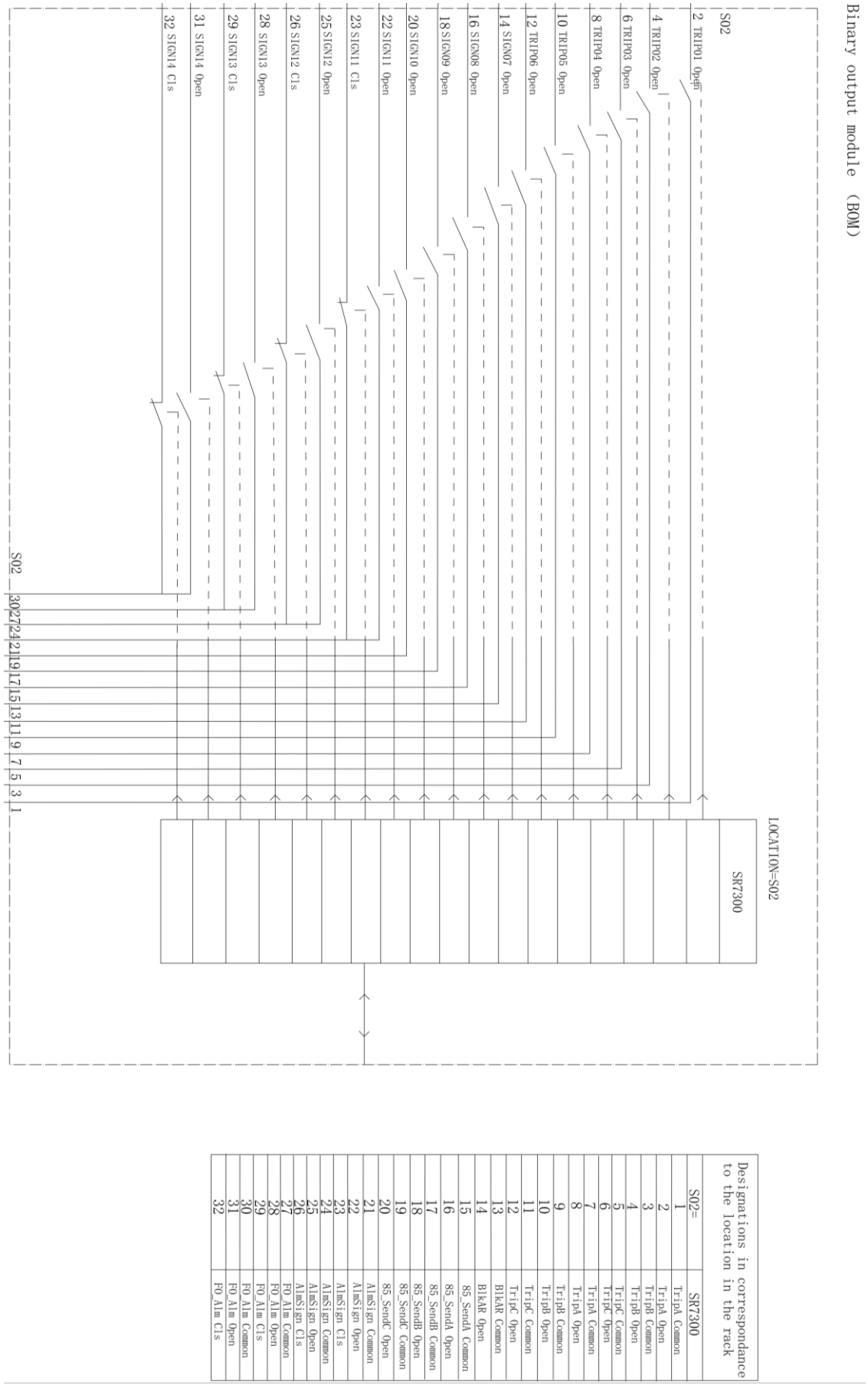


Figure 14.2.5 Binary output module: SR7300

14.3 Drawing of structure(6U 1/1 19")

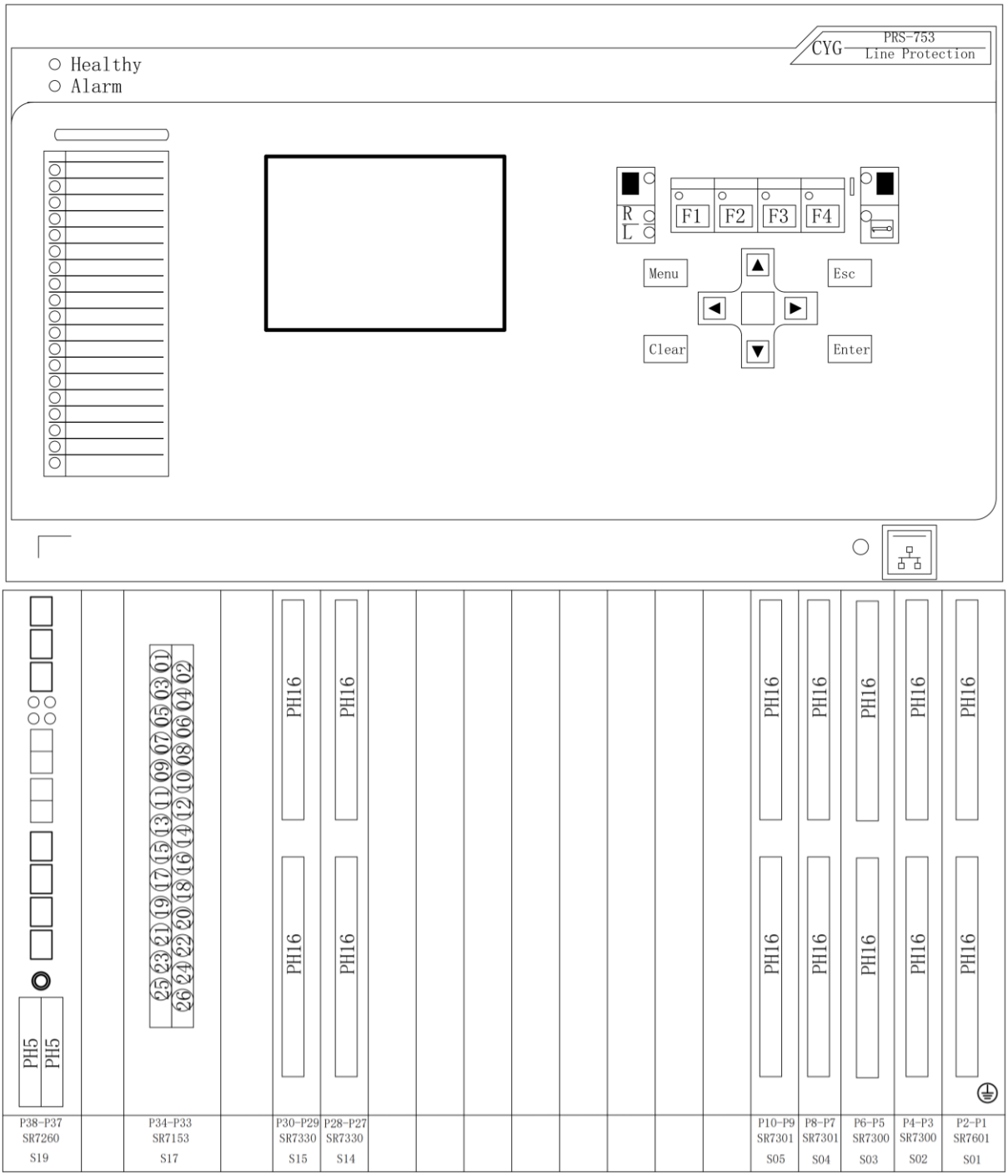
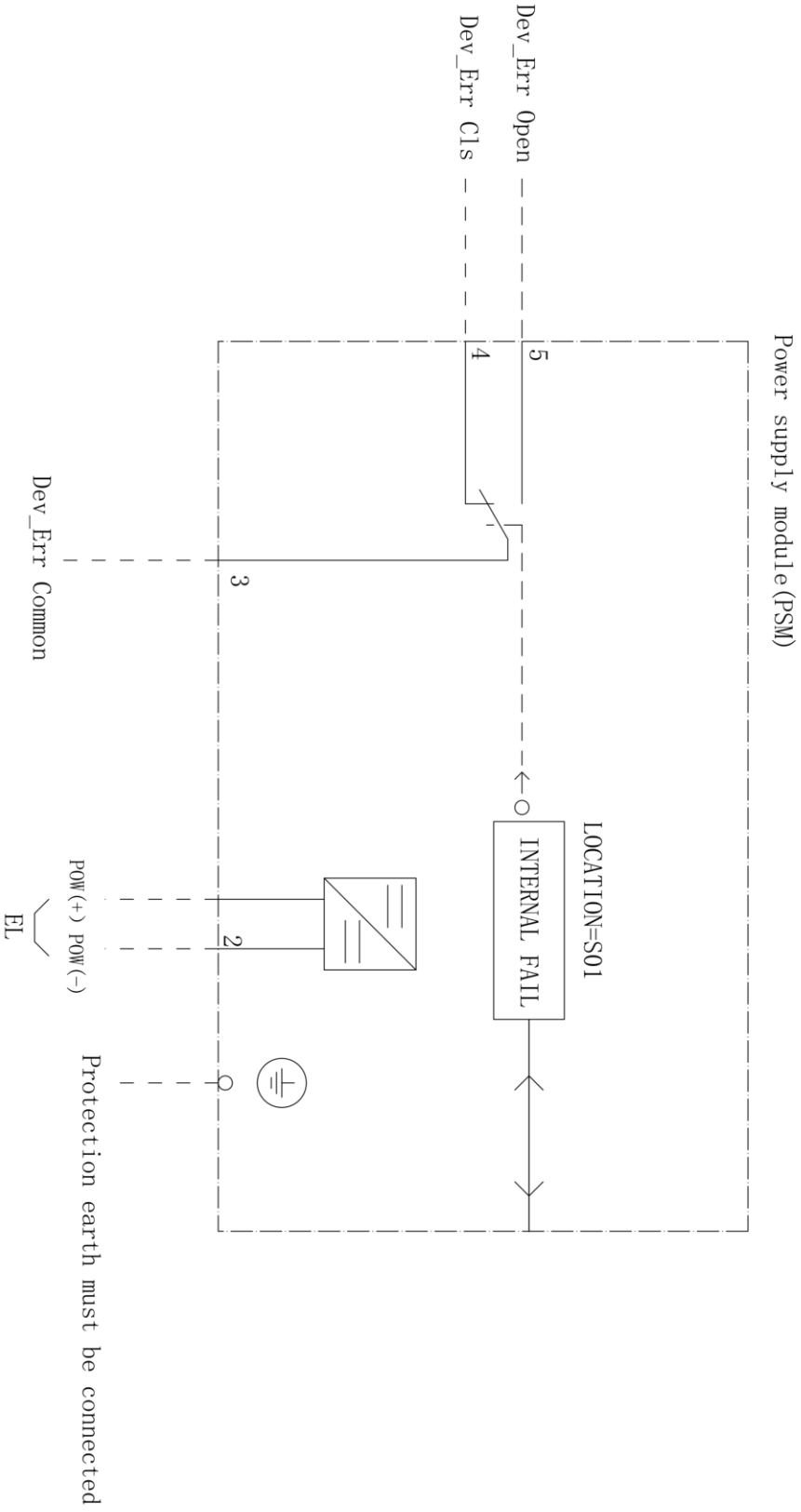


Figure 14.3.2 Drawing of structure

14.4 Drawing of Modules(6U 1/1 19")



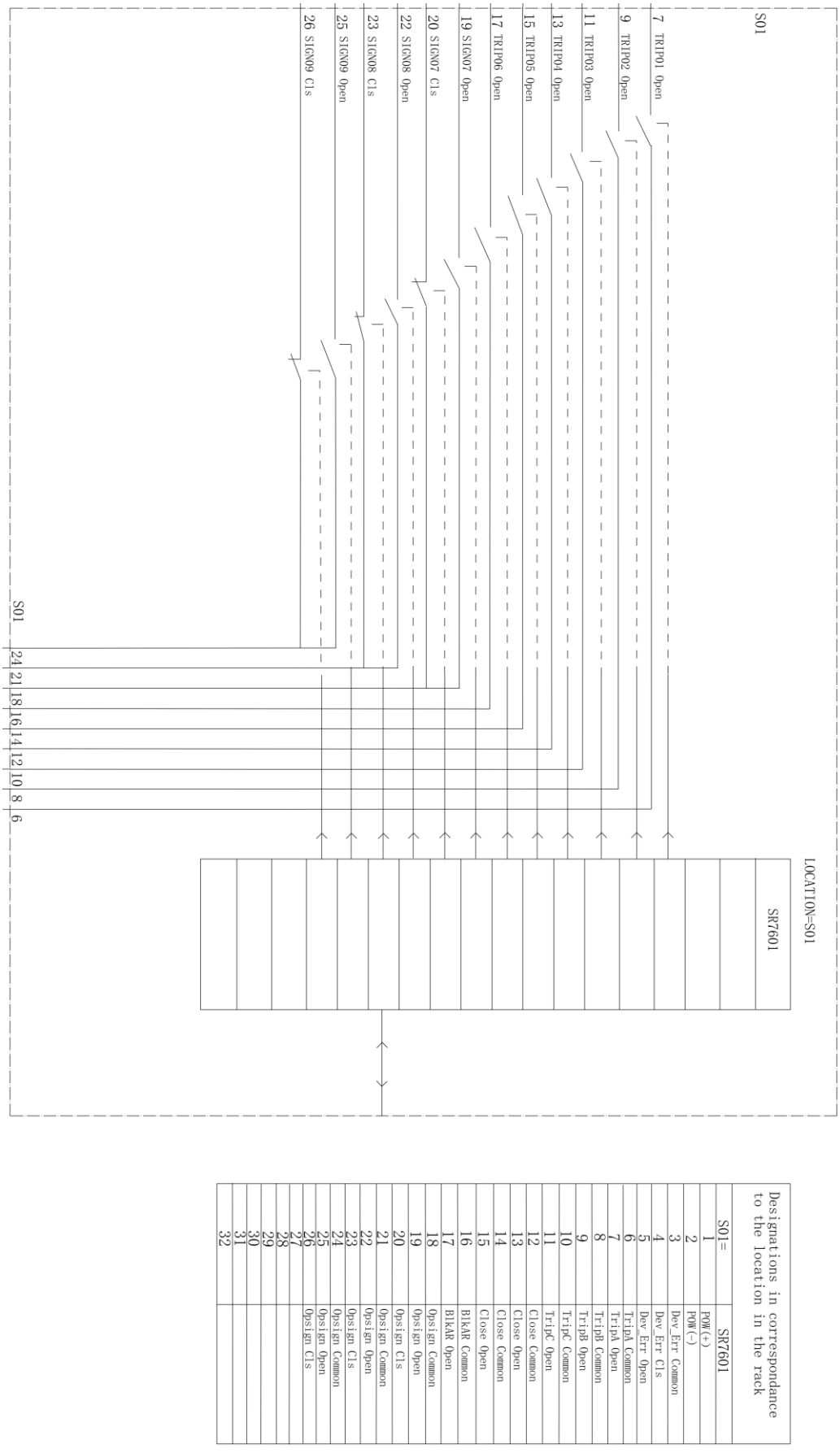


Figure 14.4.1 Power supply module

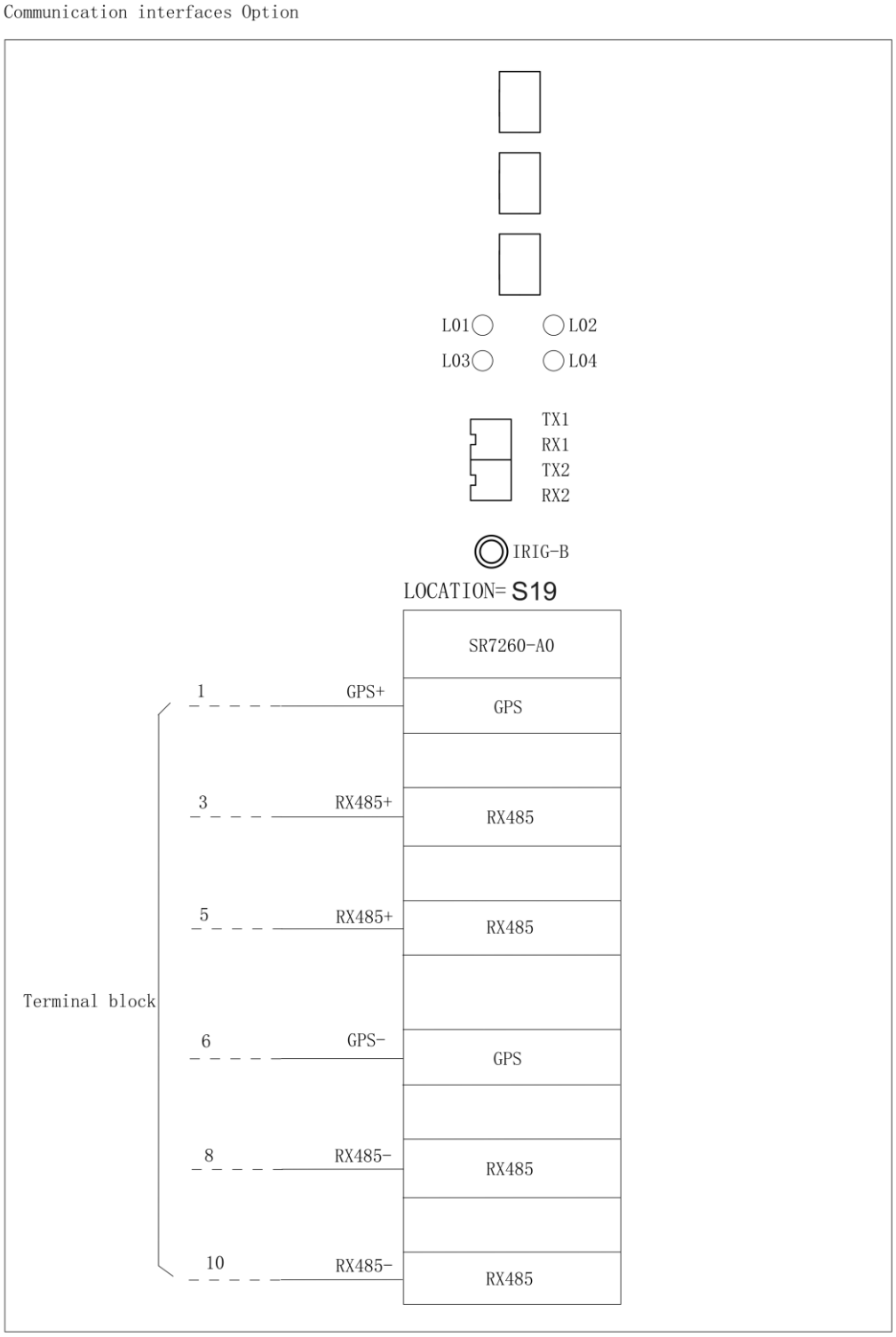


Figure 14.4.2 Communication interfaces

Note: The diagram of all CPU modules are same.

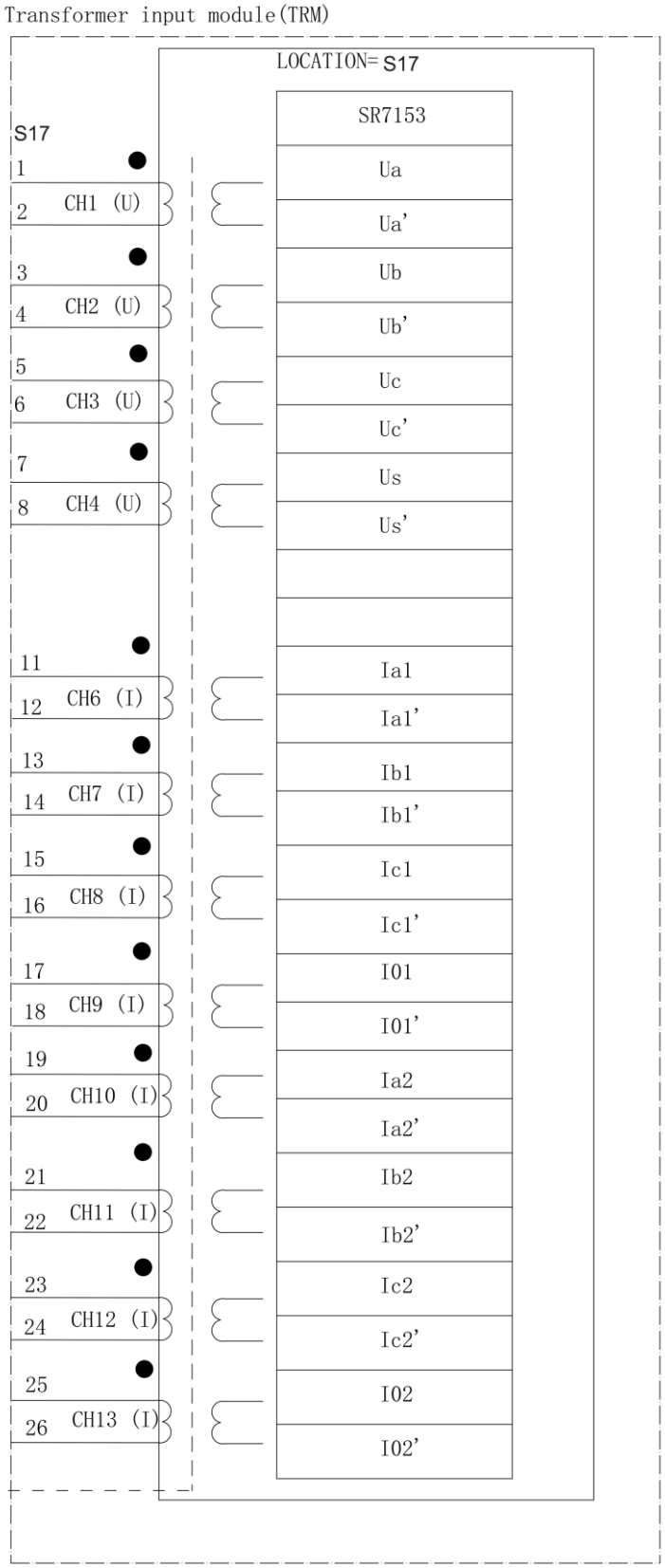


Figure 14.4.3-1 Transformer input module: SR7153-BQ(4VT+8CT)

Note: The default configuration has 4VT+8CT.

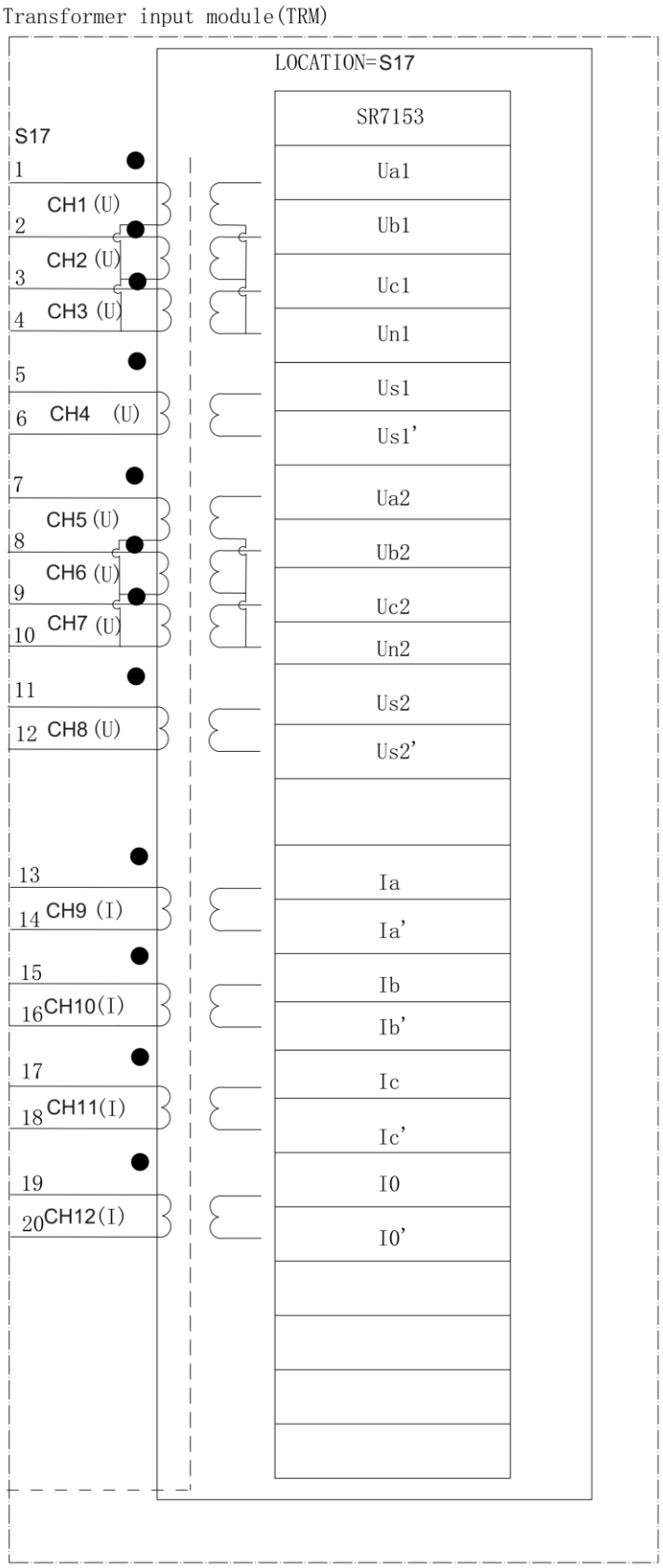


Figure 14.4.3-2 Transformer input module: SR7153-CQ(8VT+4CT)

Note: If the user needs 8VT+4CT, SR7153-CQ can be configured.

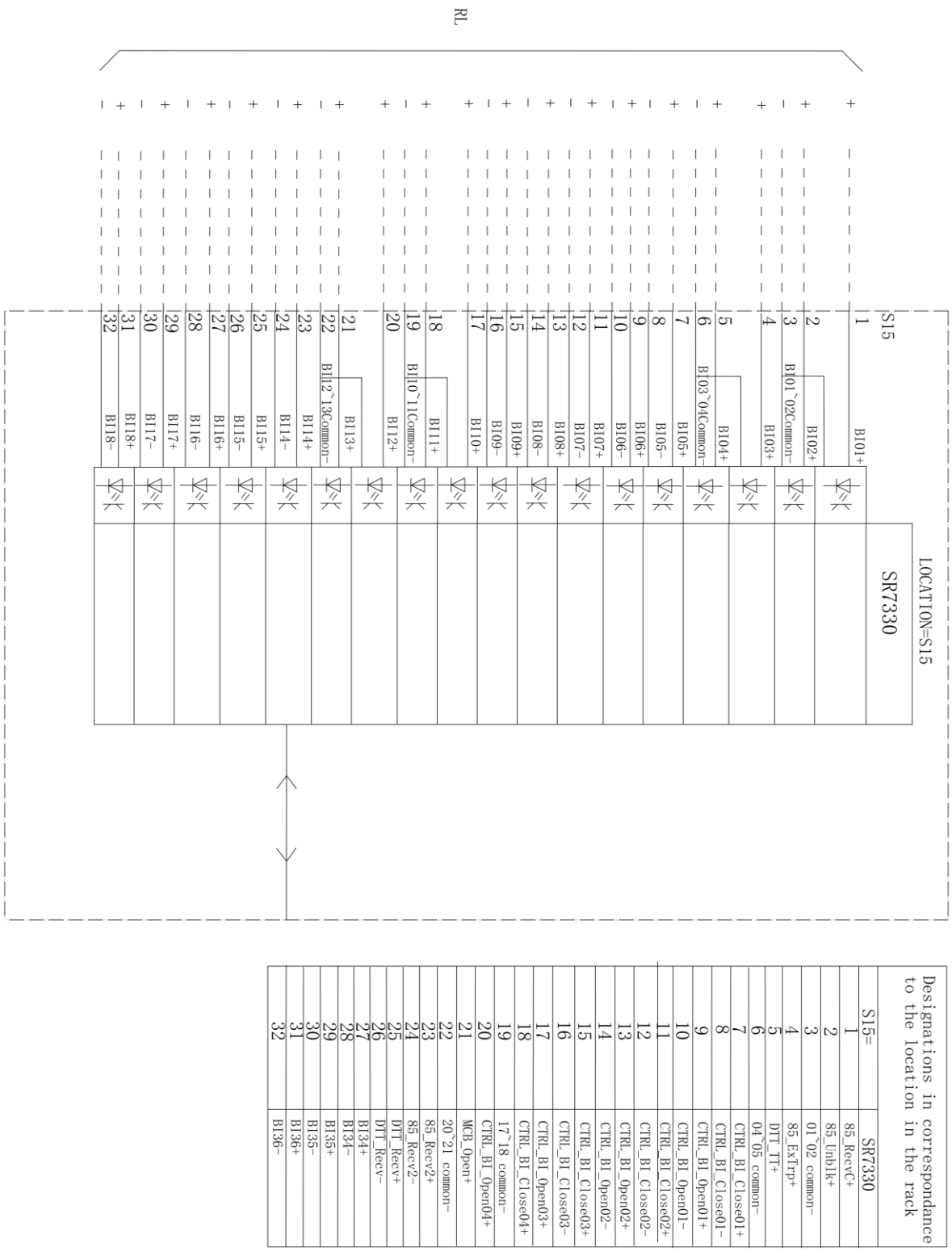


Figure 14.4.4 Binary input module: SR7330

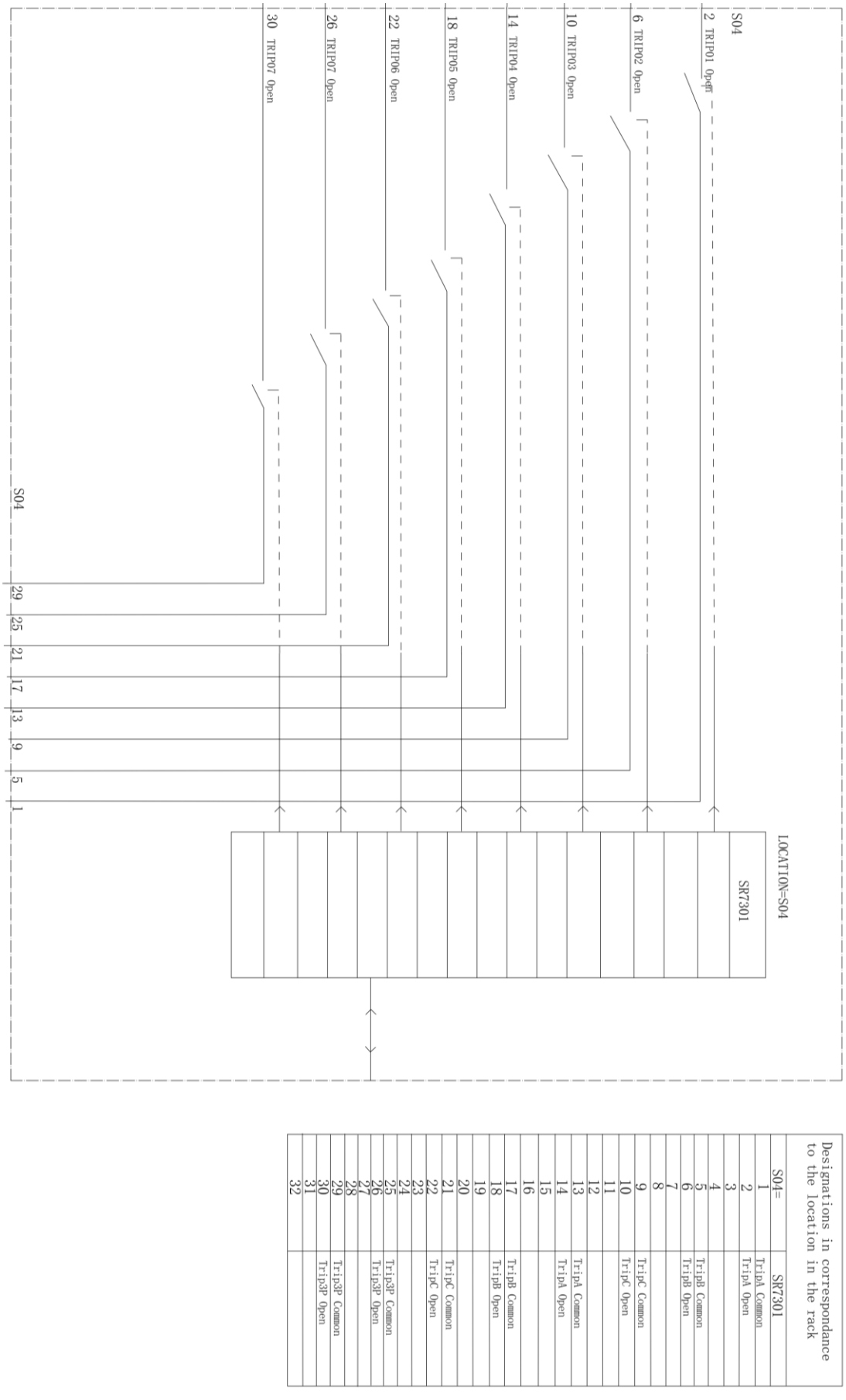


Figure 14.4.5 Binary output module: SR7301

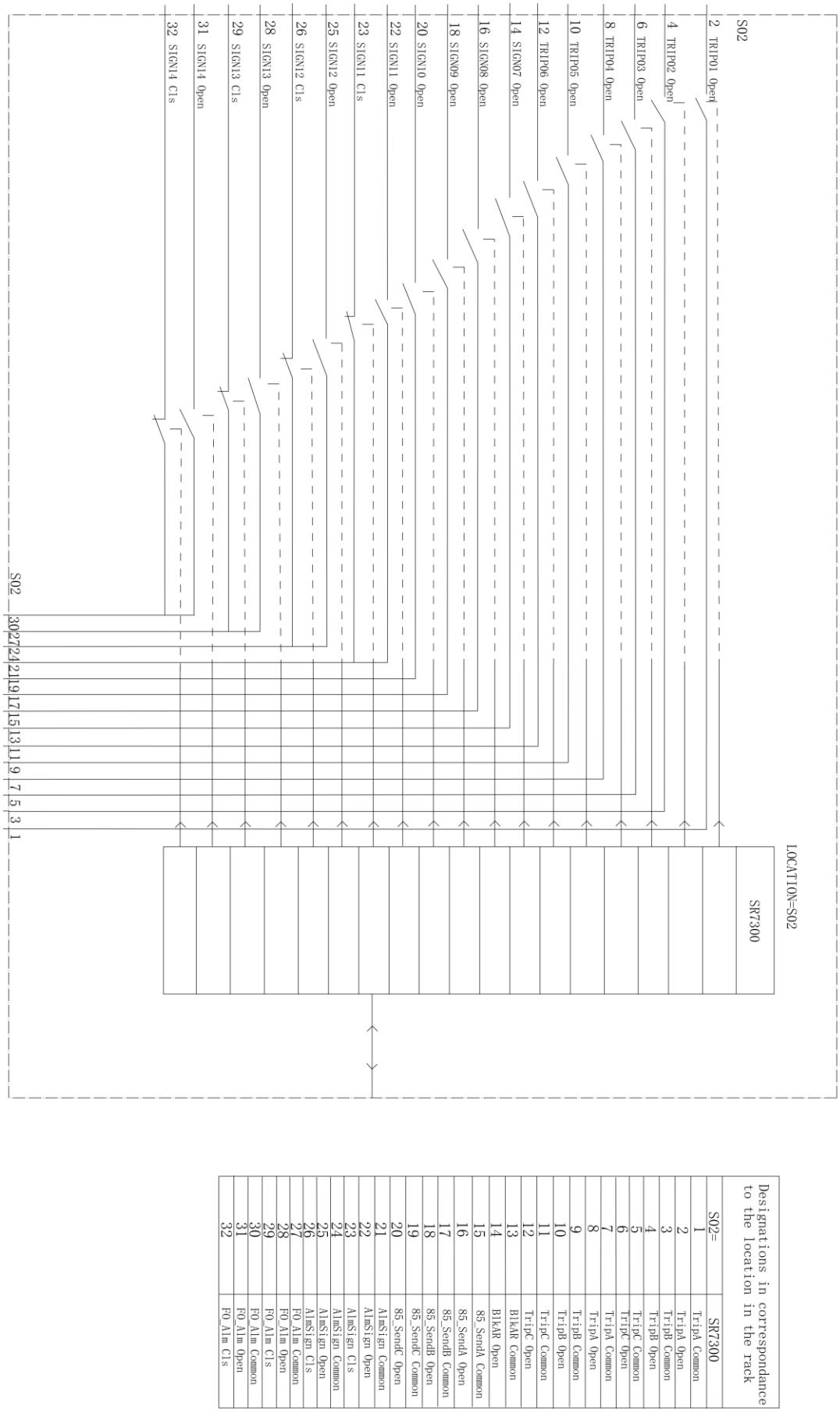


Figure 14.4.6 Binary output module: SR7300

14.5 Drawing of structure(Digital)

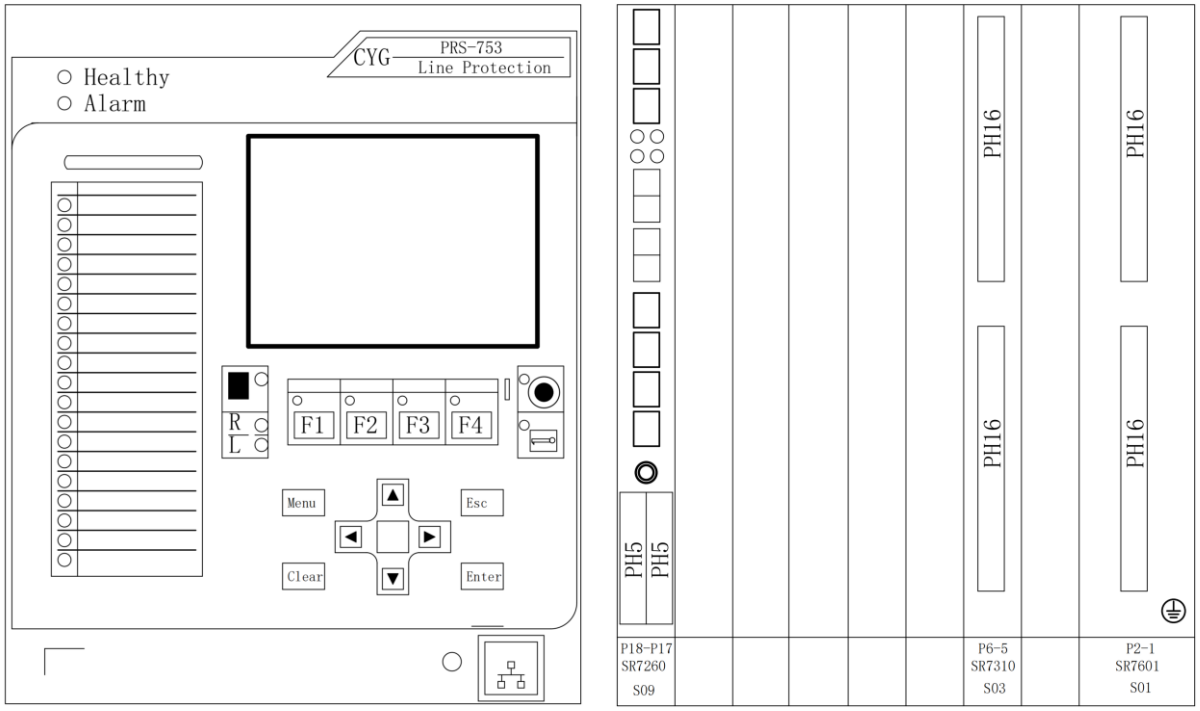
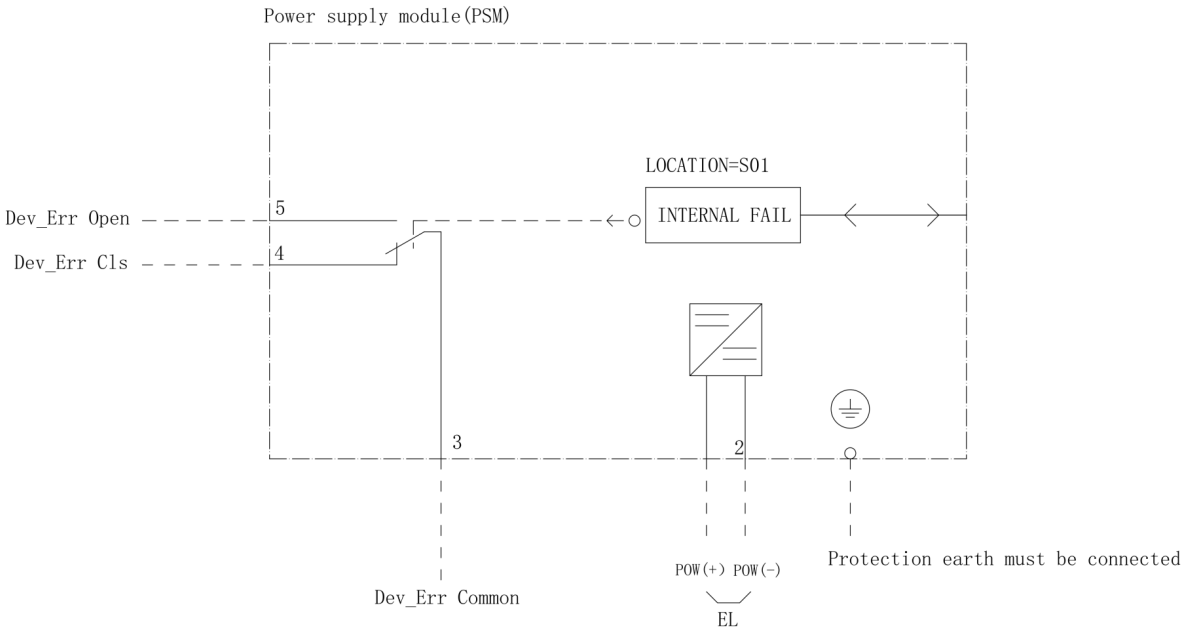


Figure 14.5.1 Drawing of structure

14.6 Drawing of Modules(Digital)



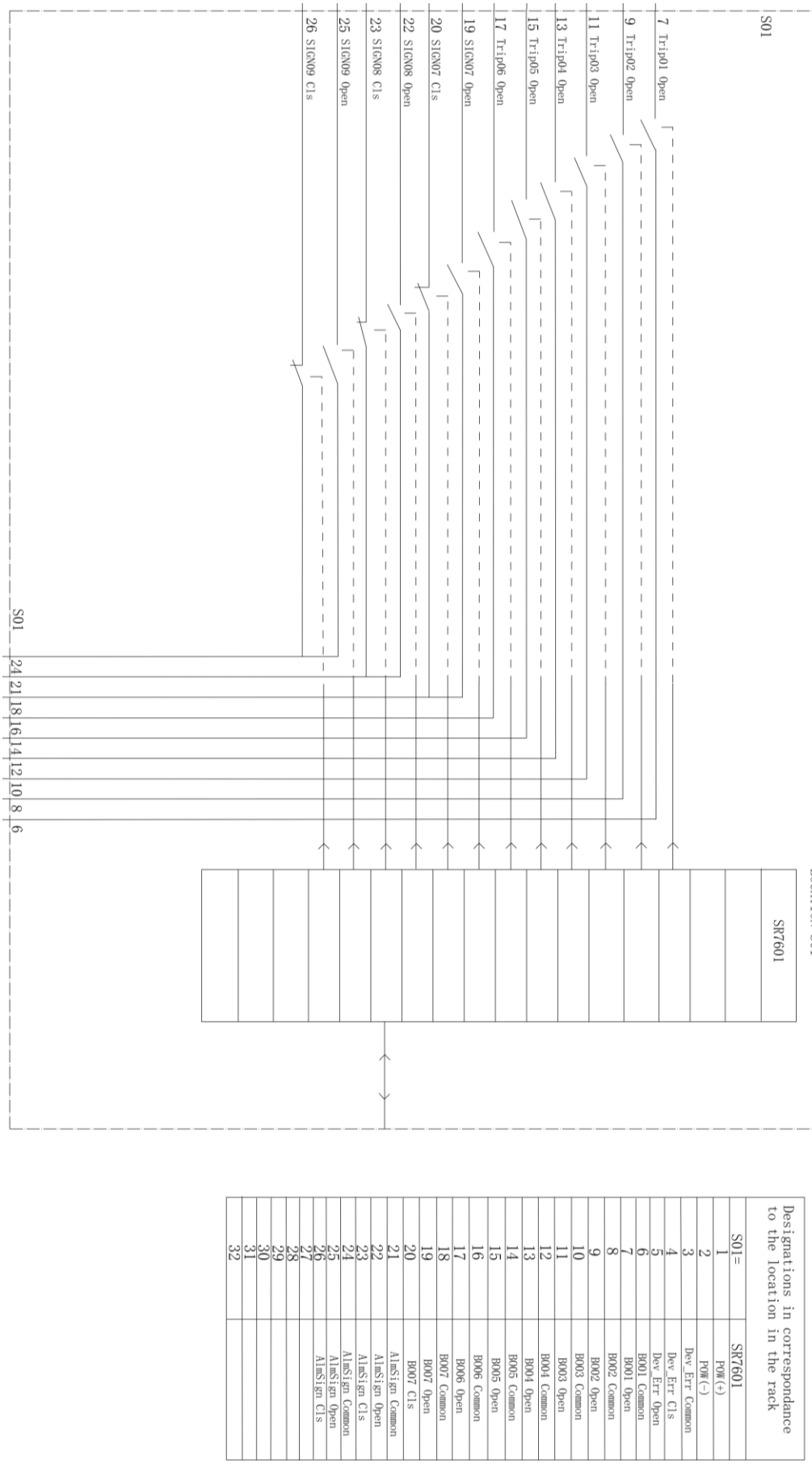


Figure 14.6.1 Power supply module

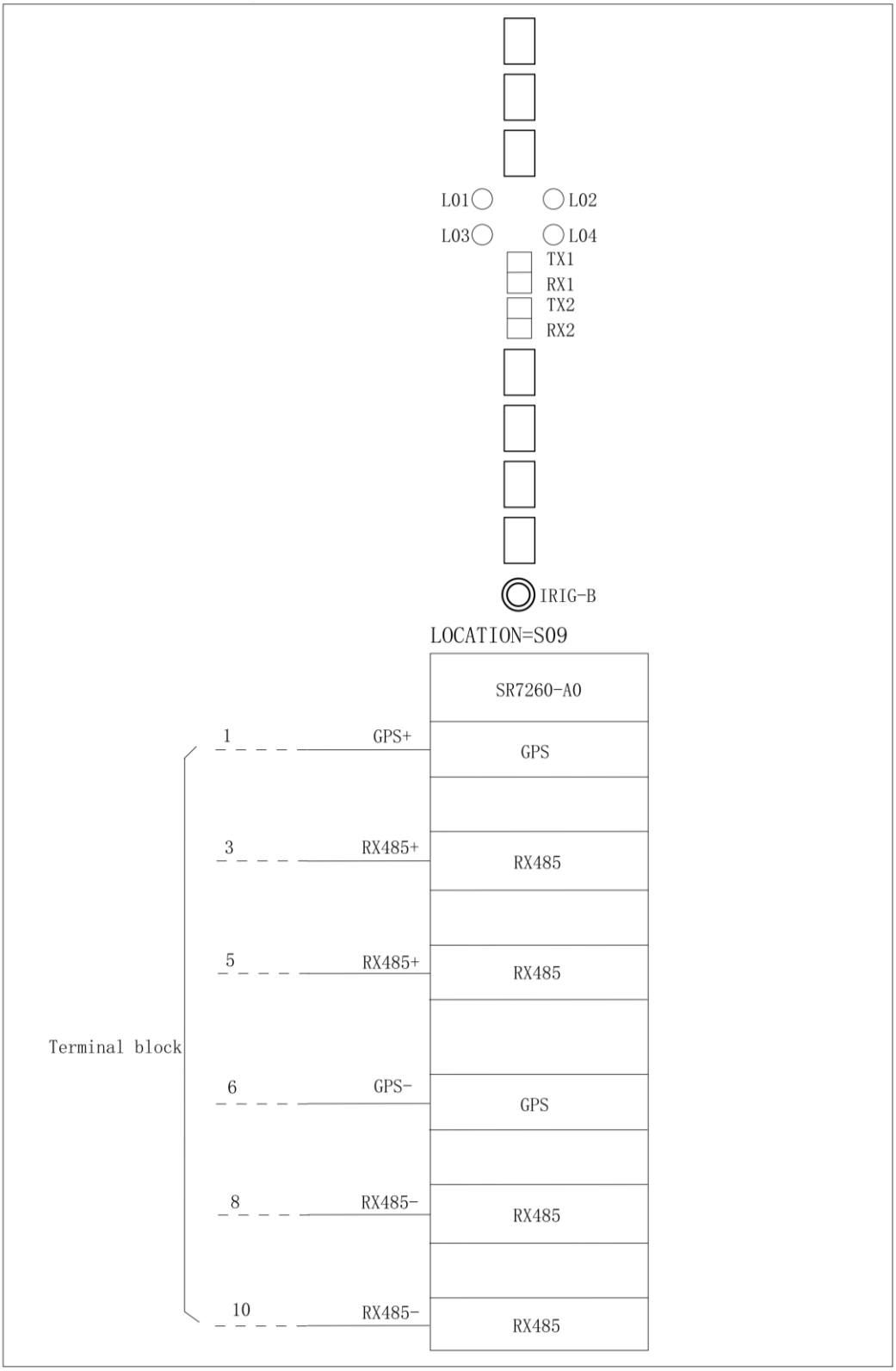
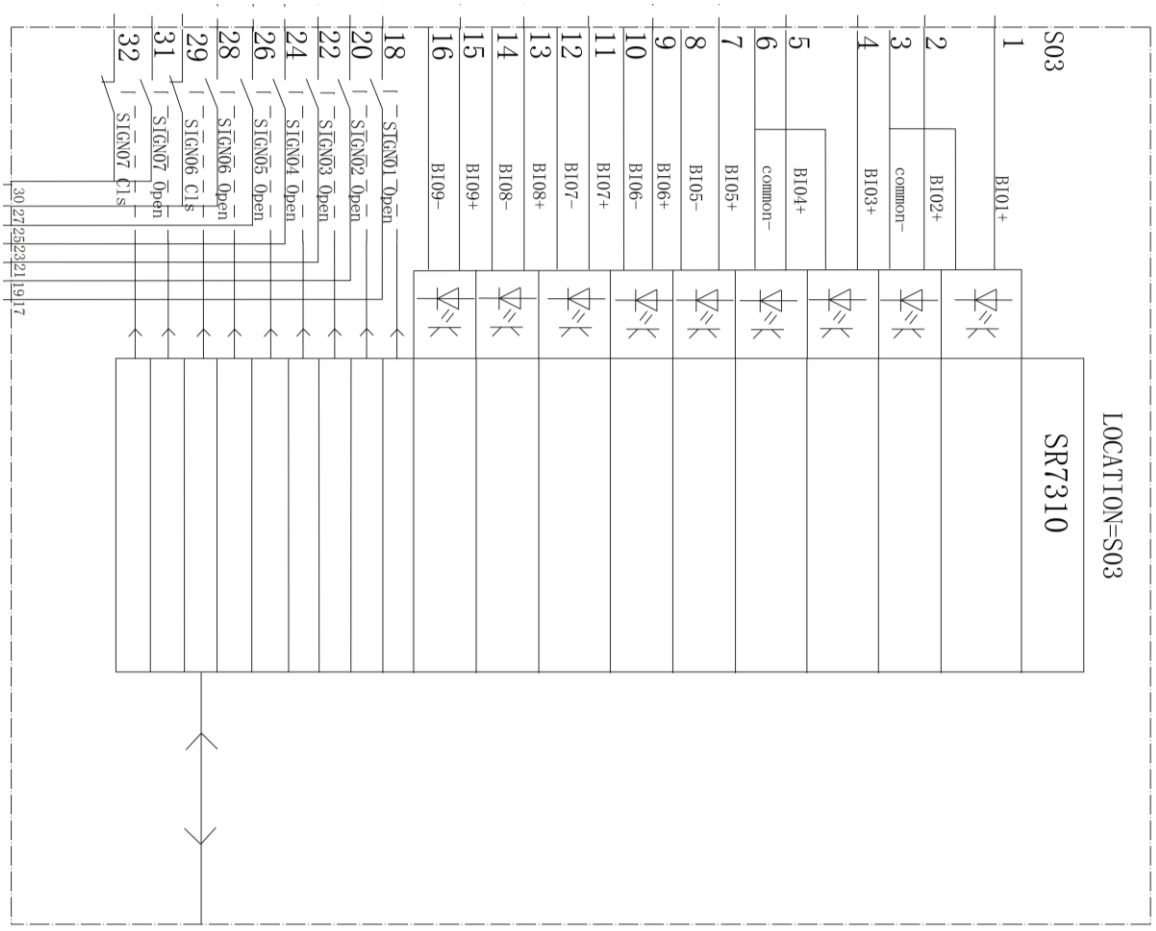


Figure 14.6.2 Communication interfaces

Note: The diagram of all CPU modules are same.



Designations in correspondance to the location in the rack	
S03=	SR7310
1	Reset+
2	Test+
3	01~02Common
4	Remote_Switch+
5	85_Abnor_Ch+
6	04~05Common
7	85_RecvA+
8	85_RecvA-
9	85_RecvB+
10	85_RecvB-
11	85_RecvC+
12	85_RecvC-
13	85_Recv2+
14	85_Recv2-
15	DTT_Recv+
16	DTT_Recv-
17	85_SendA Common
18	85_SendA Open
19	85_SendB Common
20	85_SendB Open
21	85_SendC Common
22	85_SendC Open
23	85_Send2 Common
24	85_Send2 Open
25	DTT_Send Common
26	DTT_Send Open
27	B006 Common
28	B006 Open
29	B006 Cls
30	B007 Common
31	B007 Open
32	B007 Cls

Figure 14.6.3 Binary input/Output module: SR7310

15 Manual Version History

In the current version of the instruction manual, several descriptions on existing features have been modified.

Table 15-1 Manual version and modification history records

Manual Version		Software Version	Date	Description of change
Source	New			
Beta	1.00	1.00	2014-04-15	Form the original manual.
1.00	1.01	1.01	2015-05-21	Update the number of the binary inputs and binary outputs.. Add the binary input hardware demo diagrams in the binary input tables. Update the description of IEC61850 dual-MMS Ethernet.
1.01	1.02	1.02	2016-01-24	Add parameters of fault location function. Output TEMP_RL is added Internal improvements. Update the configurable signals.
1.02	1.03	1.10	2016-08-16	Update the communication description. Update the mechanical specifications. Update the main CPU module picture. Update the setting list.
1.03	2.01	1.20	2017-12-16	Update all the protection functions. Add the “4.2 Supervision Alarm and Block” chapter Increase the amount of the terminal of BI module. Update the logic diagram of the Three-phase thermal overload protection. Update the content of the “9 Communication Protocol” chapter.
2.01	2.02	2.00	2018-2-28	Modify the description of the protection functions. Add programmable IDMT function
2.02	2.03	2.03	2018-08-24	Add GPS time synchronization IEEE 1588
2.03	2.04	2.03	2019-03-26	Modify parameters of electrical specifications.
2.04	2.05	2.03	2023-09-20	Update 87L logic: add two slopes of steady-state current differential protection.
2.05	2.06	2.03	2024-03-11	Update 25SYN logic: the dead charge check logic can apply below two conditions: Voltage selects bus VT for protection calculation, line VT for synchronism voltage. Voltage selects line VT for protection calculation, bus VT for synchronism voltage.